DRD6 WP4 electronics and DAQ

Ch. de LA TAILLE DRD6 11 April 2024

Organization for Micro-Electronics desiGn and Applications

DRD6 (calorimetry) readout schemes

Name	Track	Active media	readout
LAr	2	LAr	cold/warm elx"HGCROC/CALICElike ASICs"
ScintCal	3	several	SiPM
Cryogenic DBD	3	several	TES/KID/NTL
HGCC	3	Crystal	SiPM
MaxInfo	3	Crystals	SIPM
Crilin	3	PbF2	UV-SiPM
DSC	3	PBbGlass+PbW04	SiPM
ADRIANO3	3	Heavy Glass, Plastic Scint, RPC	SIPM
FiberDR	3	Scint+Cher Fibres	PMT/SiPM,timing via CAENFERS, AARDVARC-v3,DRS
SpaCal	3	scint fibres	PMT/SiPMSPIDER ASIC for timing
Radical	3	Lyso:CE, WLS	SiPM
Grainita	3	BGO, ZnWO4	SiPM
TileHCal	3	organic scnt. tiles	SiPM
GlassScintTile	1	SciGlass	SiPM
Scint-Strip	1	Scint.Strips	SiPM
T-SDHCAL	1	GRPC	pad boards
MPGD-Calo	1	muRWELL,MMegas	pad boards(FATIC ASIC/MOSAIC)
Si-W ECAL	1	Silicon sensors	direct withdedicated ASICS (SKIROCN)
Si/GaAS-W ECAL	1	Silicon/GaAS	direct withdedicated ASICS (FLAME, FLAXE)
DECAL	1	CMOS/MAPS	Sensor=ASIC
AHCAL	1	Scint. Tiles	SiPM
MODE	4	-	-
Common RO ASIC	4	-	common R/O ASIC Si/SiPM/Lar

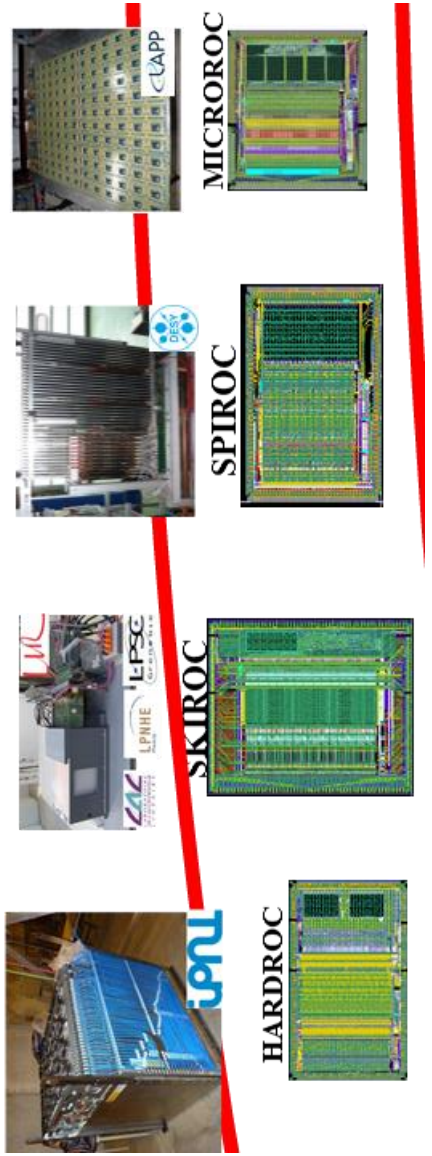
DRD6 Common readout ASICs proposal [AGH, Omega, Saclay]

- Develop readout ASIC family for DRD6 prototype characterization
  - Inspired from CALICE SKIROC/SPIROC/HARDROC/MICROROC family
  - Targeting future experiments as mentionned in ICFA document (EIC, FCC, ILC, CEPC…)
  - Addressing embedded electronics and detector/electronics coexistence
  - Detector specific front-end but common backend

  ⇒ allows common DAQ and facilitates combined testbeam

- Start from HGCROC / HKROC : Si and SiPM
  - Reduce power from 15 mW/ch to few mW/ch. Lower occupancy, slower speed
  - Allows better granularity or LAr operation
  - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
  - Extend to MCPs (PID) or HRPPD. First tests with EIC calo/PID

- Several other ASICs R/Os also developed in DRD6 and it is good !
  - FLAME/FLAXE, FATIC…
  - Waveform samplers : commercial or specific (e.g. SPIDER)
  - DECAL



Example : HGCROC (CMS HGCAL)

Overall chip divided in two symmetrical parts

- Each half is made of:
  - 39 channels: 36 channels, 2 common-mode, 1 calibration
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

Measurements

- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.16 fC binning. TOT: 2.5 fC binning
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows

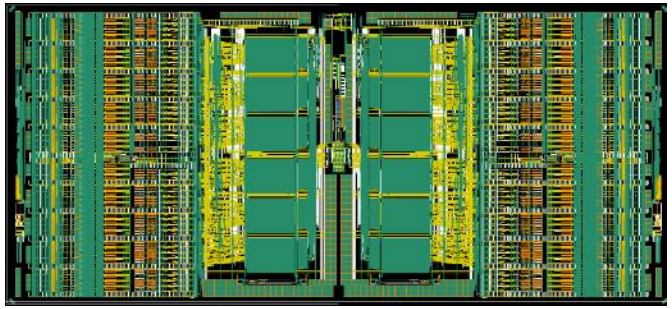
- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links (CLPS)
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links (CLPS)

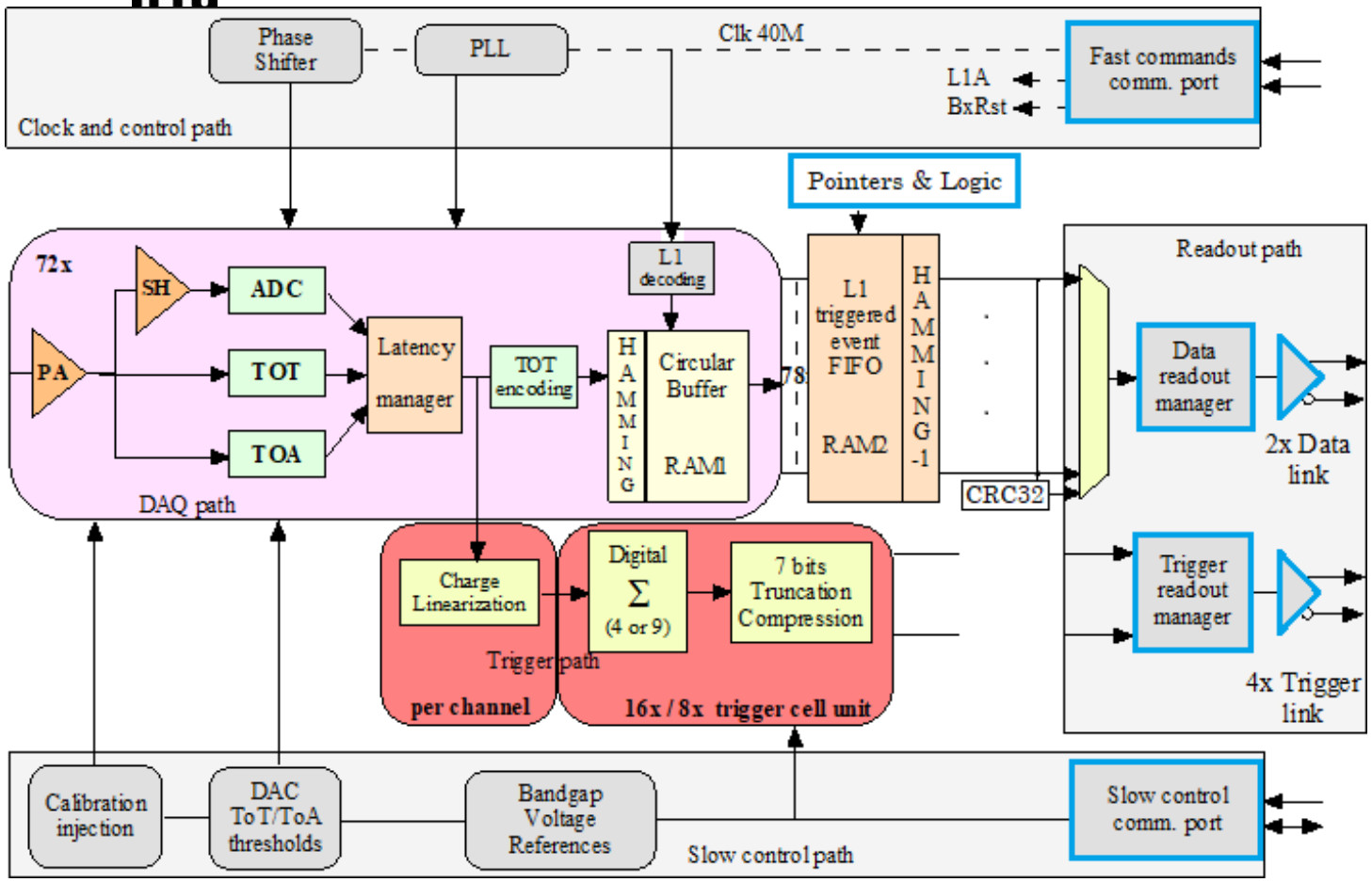
Control

- Fast commands
- $Q_{MIP}/Cd \sim 3\ fC/30\ pF = 100\ \mu V$
- I2C protocol for slow control

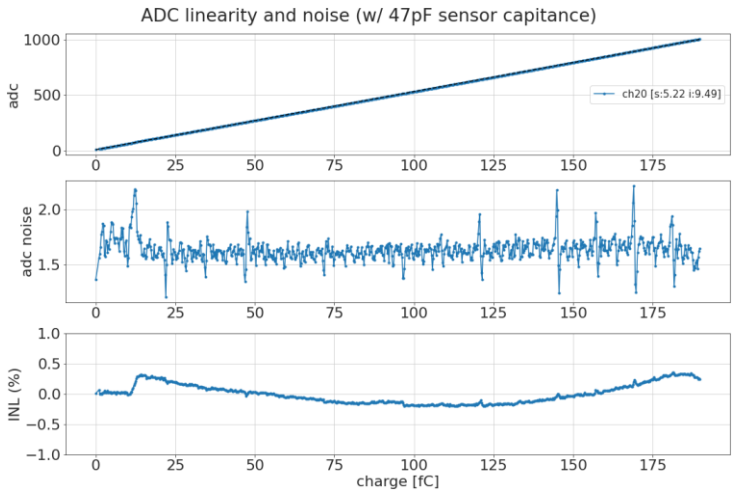
Ancillary blocks

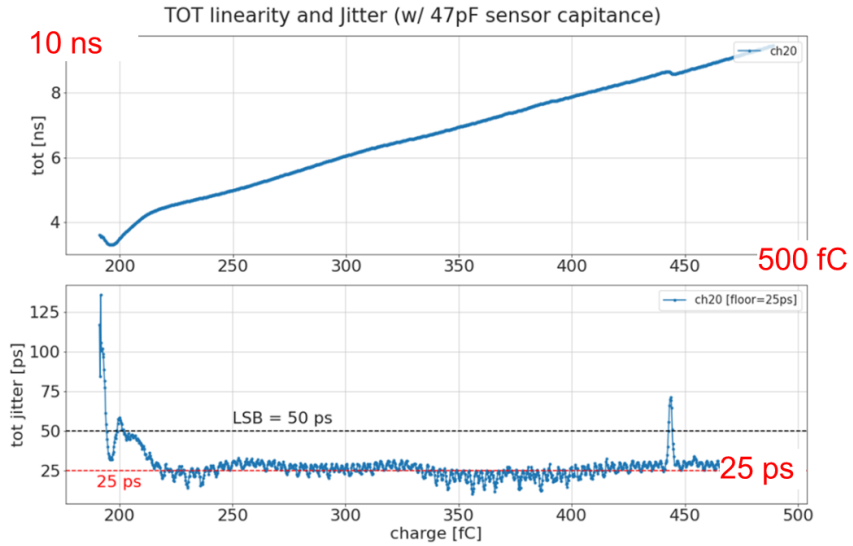
- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain

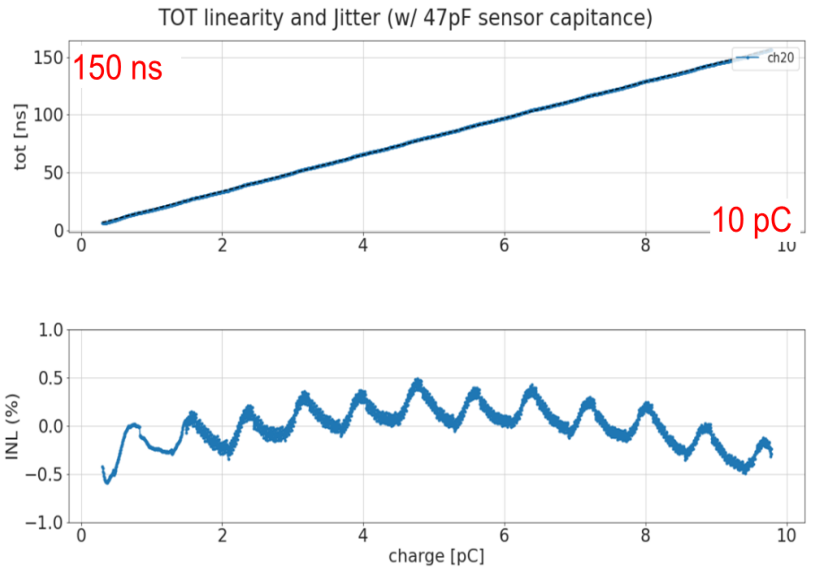


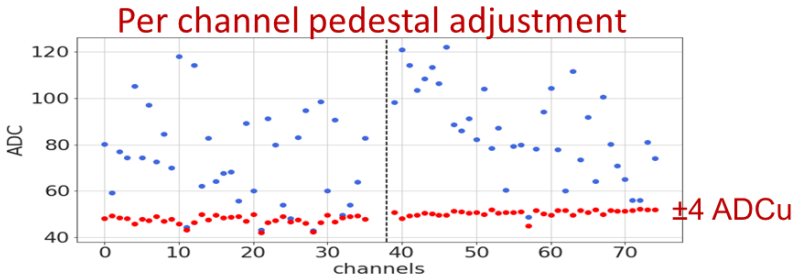


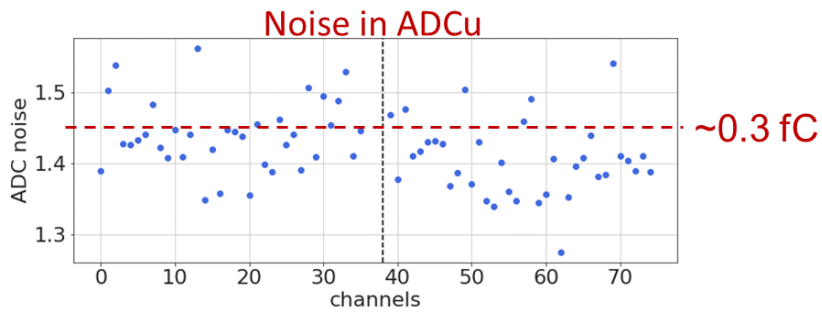
Performance

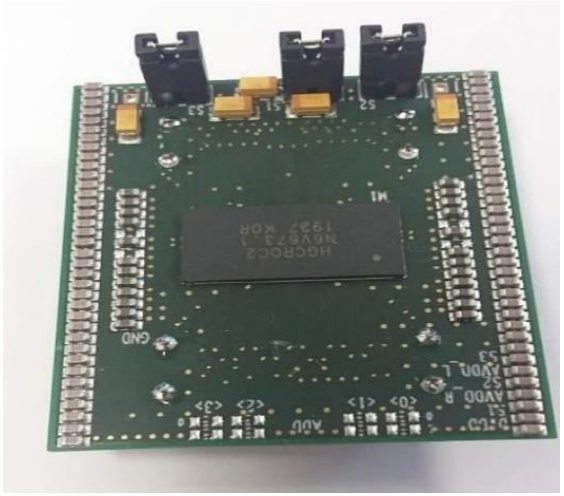


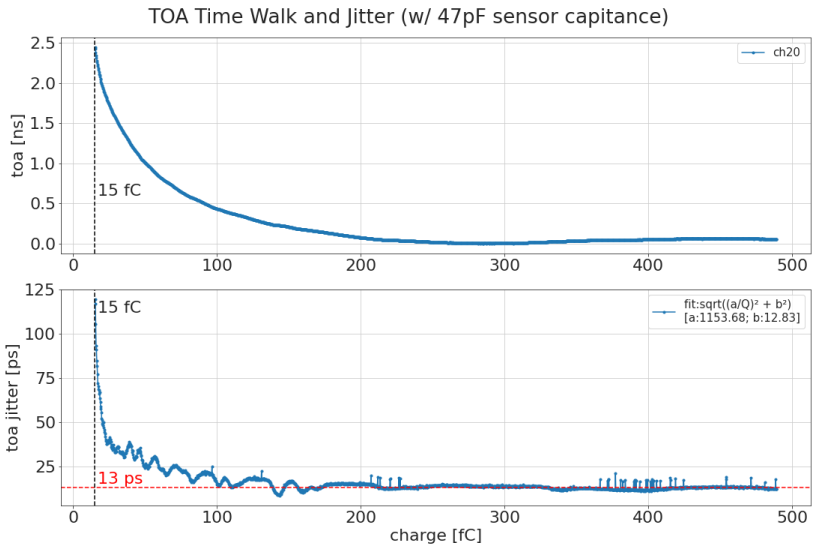






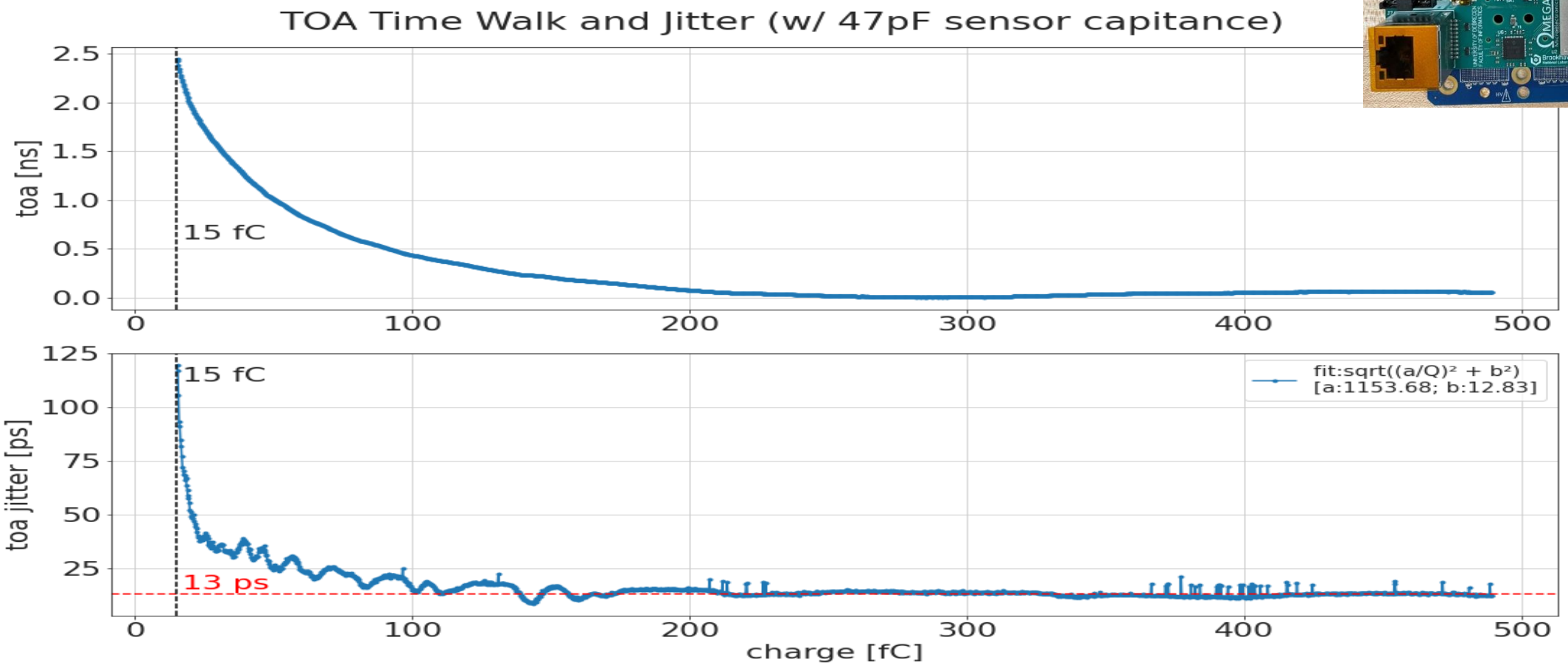






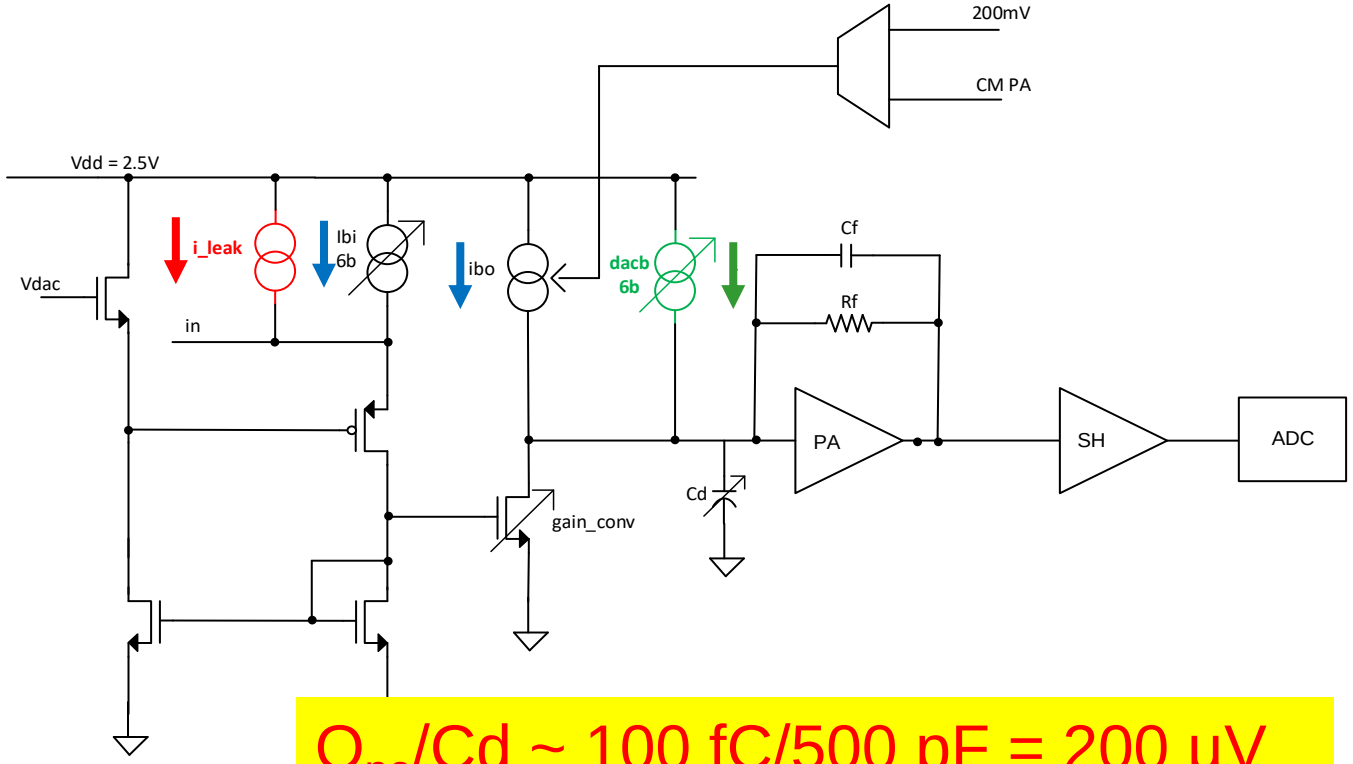
Zoom on timing

- ~2.5 ns time walk, 13 ps jitter for Q>100fC at Cd = 47 pF
- Fits also well MCPs for PID (ex HRPPD 1000 ch MCP)

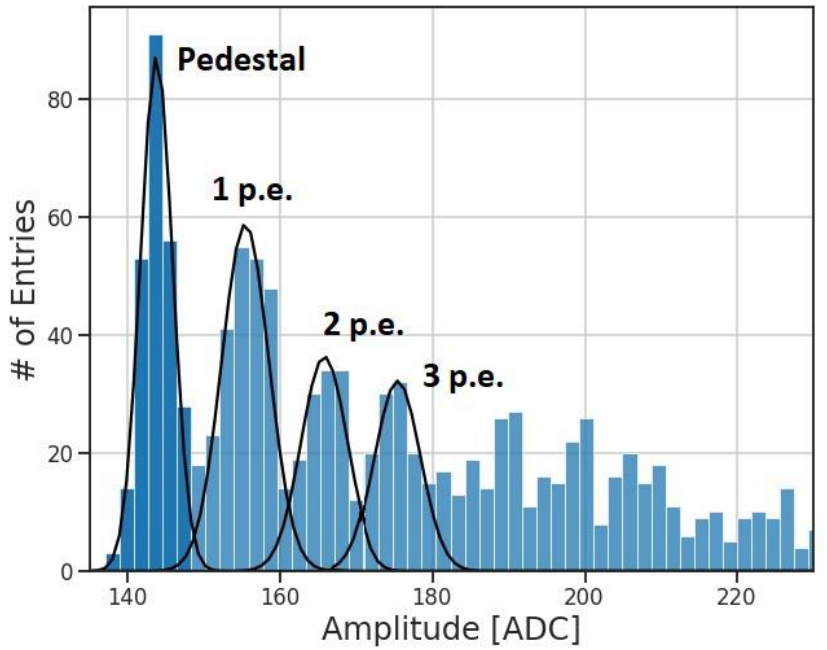


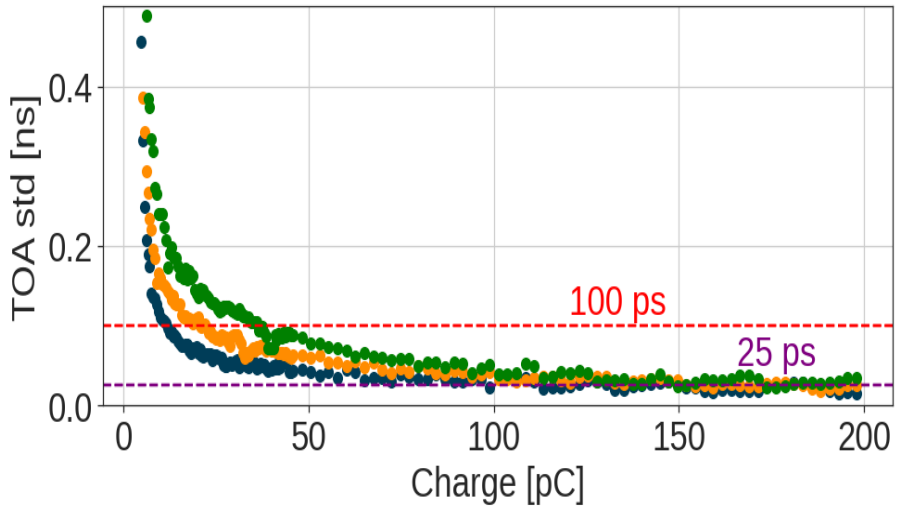
H2GCROC: SiPM version current conveyor

- **Current conveyor (Heidelberg design) to adapt to Si version**
- **Dynamic range : 50 fC – 300 pC**
- **2 typical gains**
  - Low gain (Physics mode): **44 fC/ADC gain, 50 fC noise (1.25 ADCu)**
  - High gain (Calibration mode): **10 fC/ADC gain, 20 fC noise (2 ADCu)**
- **Measurements in backup slides**



$Q_{pe}/Cd \sim 100\ fC/500\ pF = 200\ \mu V$

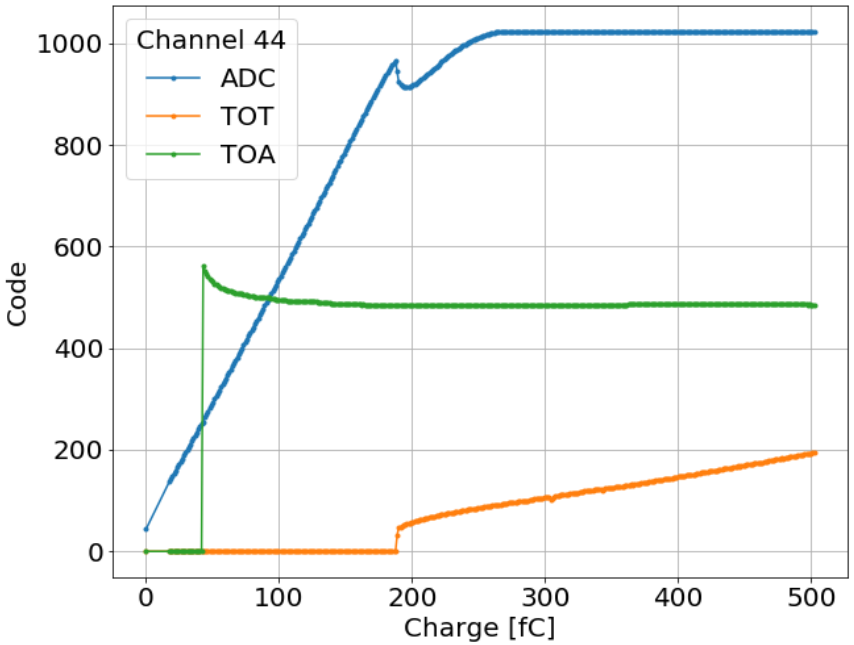


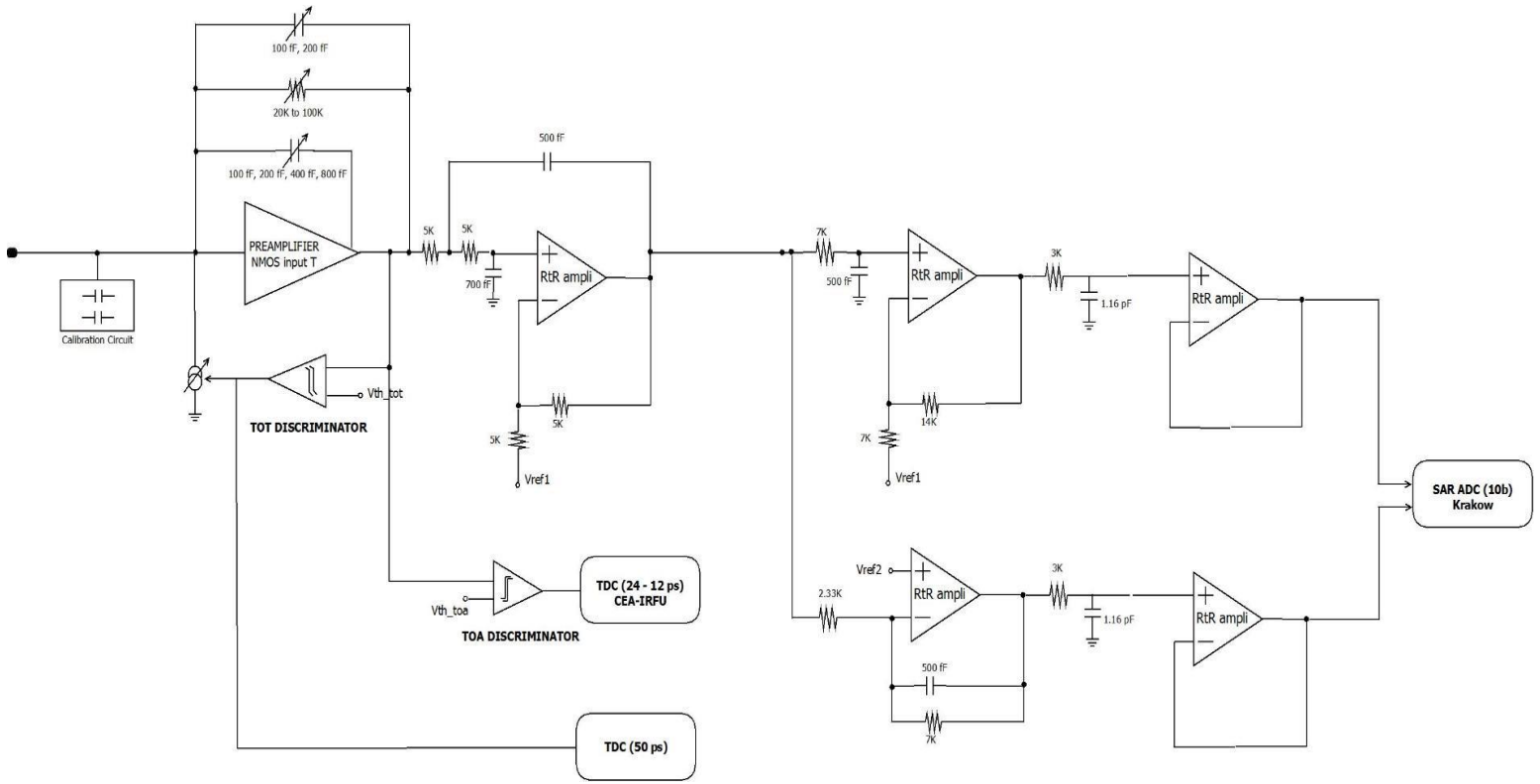


HGCROC : ADC and TOT

- ADC range 0 - 200 fC
- TOT range 200 fC - 10 pC
- Non-linear inter-region
- 200 ns dead time
- Not well adapted to SiPM version

=> go to dynamic gain switching

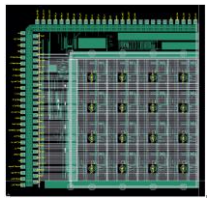


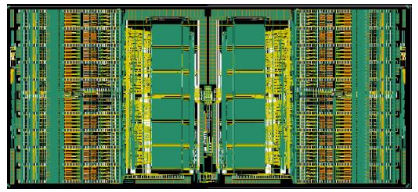


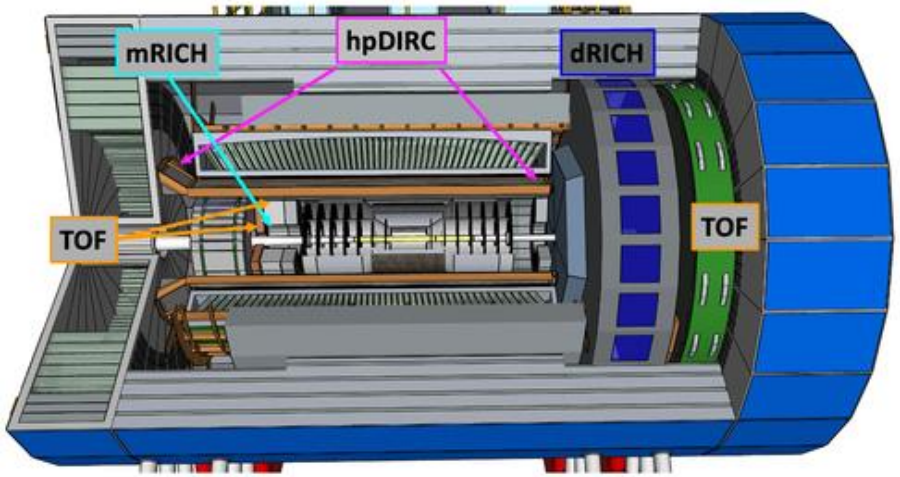
Chips for EIC : electron-ion collider at BNL

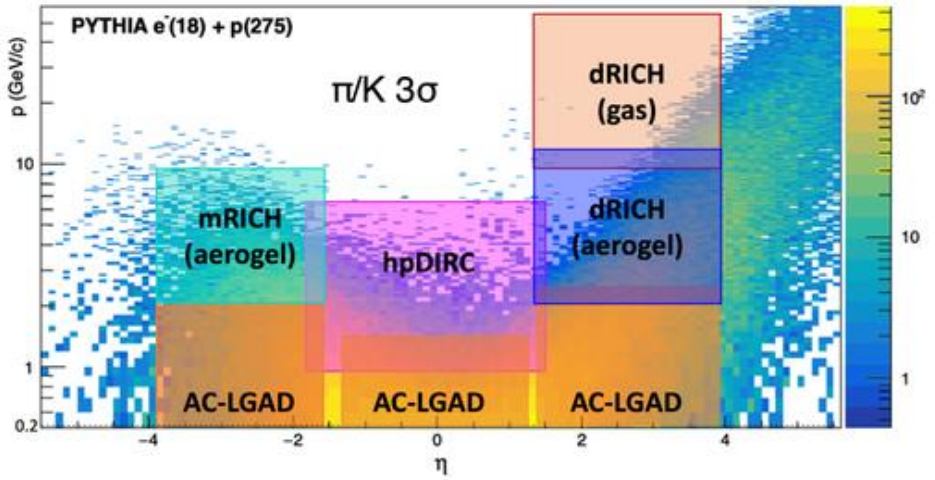
- PID and calorimeters
  - EICROC for AC-LGAD roman pots
  - H(2)GCROC for calorimeters
  - « Event driven » DAQ

Detector Group	Channels			
	MAPS	AC/DC-LGAD	SiPM/PMT	MPGD
Tracking	32 B			100k
Calorimeters	50M		67k	
Far Forward	300M	2.3M	500	
Far Backward		1.8M	700	
PID		3M-50M	600k	
TOTAL	32 B	7.1M-54M	670k	100k
ASIC	ITS-3	EICROC FCFD HPsOC ASROC FAST	Discrete/COTS HGCROC3 ALCOR-EIC	SALSA









CALOROC1 (Q3 2024)

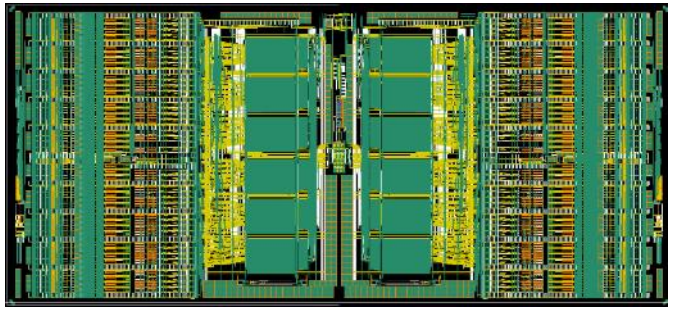
- SiPM readout calorimetry : CMS H2GCROC with EIC readout (200 MHz clock and fast commands)
  - SiPM from 500 pF to 2.5 nF (or 10 nF)
  - ~5-10 mW/channel

- 2 versions : conservative and exploratory
  - Conservative : uses H2GCROC (ADC, TOT) as it is and replaces the backend
  - Exploratory : new analog part (dynamic gain switching).
  - Pin to pin compatible
  - Backend « à la HKROC » : auto-triggered, zero-suppressed
  - 40 MHz internal clocking (ADC, TDCs)

- Channel number tbd : 32 (HKROC) or 64 (HGCROC)

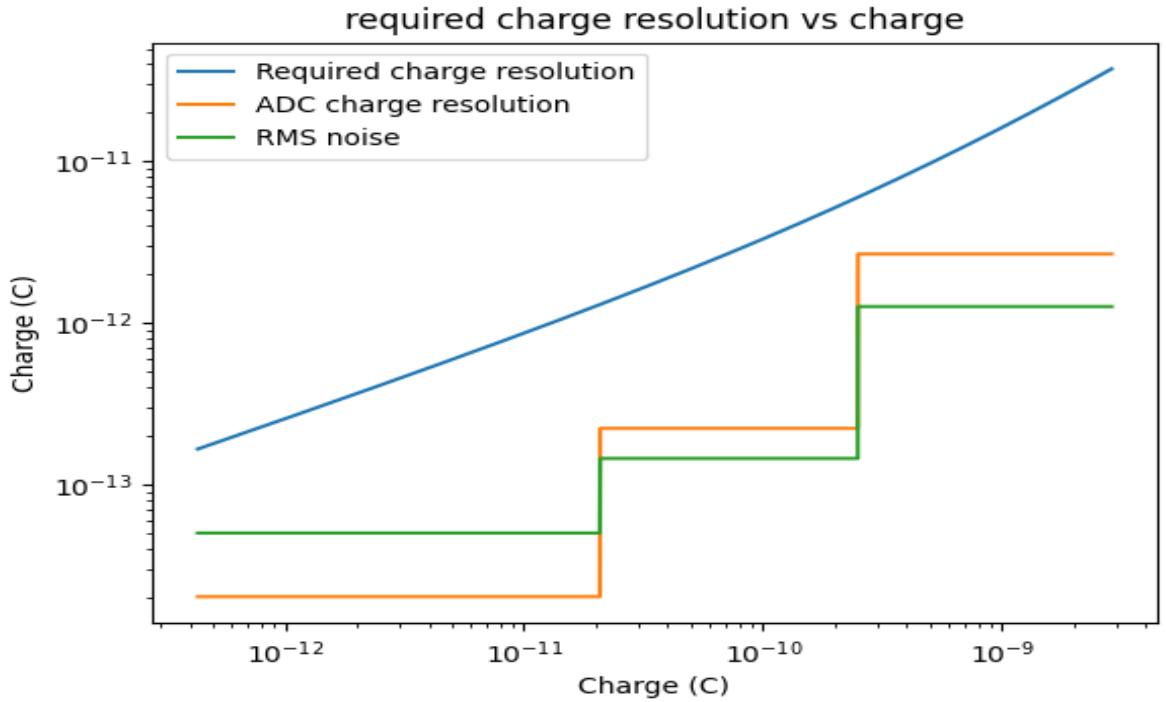
- should also fit DRD6 Si / SiPM calorimeters

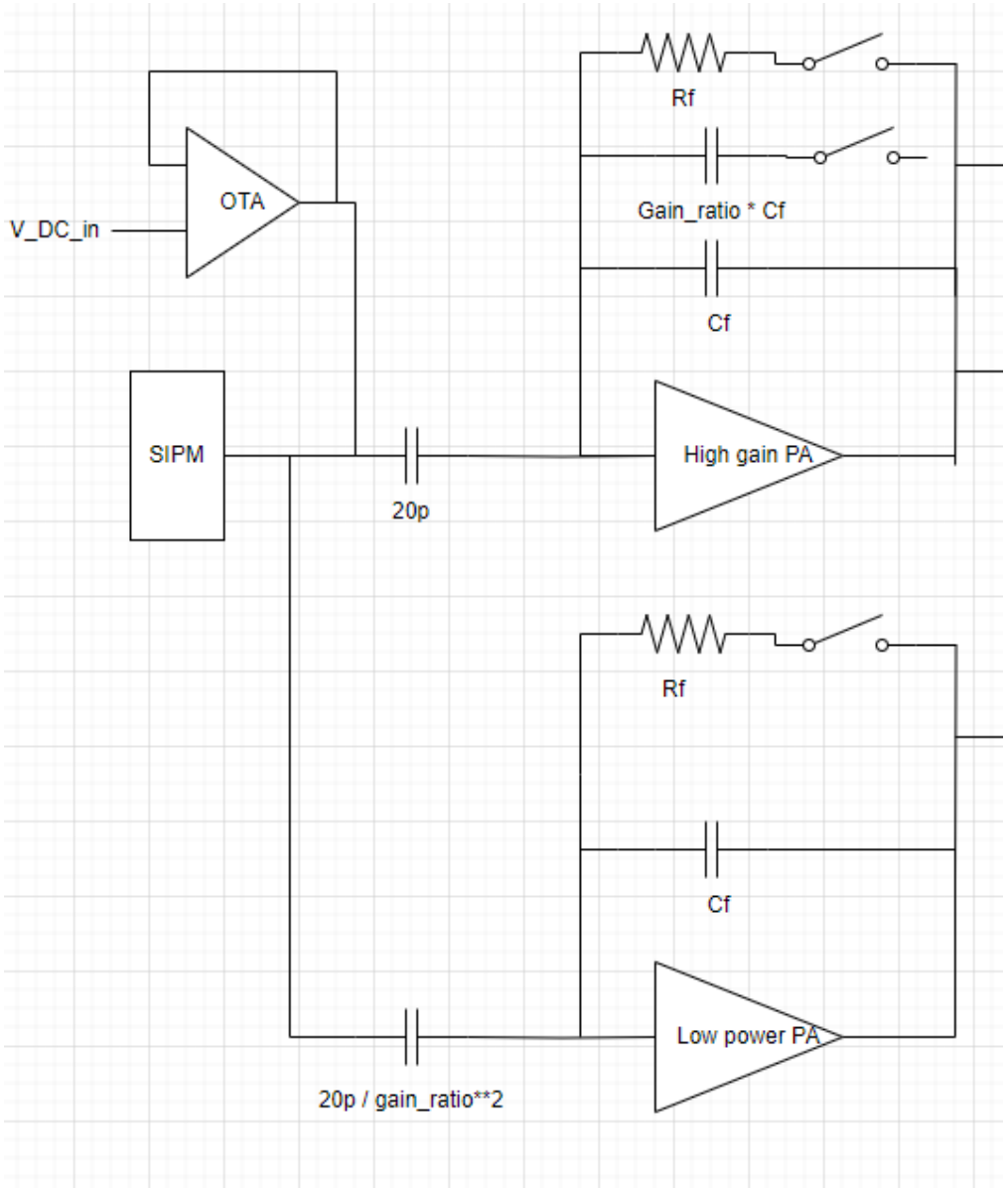
HKROC



CALOROC1A (also 2024)

- Variant with new analog part
- Dynamic gain switching
- Study of current conveyor and voltage amplifiers « à la spiroc »
- Study low power ADCs (clock gating)





AGH in DRD6 WP4

Marek Idzik for AGH-UST

Objectives

- Main goal
  - **Cooperation with WP4 partners in designing the best possible front-end ASIC(s) for applications in calorimetry**
- Additional goal – depending on manpower resources
  - **Improvement of already developed front-end ASICs for calorimetry**

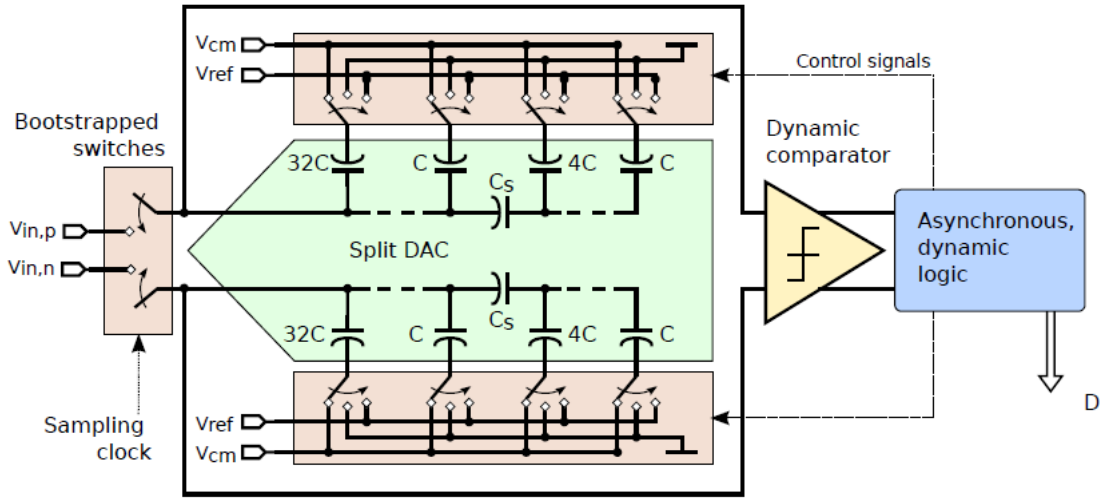
Cooperation with WP4 partners

- Developing key functional blocks and integrating it together with partners into complete front-end ASIC(s)
  - Blocks: fast ADCs of different resolutions (10-12 bits), fully differential amplifiers, serializers&transmitters, …
  - Common request – ultra-low power to achieve ~mW per complete front-end channel
  - Technologies: presently CMOS 130/65 nm, later on CMOS28nm

Cooperation with WP4 partners
Example work on extension of 10-bit ADC

Our existing 10-bit ADC in CMOS 130nm

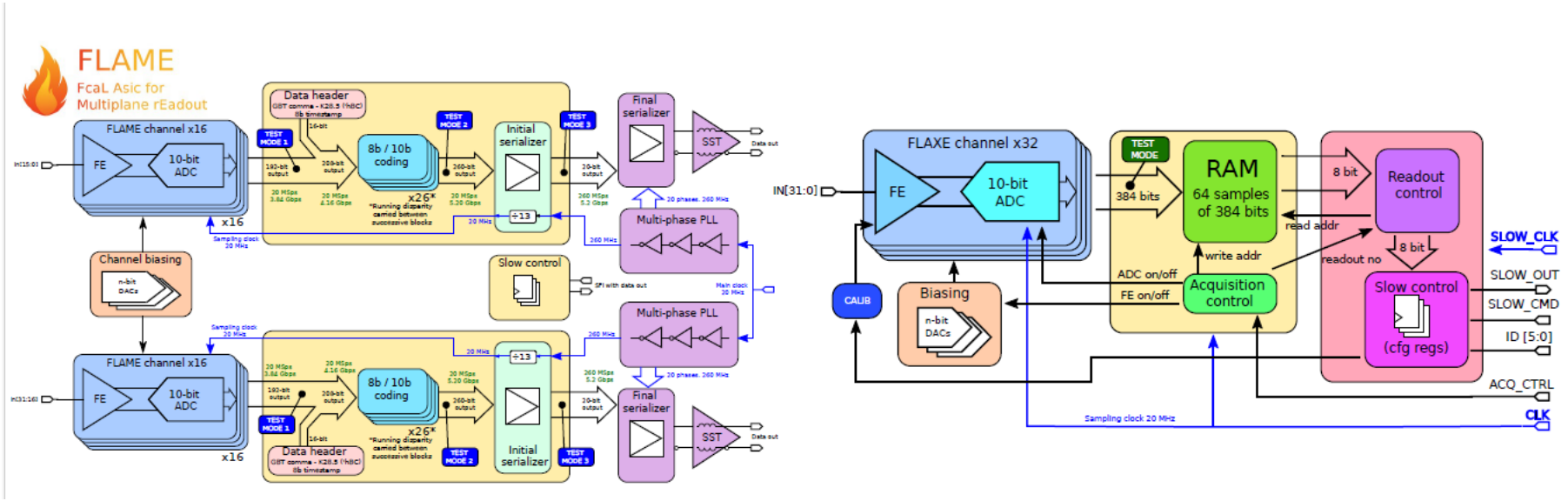
- power 680uW@40MSps
- works up to 50MSps



- To decrease power consumption even further, we are introducing additional comparison with threshold, in order to make full conversion only for signal (and not for noise)
  - –If Signal (>Vth) - 11 comparisons are done instead of 10
  - –If NO signal – 2 comparisons are done and ADC is reset
- The result is that ADC is slightly slower, but
  - –Estimated power for low occupancy ~ one third of the current one
- Work in progress...

Improvement of existing front-end ASICs for calorimetry

- Works on variations of FLAME/FLAXE ASICs

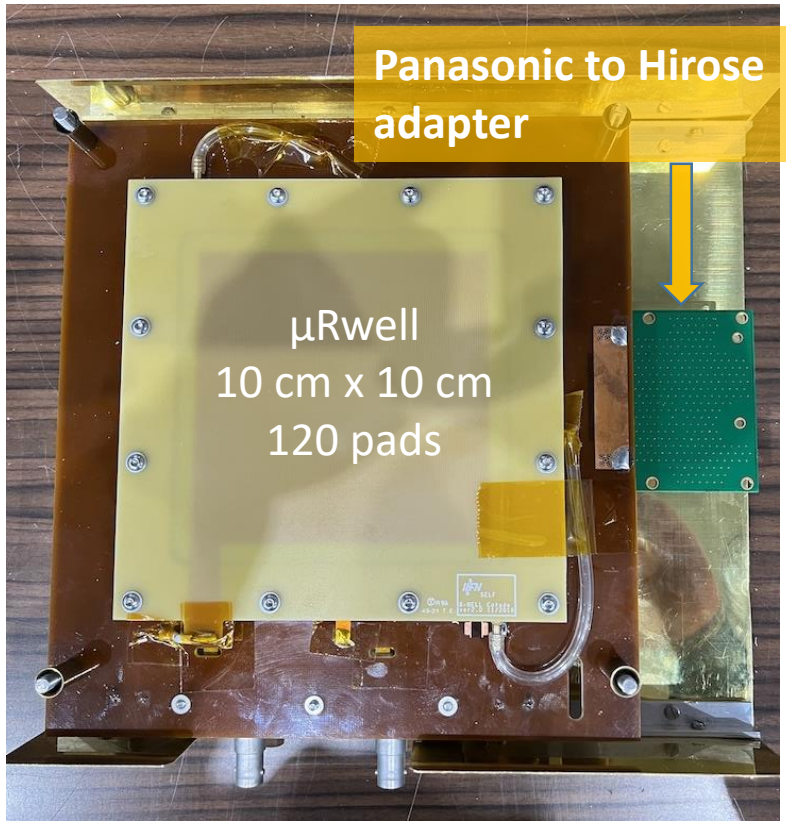


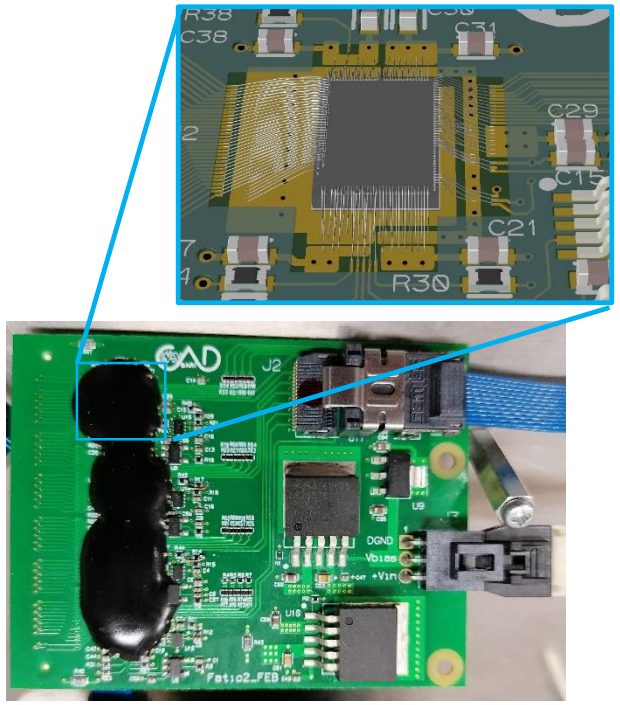
•FLAME/FLAXE are a 32-channel chips CMOS 130nm comprising analog front-end and fast ultra-low power 10-bit ADC in each channel. FLAME has two high speed (5.2Gb/s) serialisers&transmitters, while FLAXE is intended for low trigger rate.

Micro-RWELL Frontend Electronic

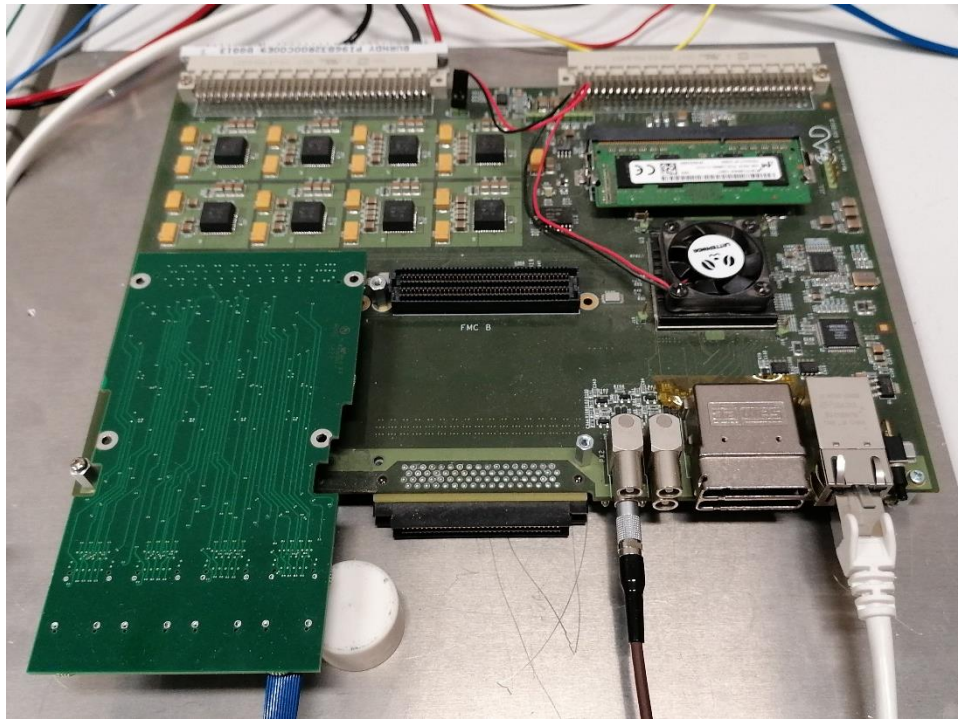
Giuseppe de Robertis, Luigi Longo
for the micro-RWELL LHCb group
Bari, LNF, Roma2

Electronic chain





Front End Board
- 4 x FATIC2
- 128 channels

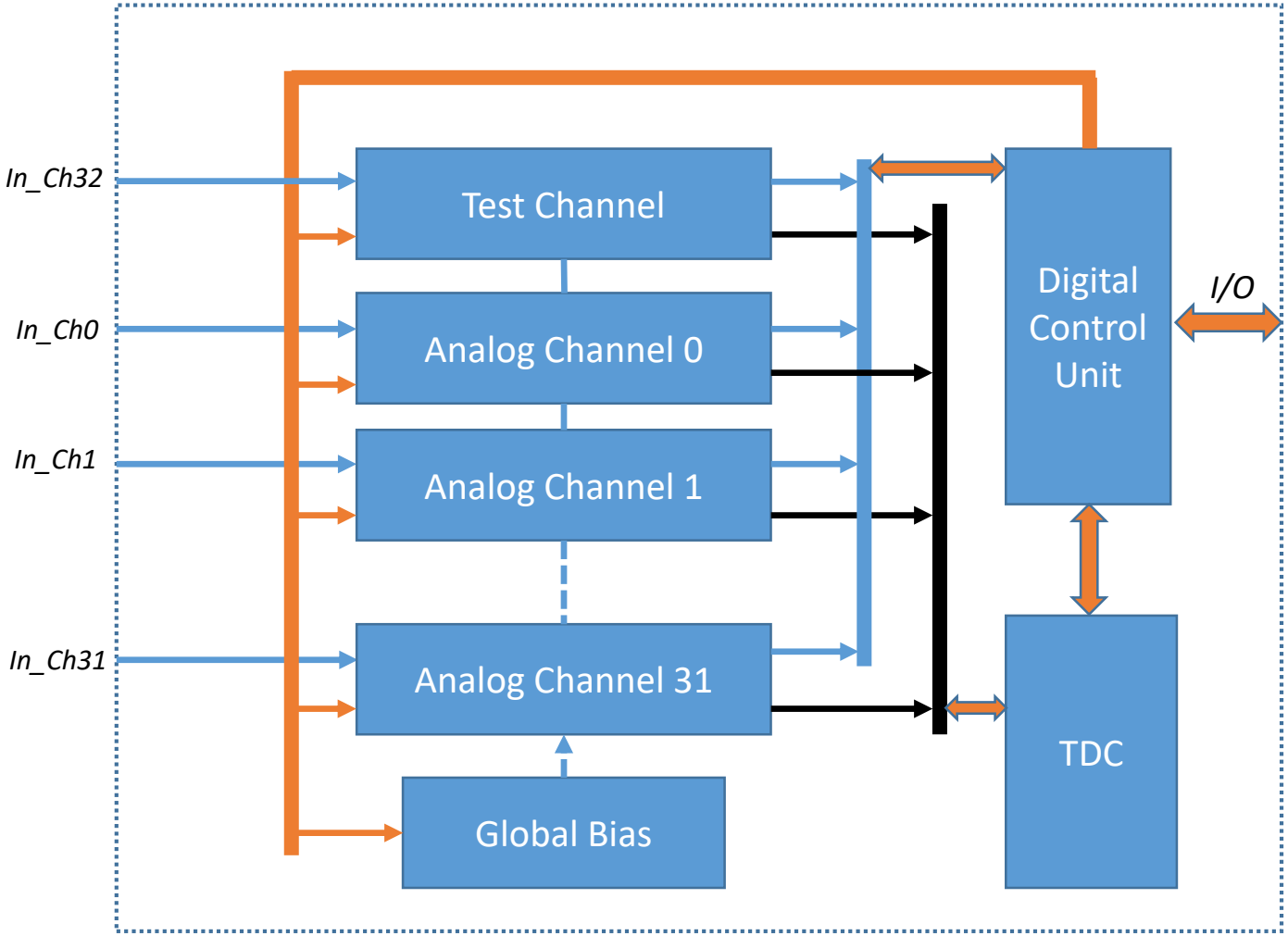


MOSAIC DAQ board + FMC adapter
- Up to 4 FEB

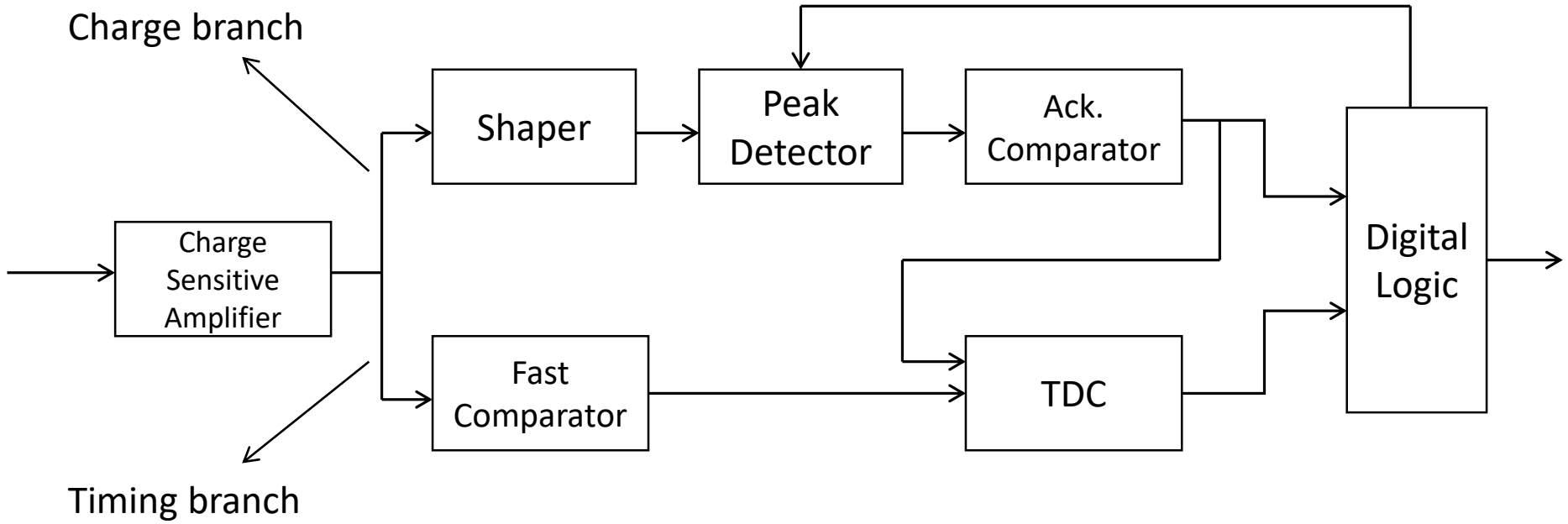
FATIC2 architecture

Features:

- Technology: TSMC 130 nm
- 32 channels
  - Programmable polarity, gain and peaking time
  - Charge and time measurement
  - Time measurement using 100 ps TDC
- Calibration, Bias and Monitoring
  - ➢ Charge injection calibration
  - ➢ Programmable biases (currents and voltages)
  - ➢ Monitoring ADC (12 bit SAR)
- 320 Mbps serial link, LpGBT compatible
- Power supply 1.2 V
- Radiation hardness: up to 100 Mrad



Channel block diagram



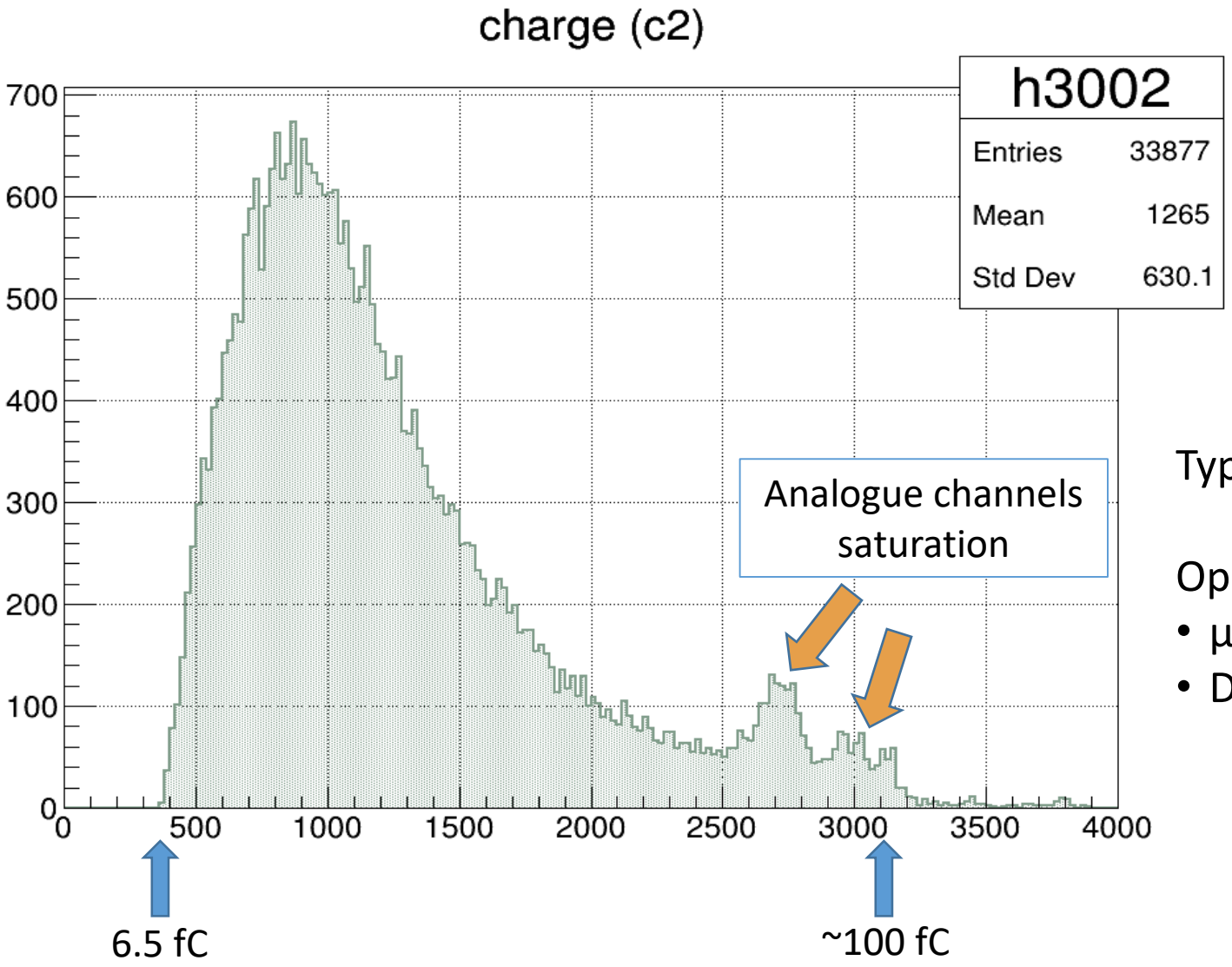
Preamplifier features:
- CSA operation mode
- Input signal polarity: positive & negative
- Recovery time: adjustable

CSA mode:
- Programmable Gain: 10 mV/fC ÷ 50 mV/fC
- Peaking time: 25 ns, 50 ns, 75 ns, 100 ns

Timing branch:
- ✓ Measures the arrival time of the input signal
- ✓ Time jitter: 400 ps @ 1 fC & 15 pF (Fast Timing MPGD)

Charge branch:
- ✓ Acknowledgment of the input signal
- ✓ Charge measurement: dynamic range > 50 fC, programmable charge resolution

Charge distribution



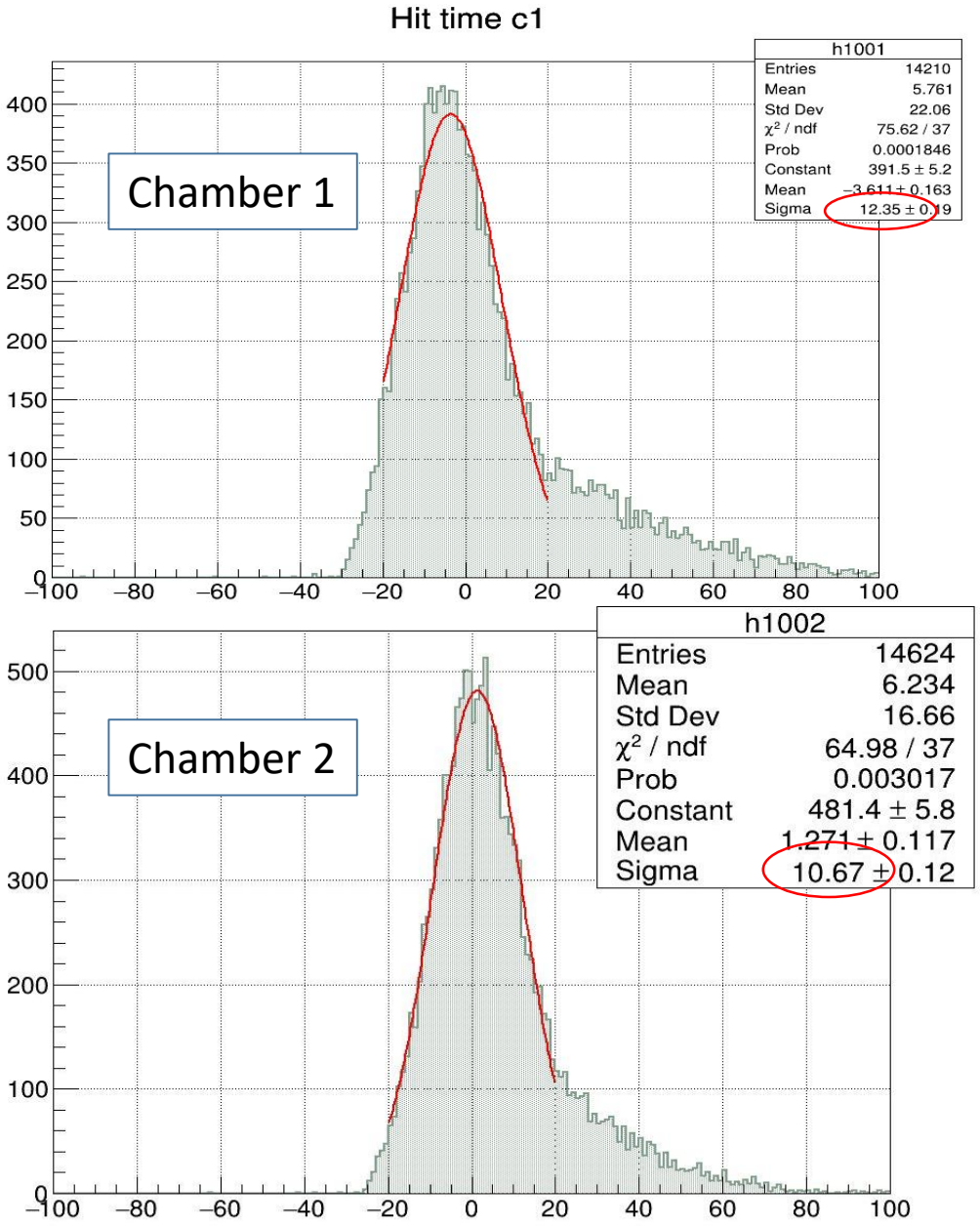
Cosmic ray tests

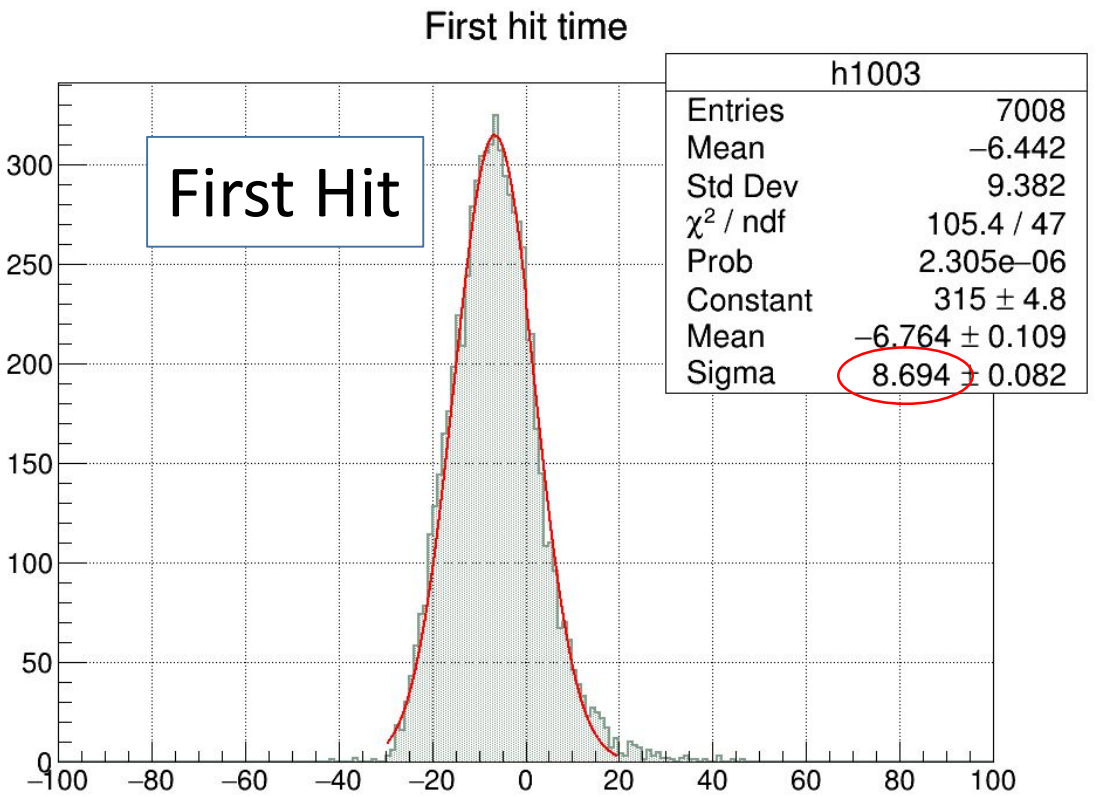
Typical run lenght: 24 – 48 hours

Operative condition:

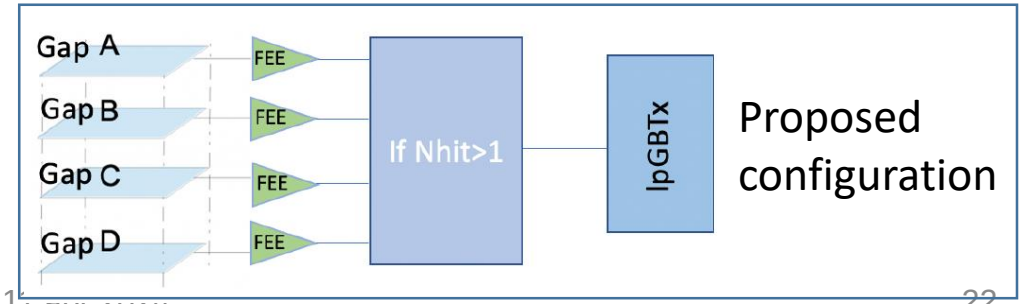
- µRwell gain voltage 640 V
- Discriminator thresholds 6.5 fC / 6 fC

Time distribution – First Hit





- Time measurements are still affected by trigger jitter
- The aim is to gain a 1.4 factor moving from 2 to 4 chambers



Proposed configuration

FATIC3 & FATIC4 ASIC

FATIC3: Mainly a bug fixing plus some features integration

- Channel FSM bug fix
- Trigger data filter moved from FPGA to ASIC
- Increase of transmission speed from 320 to 640 Mbps
- Integrated monitoring ADC and voltage reference IP
- Cut down of power consumption from 500 mW to < 150 mW
- 100 chip production submitted in January 2024 (20 for HCAL R&D)

FATIC4: Performance improvement

- Lower dead time, from ~2 us to ~100 ns
- More digital features to make the chip closer to LHCb needs

Submission foreseen for Q4 2024/Q1 2025

Specifications for dual readout [R. Santoro]

DEFINITION OF THE ASSEMBLY METHOD AND OF THE ASIC SPECIFICATIONS FOR A DUAL READ-OUT CALORIMETER PROTOTYPE

Milestone: MS35

Date: 28/02/2023

Main specifications	
Readout strategy	Charge integration
Number of channels	32 / 64
Sensitivity	0.5 p.e. (@ 2 * 10^5 SiPM gain)
Dynamic Range	0 – 320 pC (i.e. 10000 p.e. @ 2 * 10^5 SiPM Gain)
Timing resolution	< 50 ps rms (single p.e.)
Power consumption	< 500 mW

Main specifications	
Readout strategy	Waveform sampling
Number of channels	32 / 64
Sampling frequency (GHz)	5 - 10
Input Bandwidth (GHz)	> 1
Buffer length (samples)	> 4k
Feature extraction	i.e. total charge, ToA, ToT, current-peak time …
Full frame readout	Internal / external trigger (one of the two or both)

DRD6 WP4 : Electronics and DAQ

- Goals
  - Produce ASICs and DAQ for prototypes (sizeable quantities…)
  - Avoid parallel developments but encourage communications between groups
  - Optimize commonalities (readout format, interfaces, inter-operability)
  - Organize common ASIC fabrication (share engineering run to minimize costs)

- Close communication with other DRDs
  - DRD3 : MAPS for digital calorimetry
  - DRD4 : photodetectors
  - DRD7 : electronics (ADCs, TDCs…)

- Strong interplay detector/electronics
  - Noise, granularity, timing, power dissipation, data bandwidth….
  - Detector R&D vs/with Electronics R&D

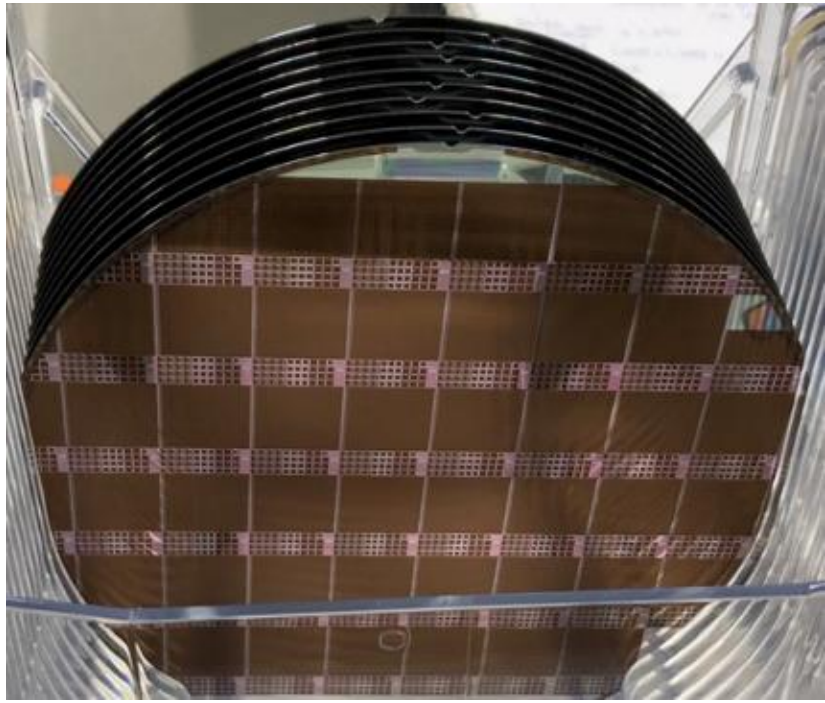
Next steps

- Go over the electronics and DAQ requirements/wishes from the different participants
  - See what exists and what needs R&D
  - Need essentially sensor capacitance and dynamic range (in fC)
  - See what's covered internally and what can be provided by DRD6 developments

- Gather the community of « calorimeter electronics developers »
  - Share expertise and experimental results
  - Address specificities of calorimetry
  - Share fabrication (engineering) runs to equip prototypes

conclusion

- Importance of joint optimization detector/readout electronics



- Trend to reduce power and data volume
  - Pileup will be less of an issue, better granularity will be appreciated !
  - Low occupancy, auto-trigger, data-driven readout
  - Low power ADCs and TDCs (DRD7 with AGH&CEA)
- Picosecond Timing important R&D area
  - PID and/or calorimetry, several new detectors appearing : need R/O
- Next chips at OMEGA will target EIC, DRD1-4-6-7
  - Calorimetry and timing : CALOROC1 and 1A : Q3 2024
  - Further R&D needed to bring power down to ~1 mW/ch (LAr)
- Technology choice to be addressed in coordination with other design groups
  - Cost sharing for engineering runs

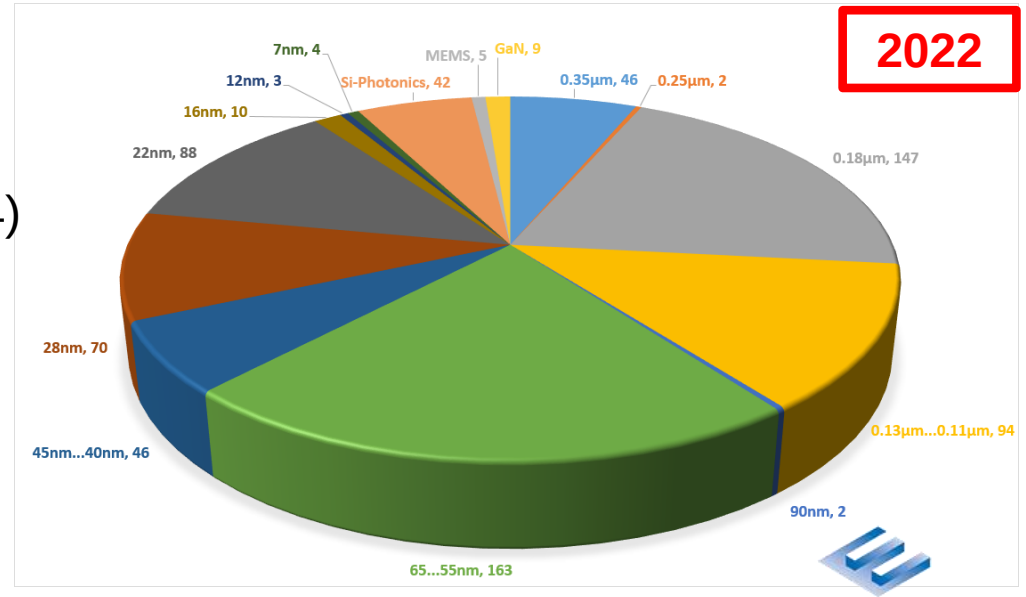
backup

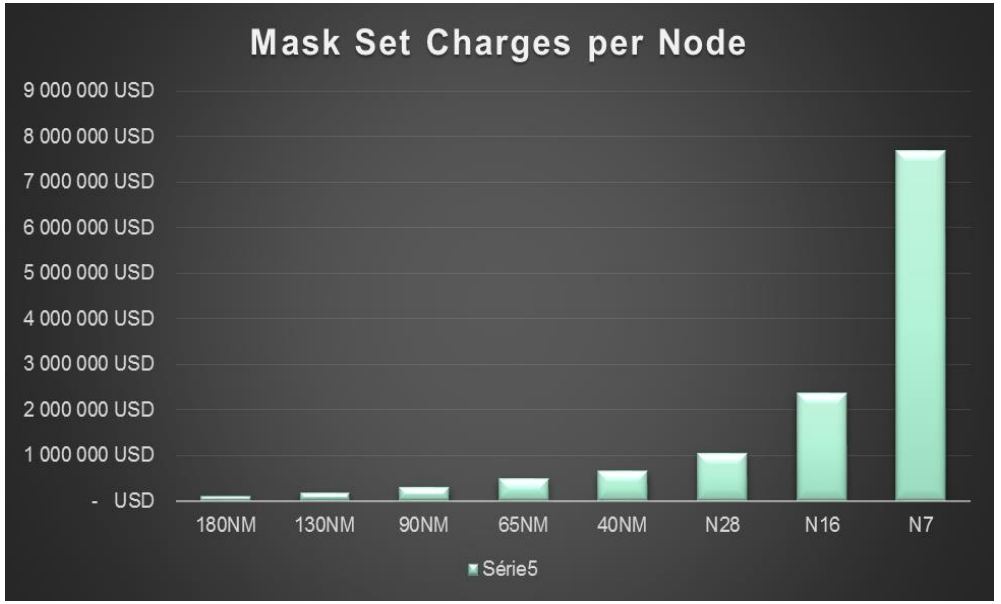
Technology choice for mixed signal ASICs

- TSMC 130nm : mixed signal, cheap
  - Very mature technology with good analog performance
  - 2.5 k€/mm² MPW, 300-350 k€/engineering run (20 wafers C4)
  - Perenity ?

- TSMC 65 nm : mixed signal, main stream
  - ~2-3 times lower power in digital, similar in the analog (compared to 130n)
  - 5 k€/mm², 700-800 k€/ engineering run

- TSMC 28 nm : digital oriented
  - High density integration (pixels)
  - High performance, lower power digital, similar in the analog
  - 10 k€/mm², 1-1.5 M€/ eng run





Trends for calorimeter readout

- On-detector embedded electronics, low-power multi-channel ASICs
  - CALICE SKI/SPI/HARDROC, FLAME, CMS HGCROC, FCC LAr, FATIC…
  - Challenges : #channels, low power, digital noise, data reduction

- Off-detector electronics : fiber/crystal readout
  - Wavefrom samplers : DRS, Nalu AARD, LHCb spider…
  - Challenges : low power, data reduction

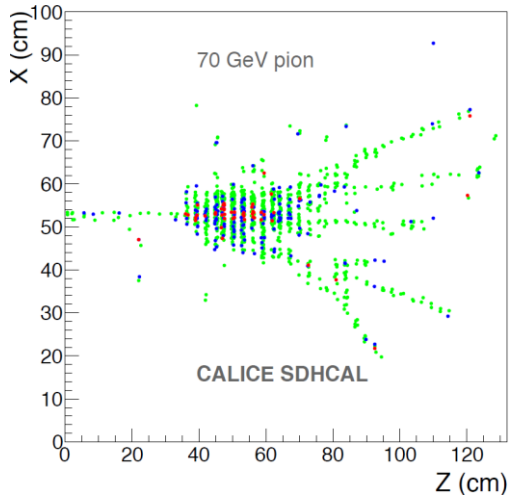
- Digital calorimetry : MAPs, RPCs…
  - DECAL, ALICE FOCAL, CALICE SDHCAL
  - MAPS for em CAL : eg ALPIDE ASIC for FOCAL, DECAL…
  - Challenges : #channels, low power, data reduction

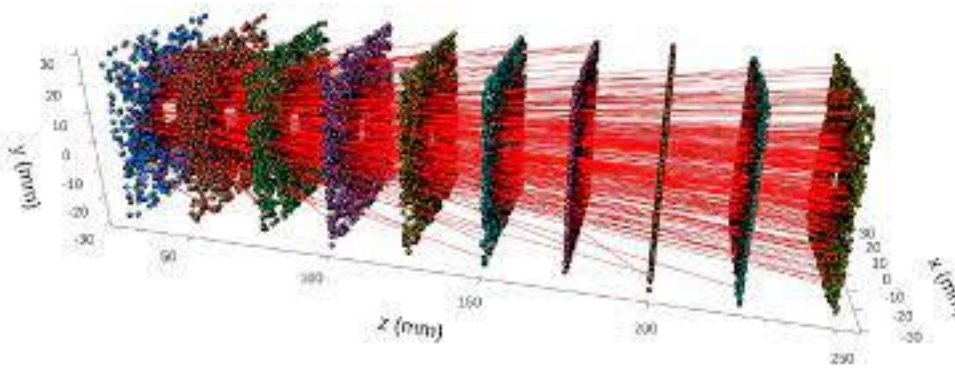
Digital calorimetry

- Hadronic : e.g. CALICE RPCs or µmegas
  - ~1 cm² pixels, low occupancy, ~1 mW/cm² (unpulsed)
  - Performance improvement with semi-digital architecture
  - Timing capability can be added

- Electromagnetic : e.g. DECAL, ALICE FOCAL…
  - Based on ALPIDE : (30µm)² pixels, high occupancy, ~ few 100 mW/cm², slow
  - To be compared with embedded electronics ~10 mW/cm²
  - Most power in digital processing => would benefit a lot from ≤ 28 nm node
  - Semi-digital and/or larger pixels couldl be an interesting study

- Upcoming R&D
  - Power reduction, dead area minimization
  - Coping with high occupancy, managing data bandwidth



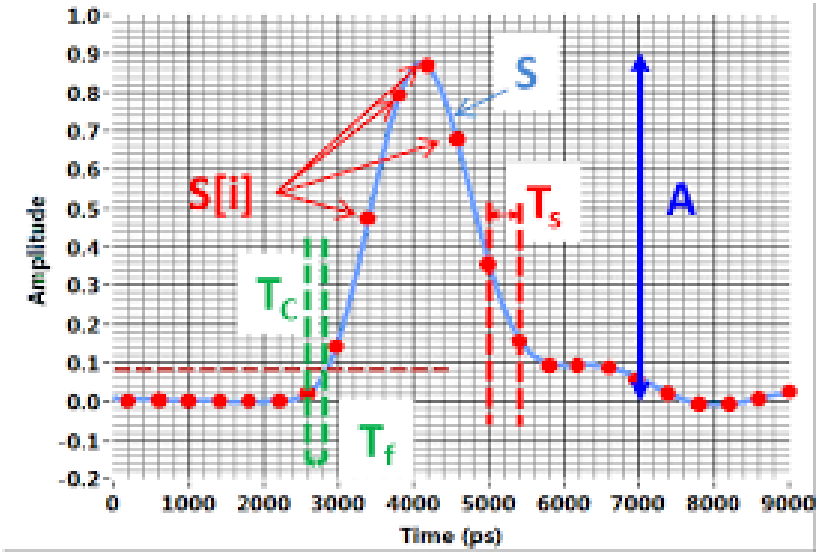


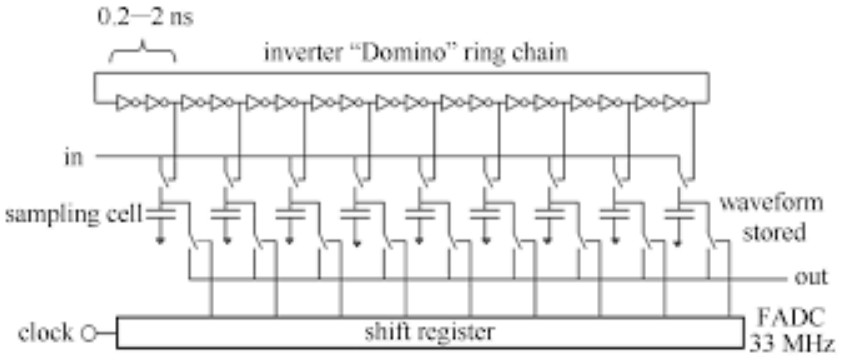
Waveform sampling

- Switched capacitor arrays (DRS4, Nalu, SPIDER…)
  - Pulse shape analysis
  - High accurcay timing, digital CFD
  - Sizeable power to provide GHz BW on large capacitance
  - large data volume

- Often used in off-detector electronics
  - Space and cooling available
  - Small/medium size detector readout and/or characterization
  - See LHCb calorimeter upgrade

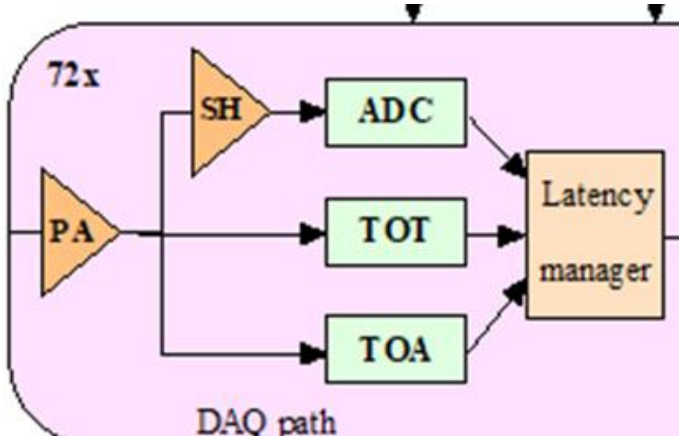
- Upcoming R&D
  - Power reduction, Front-end integration
  - Data bandwitdth
  - Time walk correction, potentially best for ps accuracy



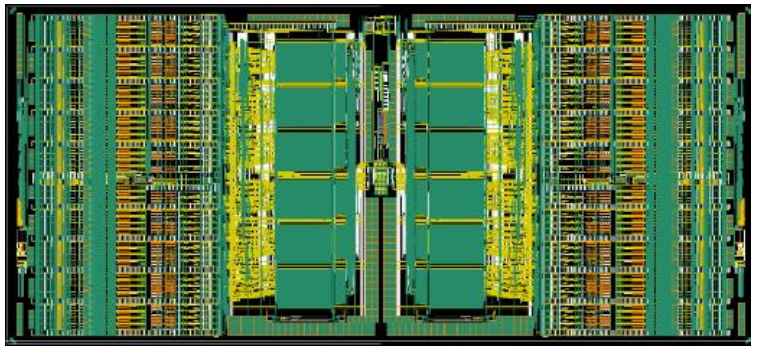


Embedded ASICs

- Pioneered with CALICE R&D (SKIROC, SPIROC..)



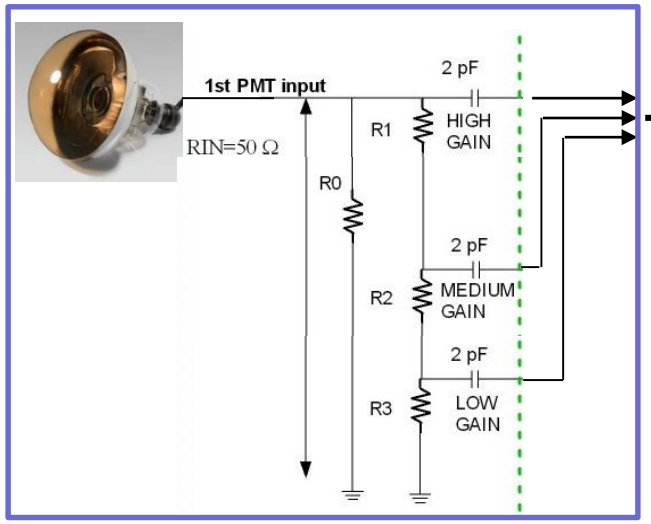
- Multi-channel charge/time readout
  - Fast preamp
    - Full dynamic range. Possible extension with ToT
  - Fast path for time measurement (ToA)
    - High speed discriminator and TDC
    - Time walk correction with ADC (or ToT)
  - Slow path for charge measurement
    - ~10 bit ADC ~40 MHz
  - Low power for on-detector implementation (~10 mW/ch) e.g. CMS HGCAL

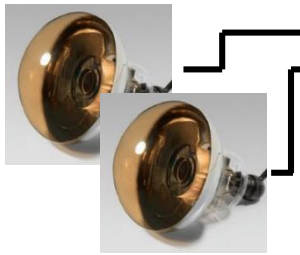


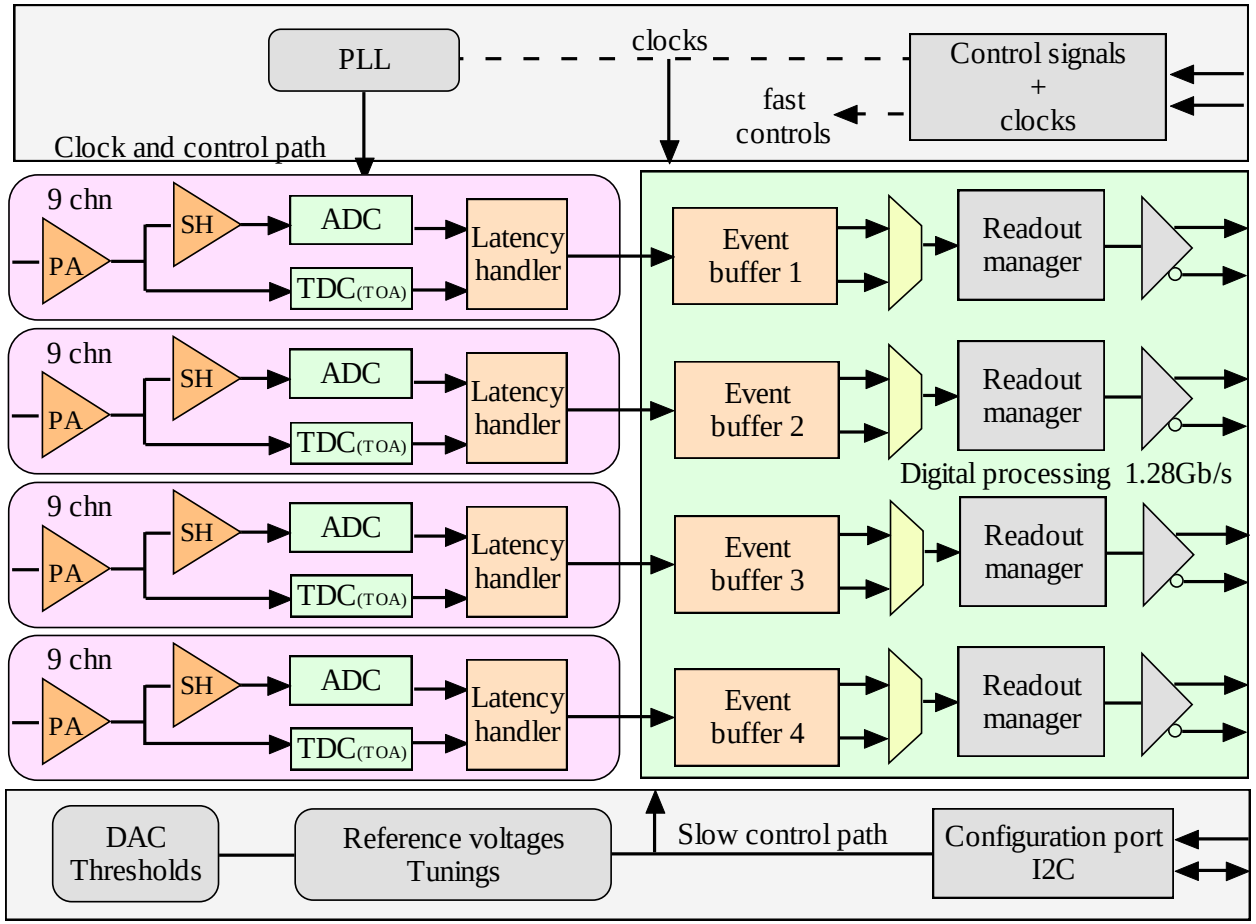
- Upcoming R&D
  - Power reduction,
  - Auto-trigger, Data-driven readout

HKROC main features

- HKROC is 36 channels: 12 PMTs with High, Medium and Low gain
  - Or 36 PMTs with one gain



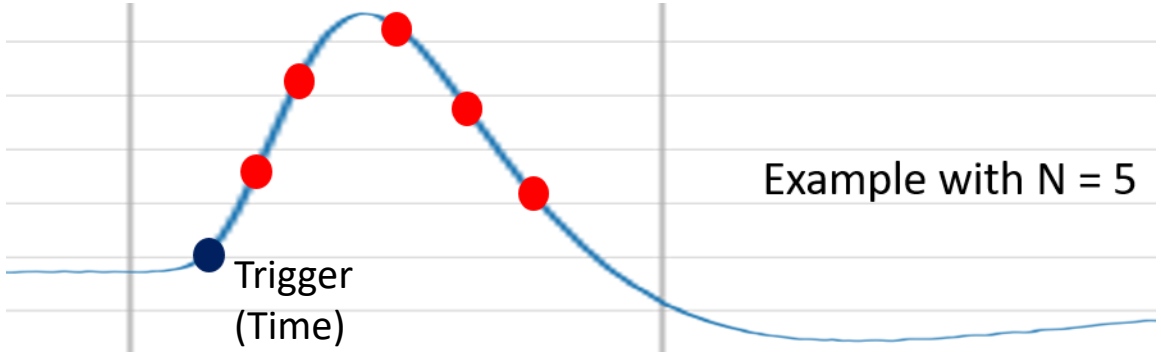




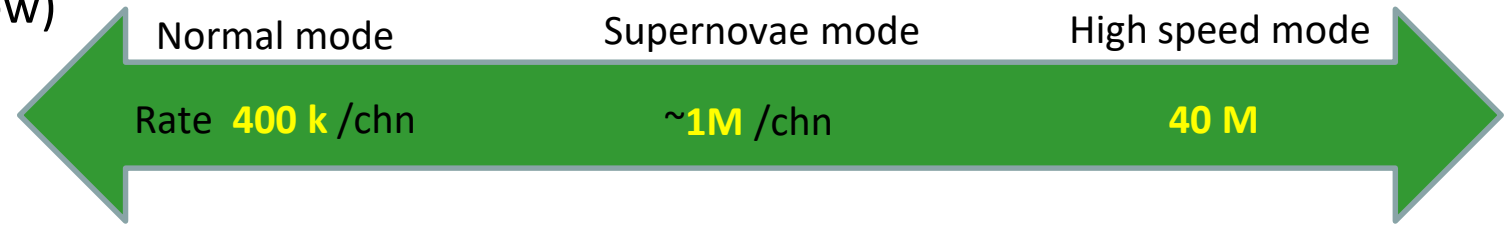
- ASIC in TSMC 130 nm node
- Low power: 10 mW per channel
- Large charge measurement with 3 gains (up to 2500 pC)
- Integrated timing measurements (25 ps binning)
- Readout with high speed links (1,28 Gb/s)
- HKROC is a waveform digitizer with auto-trigger

HKROC: waveform digitizer with auto-trigger

- HKROC is waveform digitizer working @ 40 MHz
  - Number of charge sampling points from 1 to 7
  - Fast channel for precise timing (25 ps binning)
  - Charge reconstruction algorithm in FPGA
    - 5% resources of a modern XILINX FPGA



- When using 3 gains / PMT (high, medium, low)
  - Hit rate capability up to 400 kHz / PMT
  - Increased up to 1 MHz by focusing on high gain
    - Dynamic selectable by the user
  - Average values only limited by readout speed



- Measurements in backup slides

HKROC can accept consecutive events (separated by ~30 ns)

Internal HKROC memory writing is without dead time

Readout speed is only limited by serial link bandwidth (average values above)