Preparation of Calice DAQ2 for test beams

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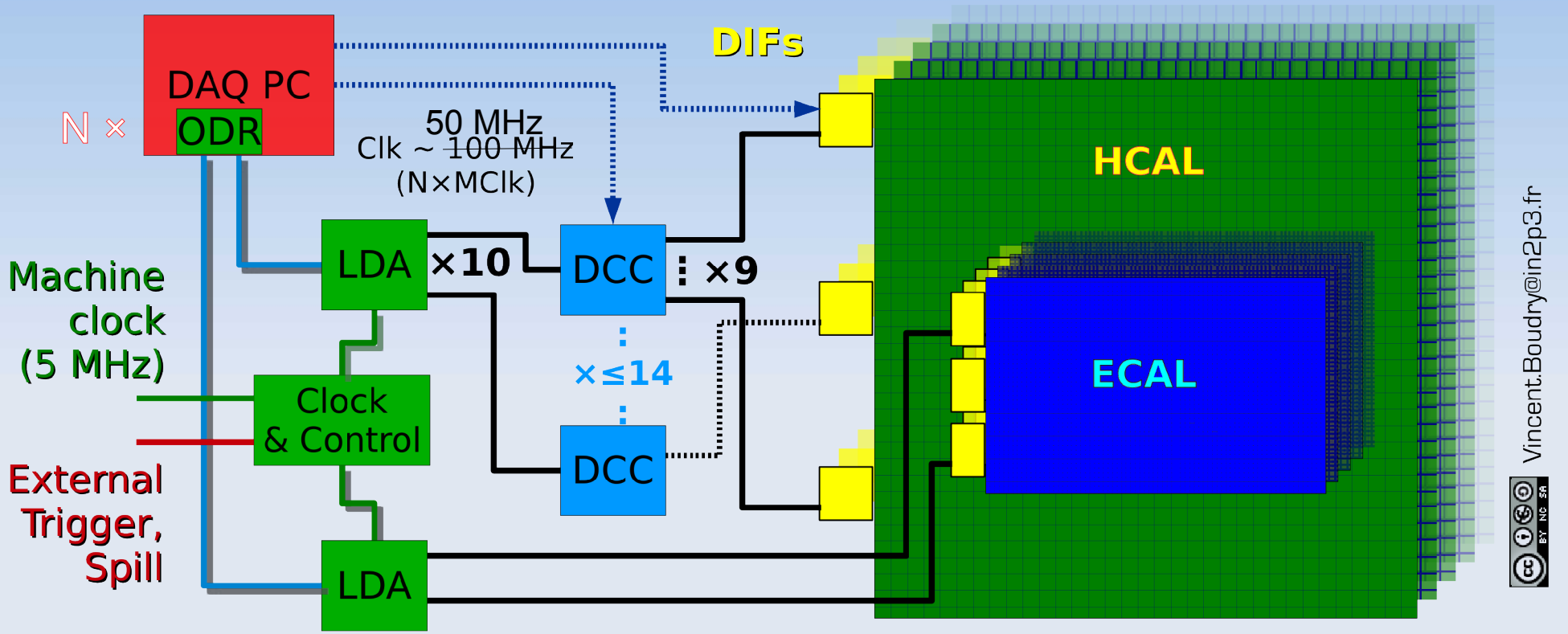
Calice collaboration meeting
CERN
20/05/2011

CALICE DAQ2 scheme



LDA-DIF on HDMI (Config, Control, Data, Clock, Trig, Busy, Sync)

Clock, Trig, Busy & Sync on HDMI (compatible LDA-DIF)

Optique (alt. Cable) GigE

Debug USB

External Trigger

ODR = Off Detector Receiver
LDA = Link Data Agregator

DCC = Data Concentrator Card
DIF = Detetcor InterFace

CCC = Clock & Control Card

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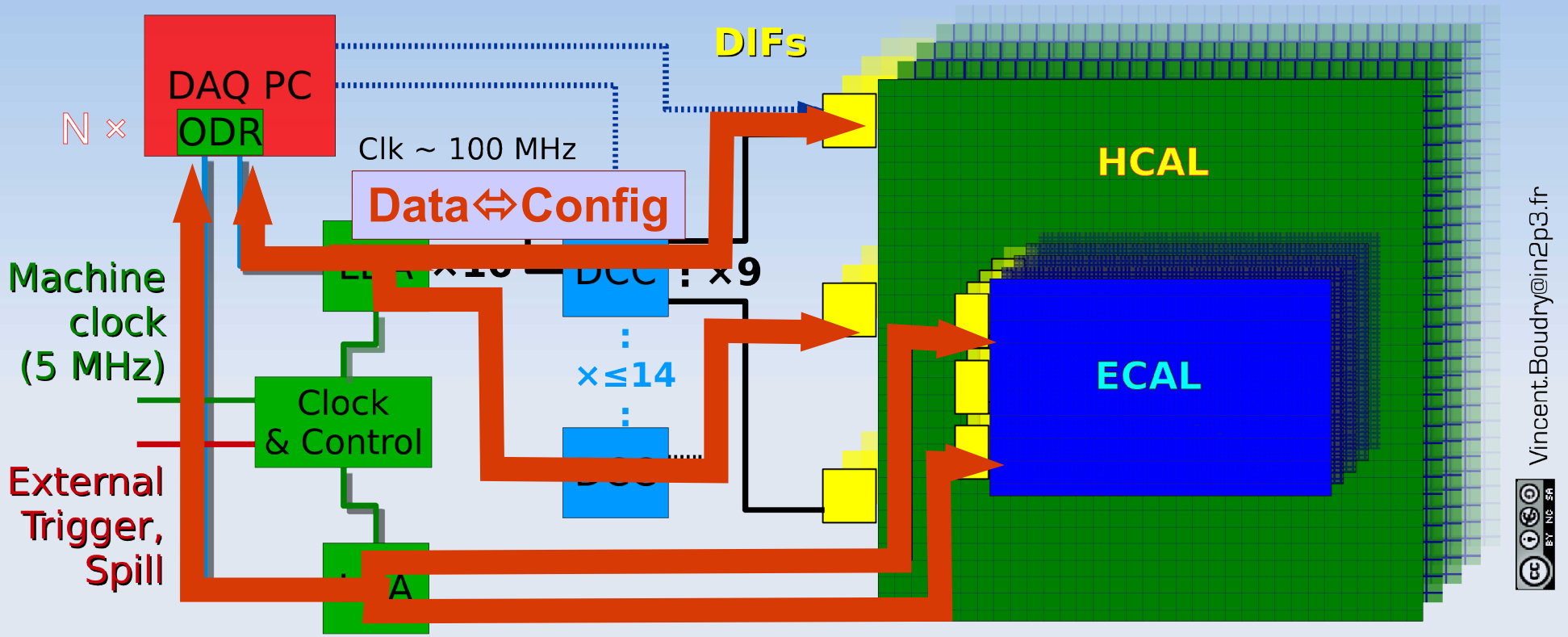

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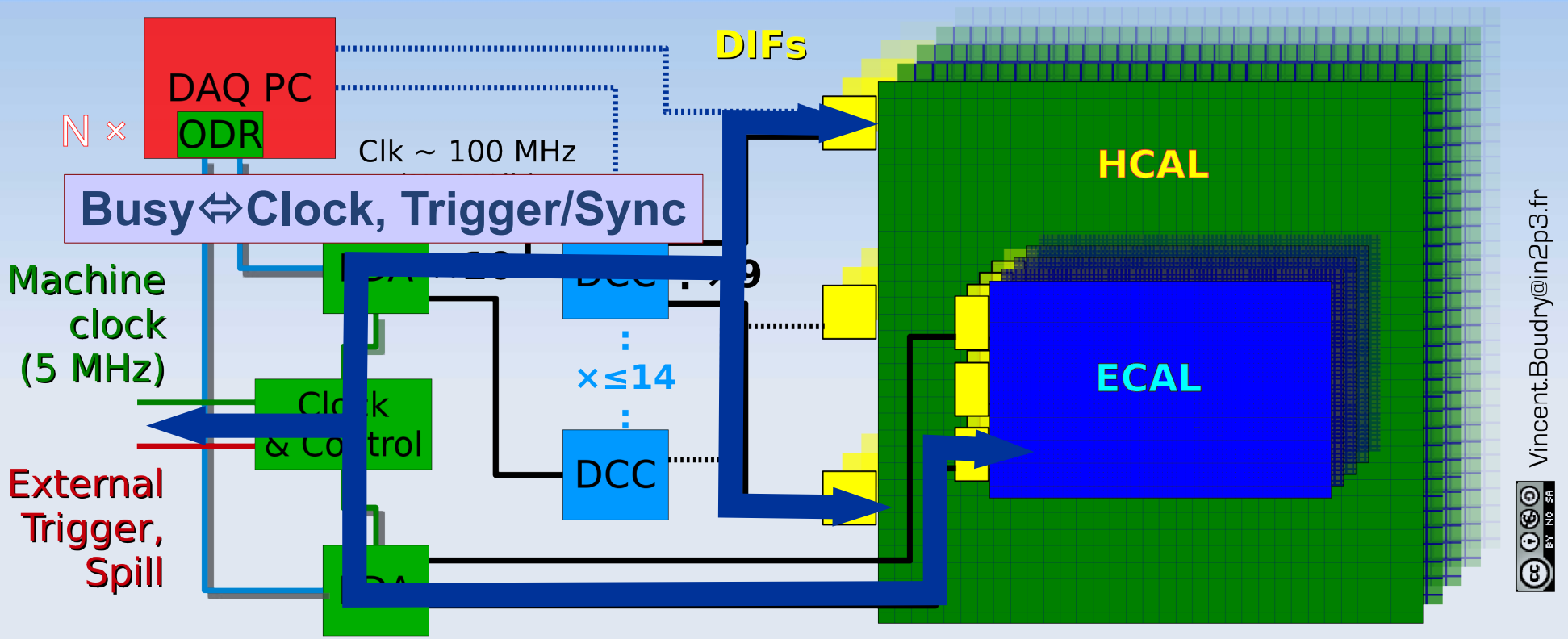

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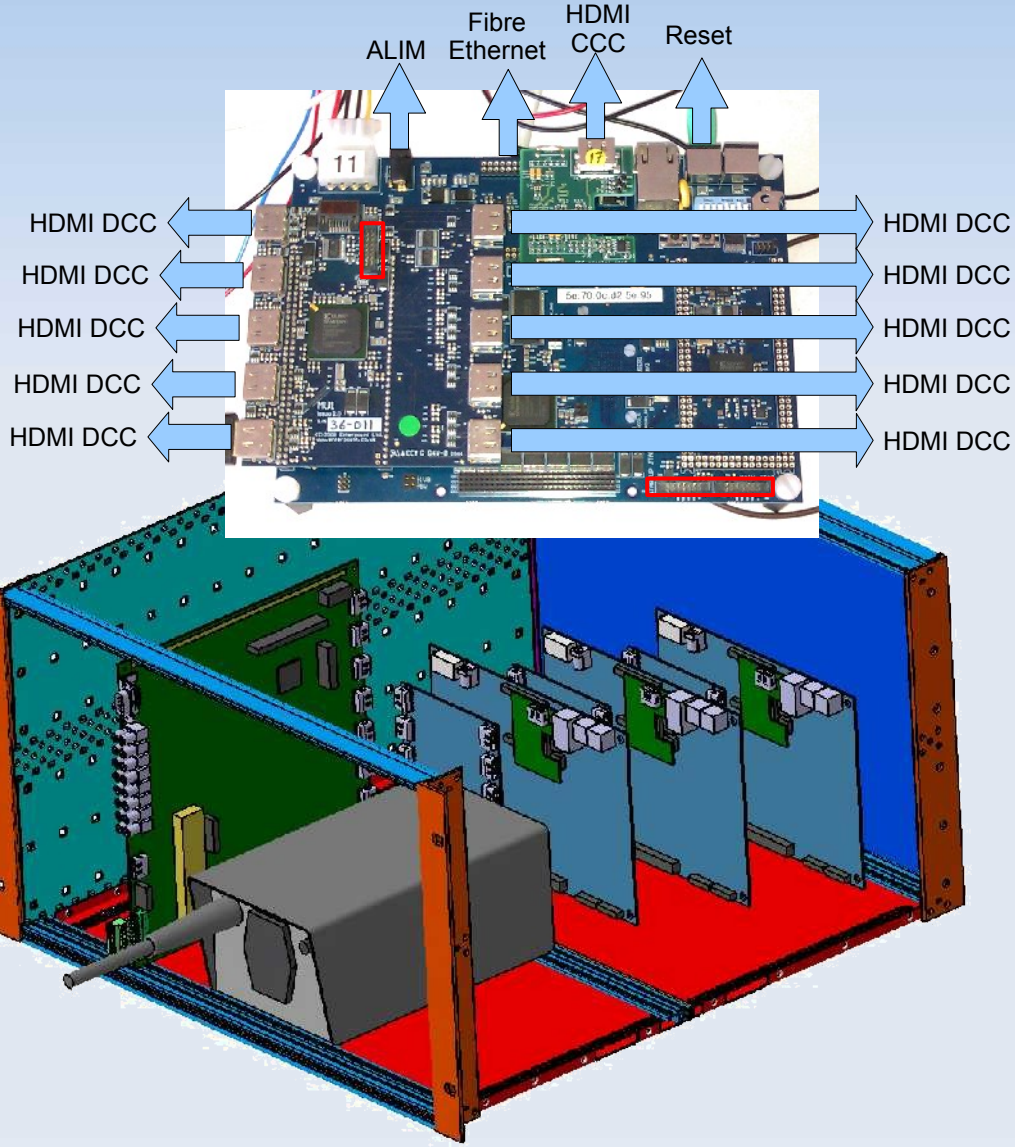
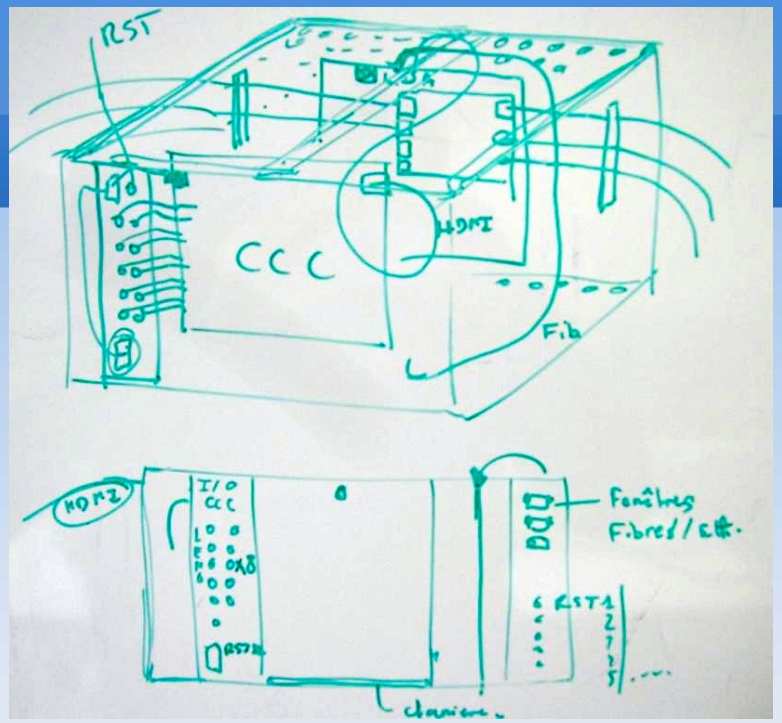
DHCAL Hardware DAQ elements

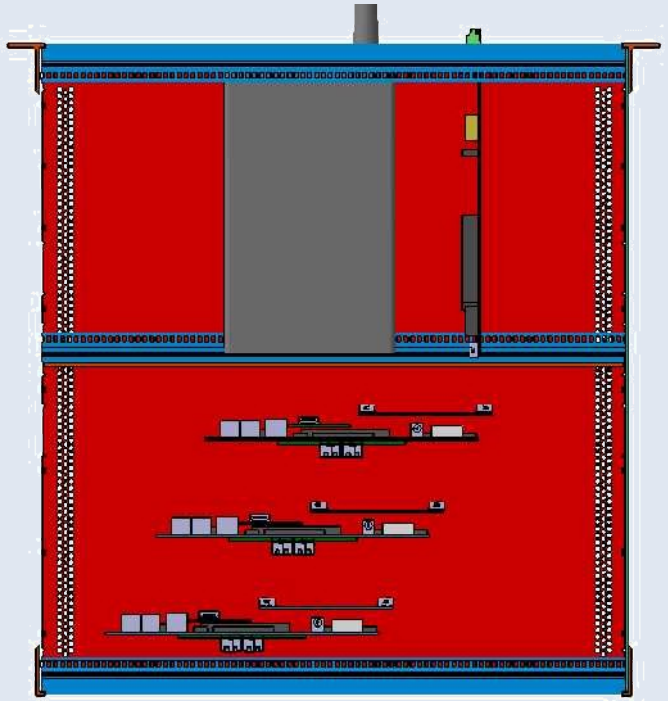
- 1 CCC: Clock & Control Card
  (8 LDA connections available)
- 3 LDA: Link Data aggregator
  (6 to 8 DCC connections available/LDA)
- 17 DCC: Data Concentrator Card
  (9 DIF connections available)
- 150 DIF: Detector InterFace
- 50 ASU: Active Sensor Unit

HW – CCC & LDA rack

- Study by M. Anduze

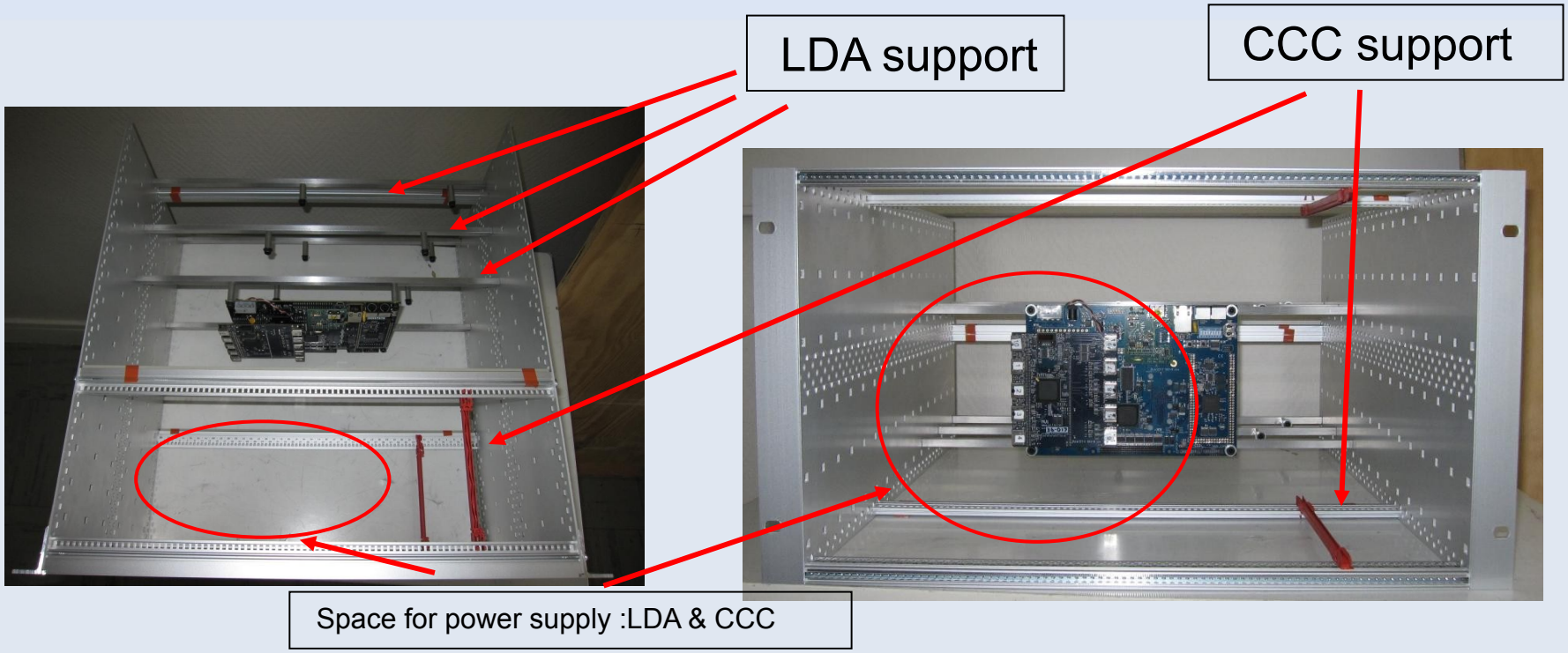






Mechanical aspect

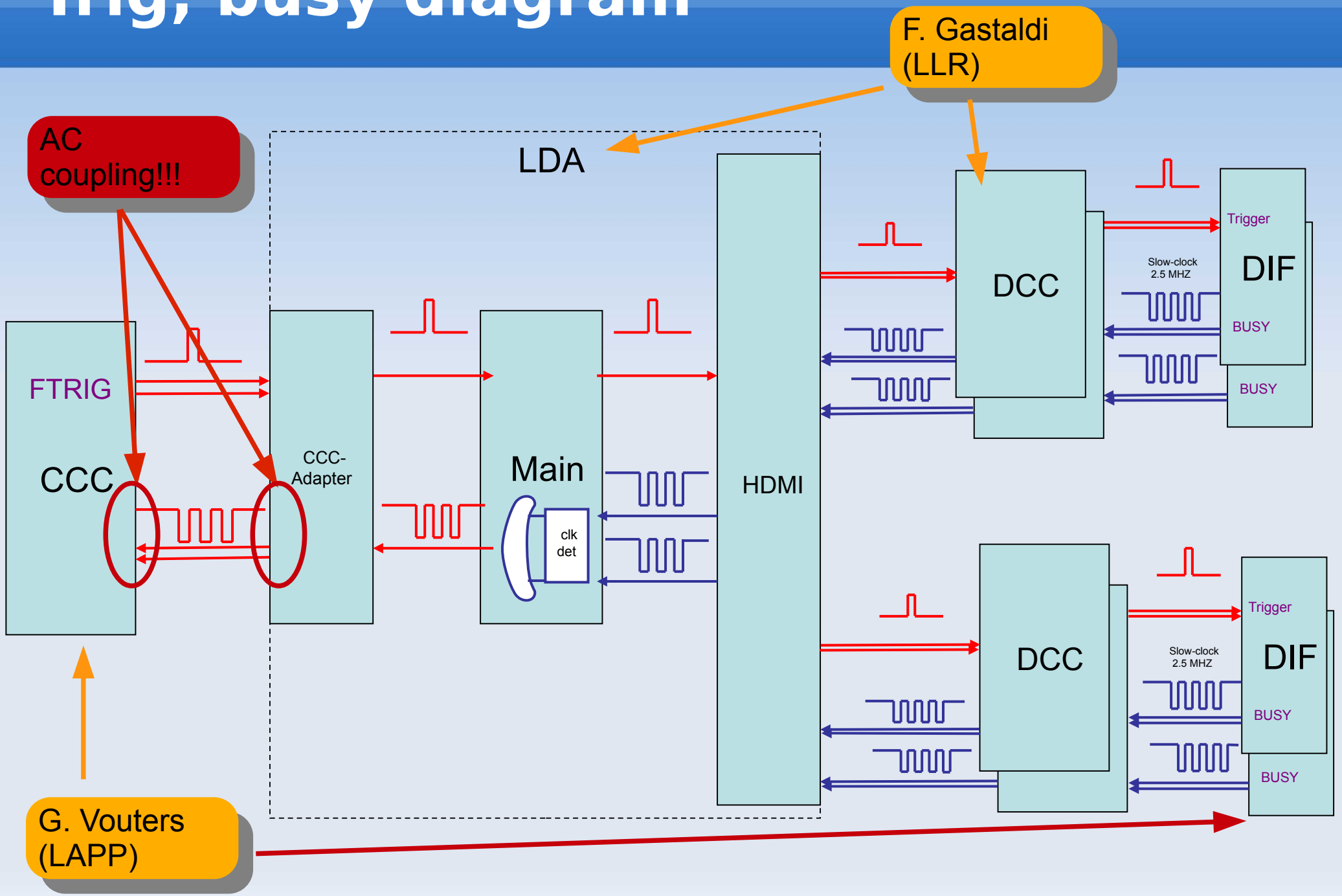
- Due to the special size of LDA, the mechanical team has install a support for each LDA in a chassis
- The HDMI cable from LDA to DCC will mounted on each side of the chassis



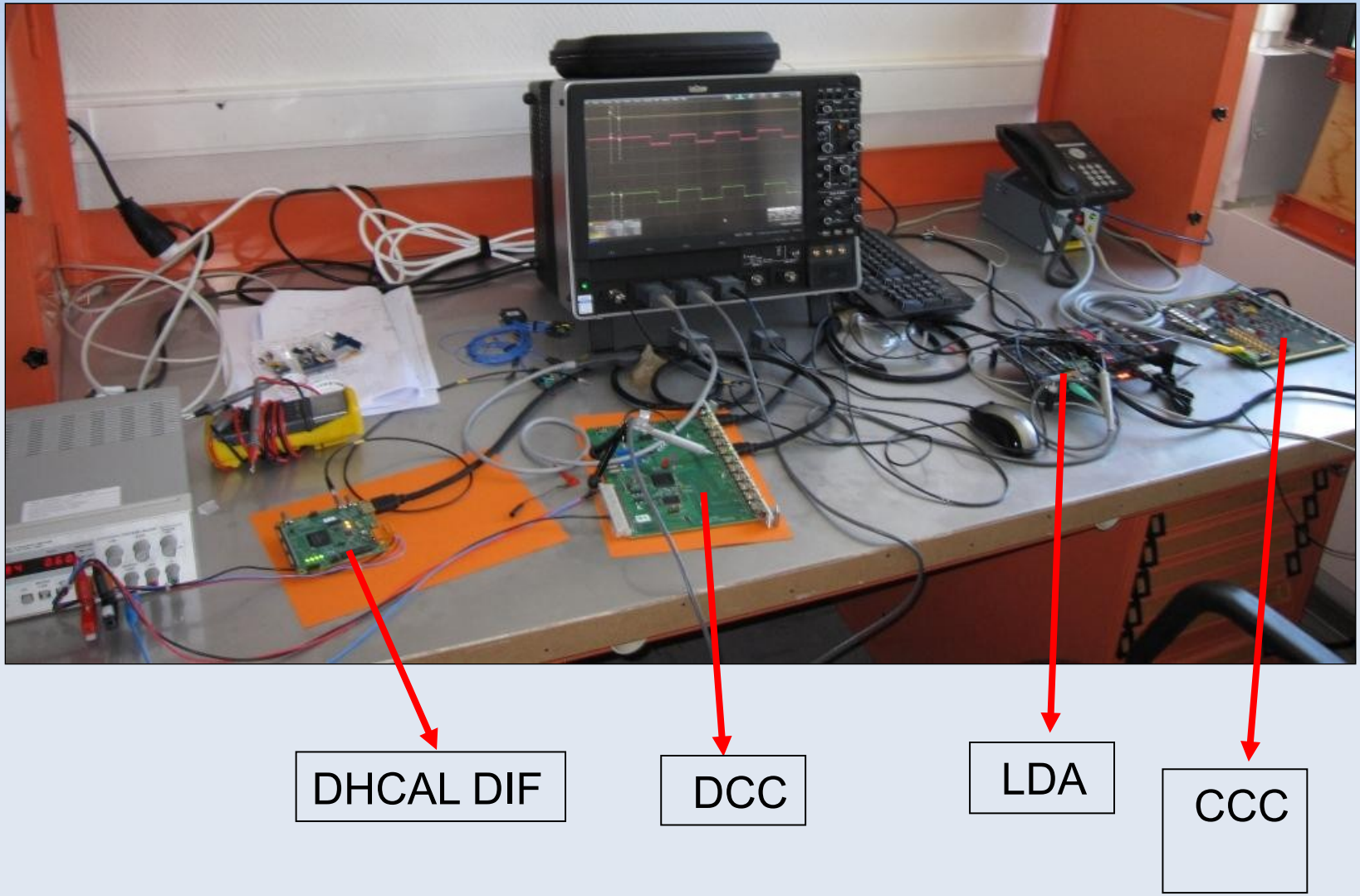
HW – Cable

- All 273 HDMI 5-m long halogen free cables arrived (remaining ones yesterday)
  - 90 arrived 4 weeks ago
    - No single pbm found.
  - SDHCAL ones being machined (~1 mm to be removed on the sides to fit onto the DCC)
  - Mechanics checked on detector side
  - Up to now: all good.
- Now Available for all detectors

Trig, busy diagram



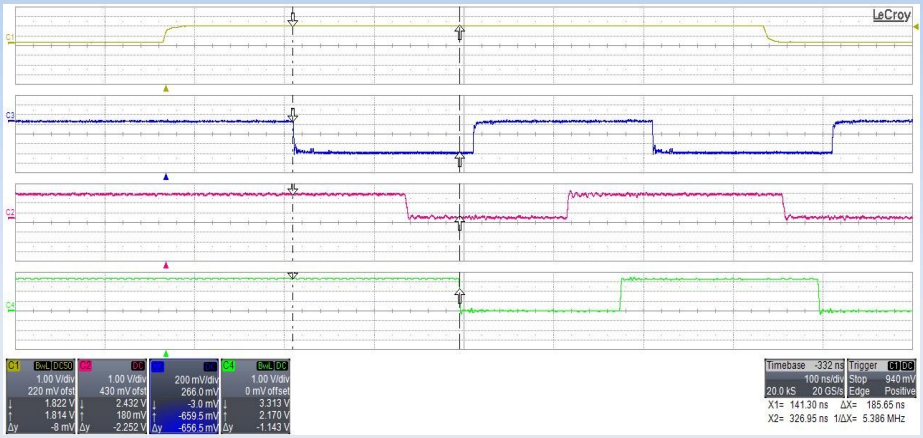
Trig, Busy tests setup



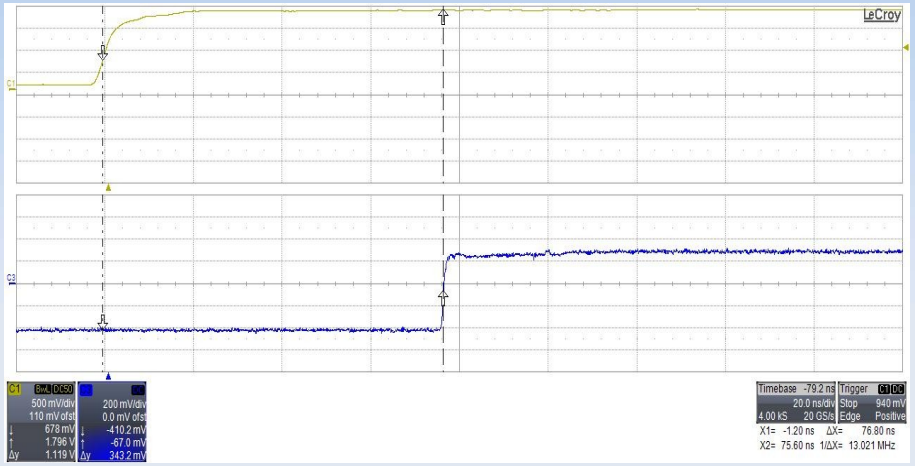
Busy : scope capture

- **Trig (NIM) → CCC → LDA → DCC → DIF**
  BUSY ← CCC ← LDA ← DCC ↵

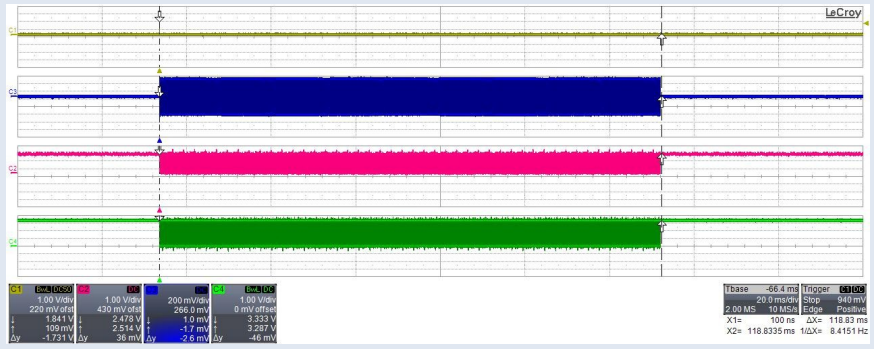
F. Gastaldi (LLR)



Yellow : Trigger
Blue : busy at the input of DCC ~ DIF out
Violet : busy at the output of HDMI card
Green : busy at the input of CCC
Delta between blue and green : ~ 185 ns



Delta between yellow and blue : ~76 ns
This is the delay between the reception of the trigger on DIF and the reception of busy on DCC.
Behavior test : The DIF receives a trigger and sends directly a busy signal

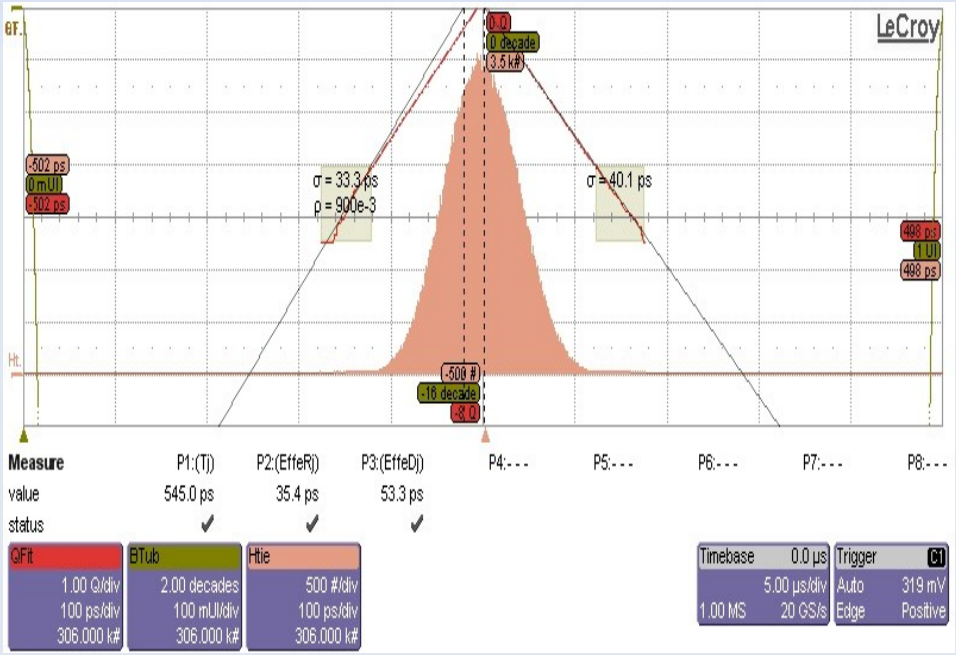
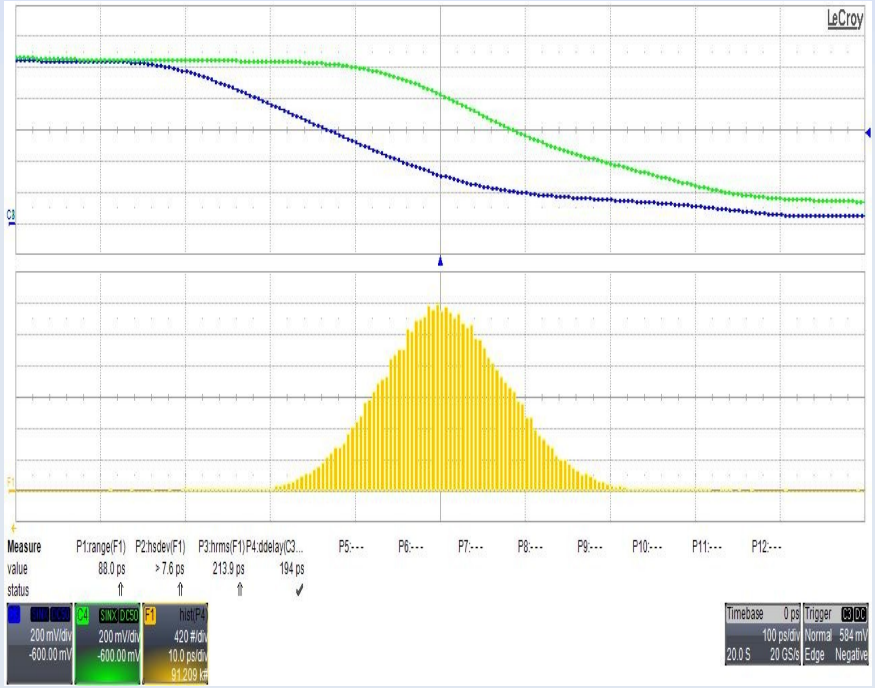


Busy duration test : here around 100 ms

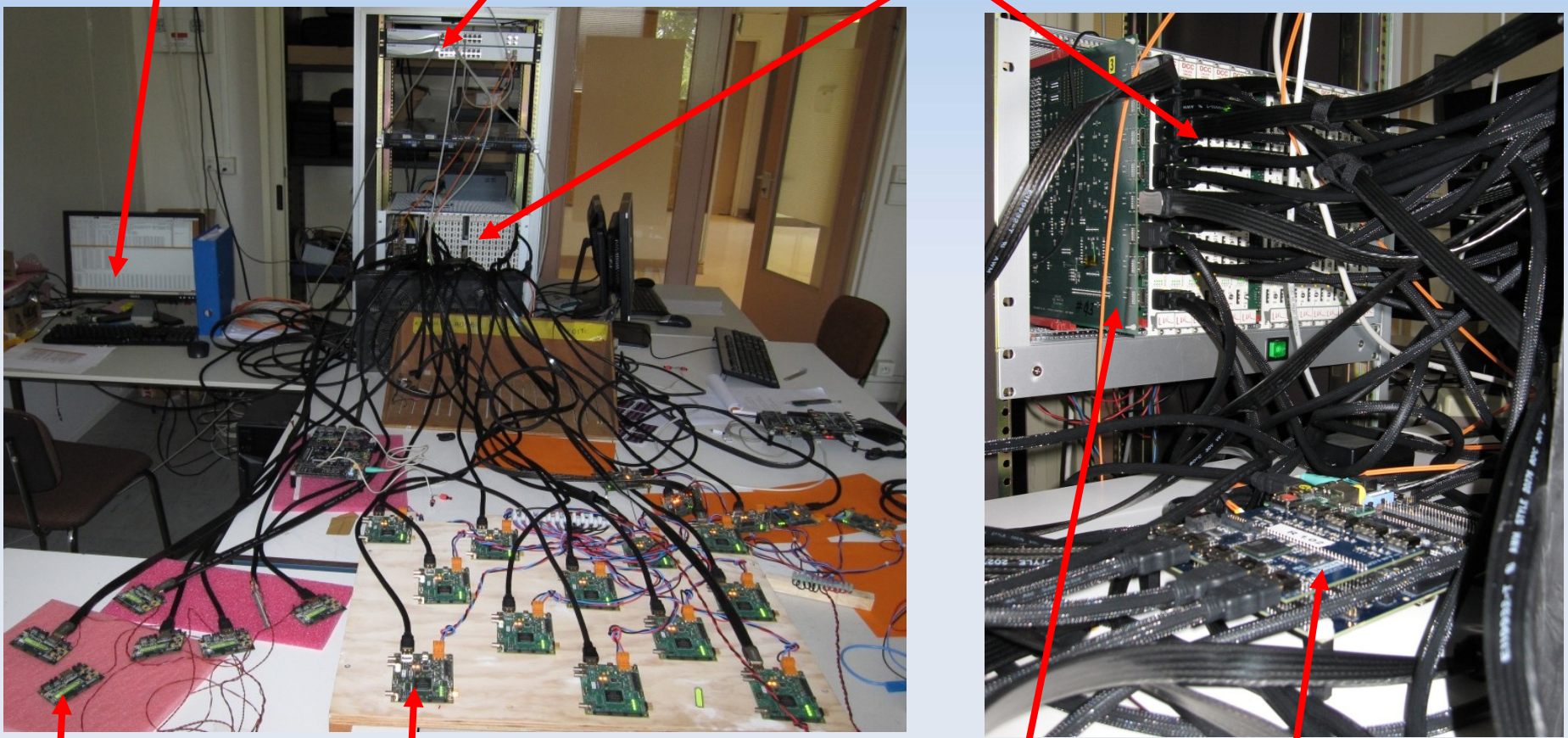
Busy signal equivalent at the slow clock 2.5 MHZ

Delay ≤ 200ns

Jitter measurement

Setup : CCC – LDA – DCC -DIF	
	
Setup : CCC – LDA – DCC -DIF	Delay between trigger on 2 DIFs, the delay is around 200 ps

Intensive tests setup (octopus !)



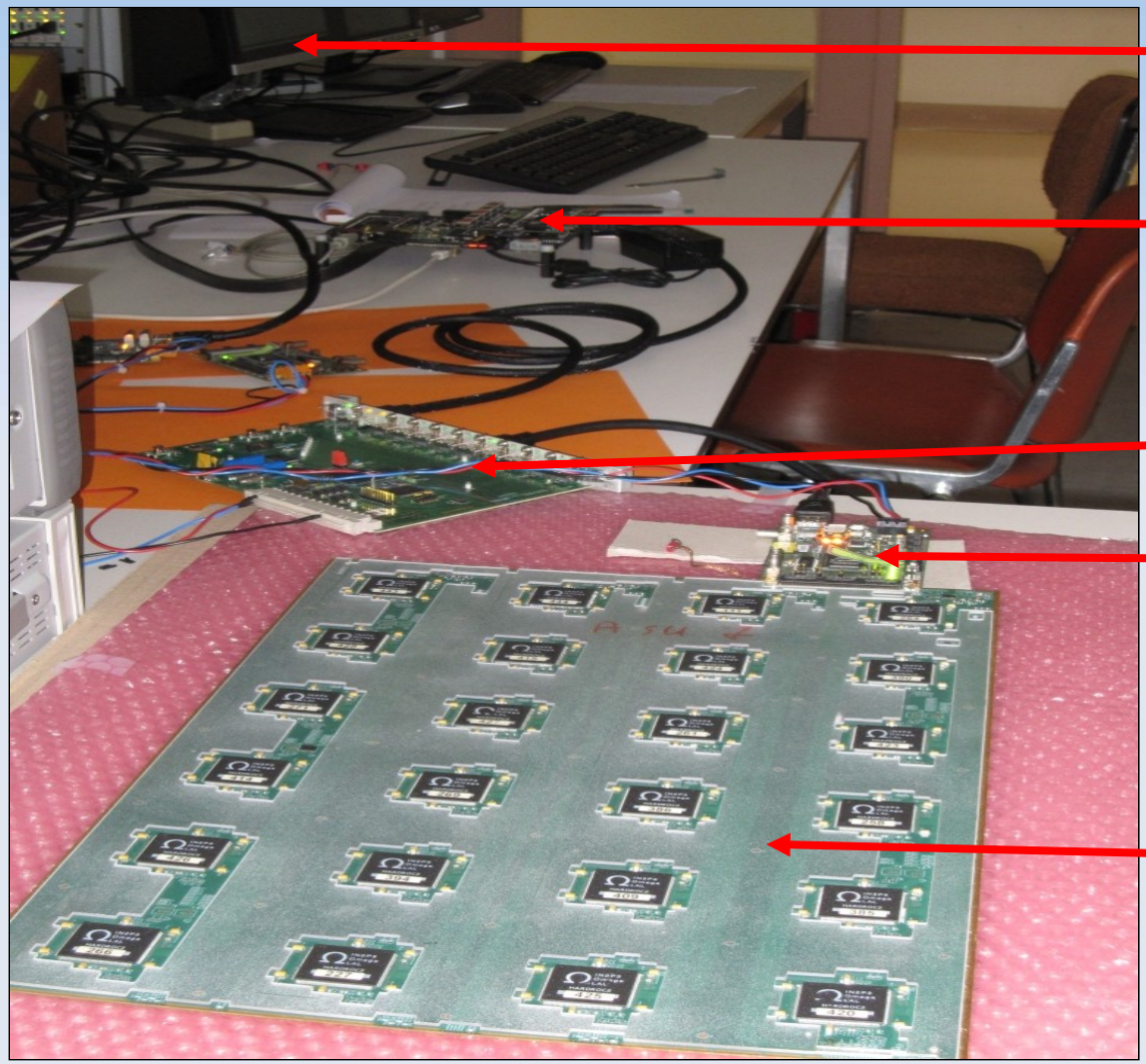
Intensity test

- The setup:
  - **2 DCC connected to 9 DIF and 1 DCC connected to 4 DIF.**
  - We launch a test and check if it appear an error in packet or a loss in packet.
  - The test is a pseudo-random pattern generation from the DIF at the maximum data rate (16 bits at slow-clock) in continuous.
  - In normal mode, we have a data rate of 1 bit at slow-clock (speed of ASIC) or slighly above
  - readout using libLDA (C++ API for DAQ2).
- We made these tests for each LDA channel which work
- These test shown an acquisition without error or loss during several hours (between ½ day to 1 week-end)
- We have succeeded to send and to receive data on DIF (ECAL or DHCAL).
  - However, we couldn't get a good acquisition on 10 LDA channels together. The average of good connection on each card is 7.
  - We haven't really investigate this issue because our priority was to get a stable behaviour with the intensive test.

Intensity tests

- ≠ configs
  - 1 LDA ← 6 DCC ← 2 DIFs
  - 1 LDA ← 10 DIFs :
    - 30 Mb/s
  - 1 LDA ← 9/10 DCCs ← 1 DIFs (depending on LDAs)
    - Achievable BW: ~ 32 MB/s (tbc with 10×40Mb/s = 50 MB/s max th.)
      - 1st: High failure rate (2 10^{-4} error rate ⇒ 1 error / 10 s)
        - Found to be related with Copper Wire (Cl. 5 when Cl. 6 reqd for G-Eth)
  - With Opt. Fibre: error rate <**10^{-14}** failures (26 Mb/s × 60h)
- **To be X-checked with fast signal presence**
  - (warning from M. Warren)

Slow-control tests setup



FW – DIF

- Lot of progress since 1 ½ months
- Integration of Guillaume HardRoc code in Remi's framework
  - All vital functionality there
    - Config loading & checking
    - Data sending
      - Format ~specifications (header)
    - Trigger & BUSY
  - Migration to FM v2.1 (cleaner) done
  - Works on SDHCAL & ECAL DIF
    - HR2 & SPIROC2
  - Cleaning of code on-going for internal & external use (FCAL)
    - DIF code to be adapted (by FCAL's Witold Daniluk & Itamar Levy) for the readout of the FCAL samples
      - 4× (8 channels front-end ASIC + 8 channels ADC ASIC) → 32 channels.
    - mini-WS mid-April @ LLR by RC.
      - part of AIDA 8.6.2 package...

FW Performance Map

	LDA	DCC	DIF's
Ethernet	✔ at full speed		
CCC	Clk; Trig; Busy	Clk; Trig; Busy	Clk; Trig; Busy
Nlinks up	10 32 MB/s	9	1
Fast Commands	✔	✔	✔
Block transfert (Config loading)	✔	✔	✔
Data	✔ (< 50 MHz)	✔ (< 50 MHz)	✔ (<50 MHz)
ROC			Structure; Config; R/W; modes ~✔ Data format

Generic code for all DIFs
G. Vouters (LAPP)+ R. Cornat (LLR)

Basic function status (Python scripts)

- SDHCAL (1 LDA + 1 DCC + 1 DIF + 1 ASU(v2 : 24 HR2 ASICs))
  - Much work from G. Vouters (LAPP), F. Gastaldi (LLR), R. Cornat (LLR), N. Roche (LLR)
  - Config ✔
  - Data readout ✔
    - High intensity tests... above required perf in term of data flux.
      - tested with to the limit
      - OK with ~10.43/16th of max bandwidth (9/16th required)
  - Test beam mode identical to USB readout
    - **To be tested next!**
  - Sync mode to be tested
- ECAL (1 LDA + 1 ECAL DIF + 1 Sweat proto + 4 Skyrocs ASU)
  - Config ✔
  - Readout ~
- AHCAL
  - LDA readout started.

Integration SDHCAL (XDAQ)

- **XDAQ**+ libLDA (1 LDA + 1 DCC + 1 DIF + 1 SDHACL ASU**v3 (⊃HR2b)**
  - Configuration ✔
    - same set-up in LLR and IPNL
    - Setting & reading config
      - No basic problem with XDAQ integration
  - Step-by-step readout (DIF is PC driven)
    - (Config; Run mode; SW trigger → ROC; StopAcq; Readout)
    - with some glitches (redundant header, some bit shifts)
      - Was working with ASUv2
      - Boundary conditions being examined
        - Waiting for expert work (G. Vouters next week)

Nicolas Roche (libLDA)
Christophe Combaret (XDAQ)

- First priority → test in Beam Test mode.
  - readout on ext. trigger

CCC news – Sequencing

- Some new control commands should be instantiate in firmware for the test beam: start, stop acquisition, ram full and sync_mode.
  - Allows for sync restart of all DIF as soon as BUSY signal ↘
- These commands will be sent to the LDA. The LDA sends these commands in fast-command mode.

Nota: Guillaume and Franck will implement these functions in the coming days. They will need a few days to validate this link based on the UART protocol. Certainly tested at LYON next week (see the planning)

  - CCC code based on stand-alone CCC-DIF code developed in LAPP for µMegas & GRPC test stands.
    - Specifications ready
  - LDA modules already nearly completed.
- “Lower priority” (faster readout)

Planning and conclusions (low level)

- CCC is close to be ready. The latest improvements are underway
- DCC is ready, not really working on it now
- LDA firmware is currently in a correct state
  - The last features with the CCC is under development.

=====

- The DAQ will be send to Lyon next week for the first tests with 6 RPC (18 DIF)

=====

- June 1st, the DAQ will be send at the CERN
- Week of June 6th, cabling of the DAQ and first cosmic test

=====

- June 10th, DAQ is ready for the beam tests (we cross the fingers !!!...)

SW – CALICE integration

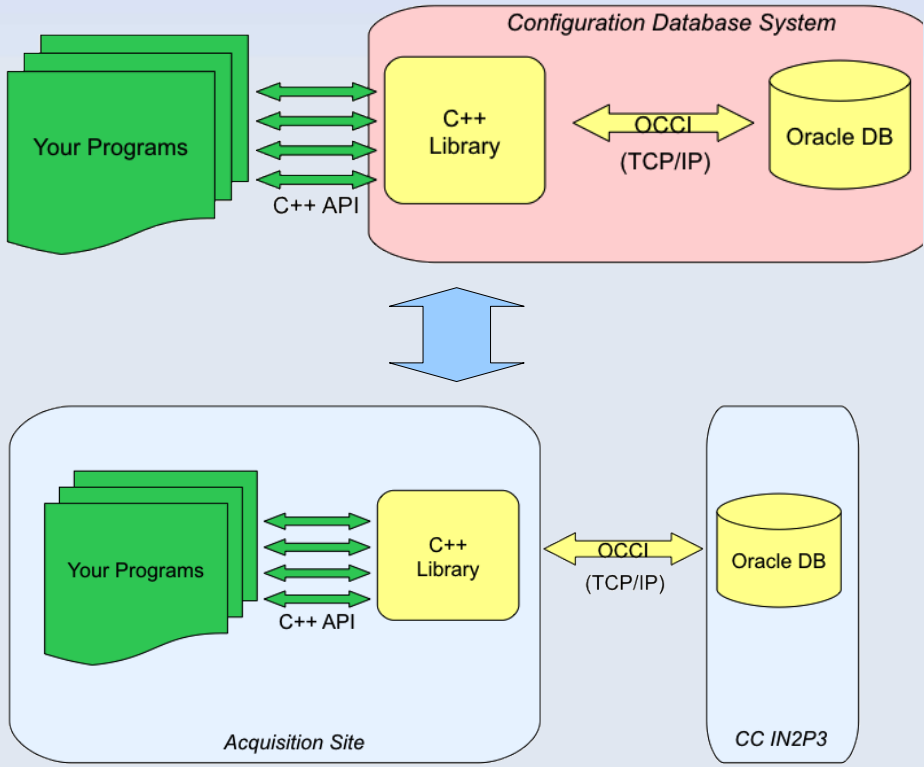
- Config DB
  - 1st prototype proposed by G. Baulieu (IPNL) 2 weeks ago
  - Configuration parameters for LDA, DCC, DIF and ASIC.
    - development DB at CC IN2P3

Possible evolutions

- The current model has been created from the DHCAL configuration (HR1, HR2, …)
  - We can improve it to make it more generic (ASIC instead of HR2, …). Need to decide now to avoid huge work later!
  - Do we need to do the same for other parts (DIF, LDA, DCC...)?
- The C++ library can also evolve :
  - hr2Object->getCTest() → asicObject->getInt("CTEST")
  - A new ASIC would be easy to integrate in the system

Are you interested in the system?
Should we go for a common database?

G. Baulieu 17/03/2011

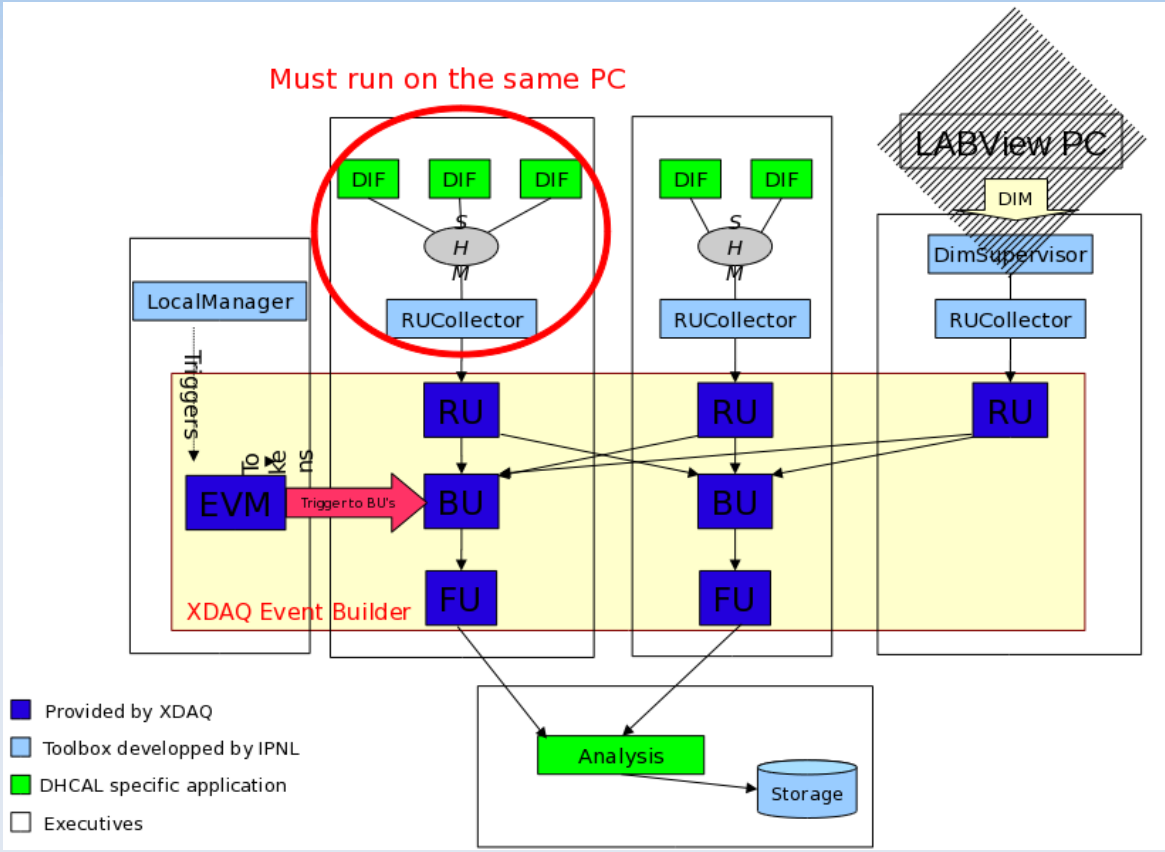


- Check Guilaume Baulieu Talk (next one)
- Link with CaliceDB → SDHCAL contact Gerald Grenier

Software: XDAQ framework

- dev[ts] started @IPNL for electronics test using XDAQ in 2008
  - Ch. Combaret (IPNL)
  - Gained (a lot of) impulsion with involvment of L. Mirabito (resp. of DAQ SW for CMS tracker)
- Ran for ≥ 1 year in TB, Cosmics & Electronics test
  - USB readout
  - Interface to old LabView program
- Recent development
  - Writing of LCIO data in RAW format
  - versatile online analysis framework (root histos)

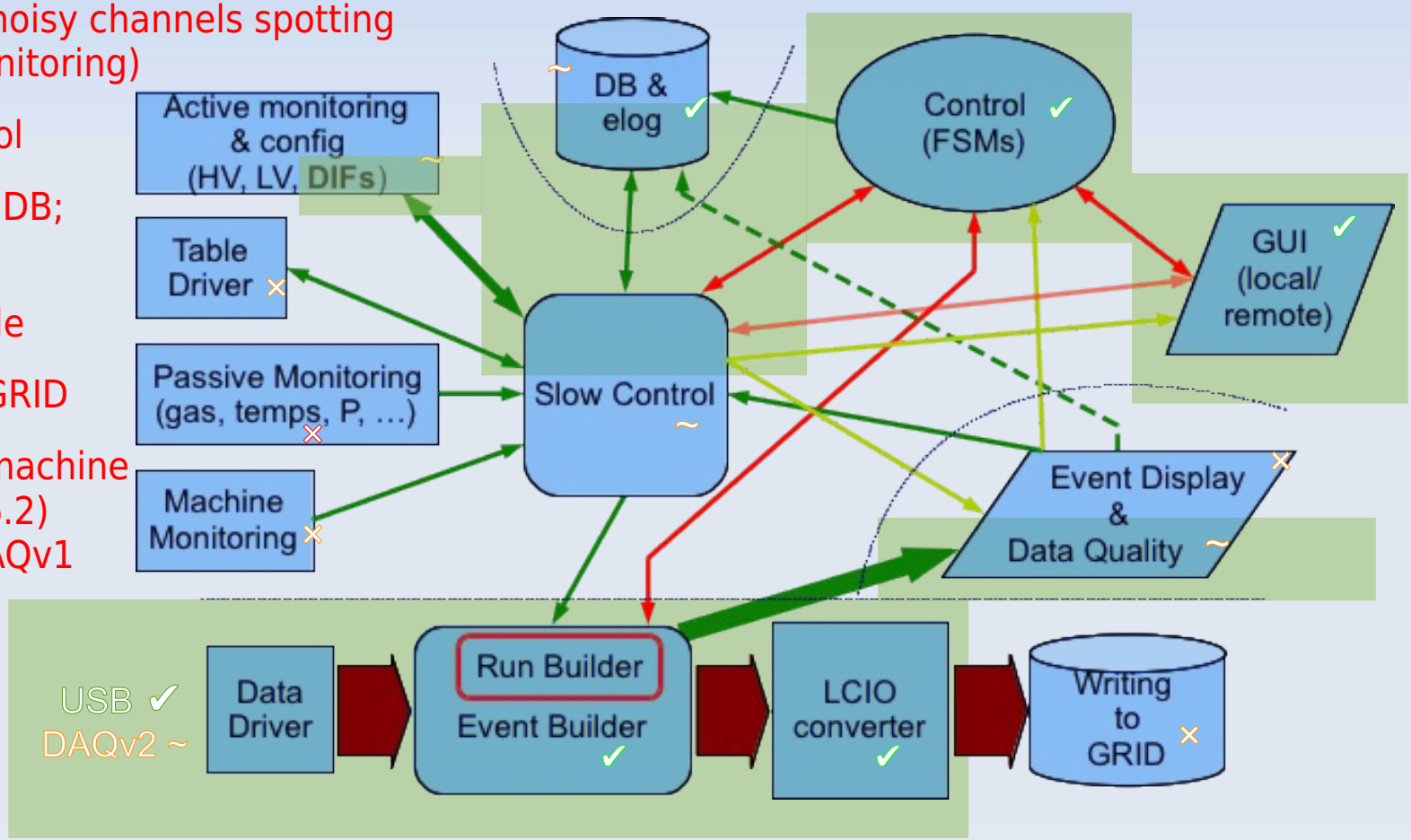
→ Marlin Based



IPN Lyon

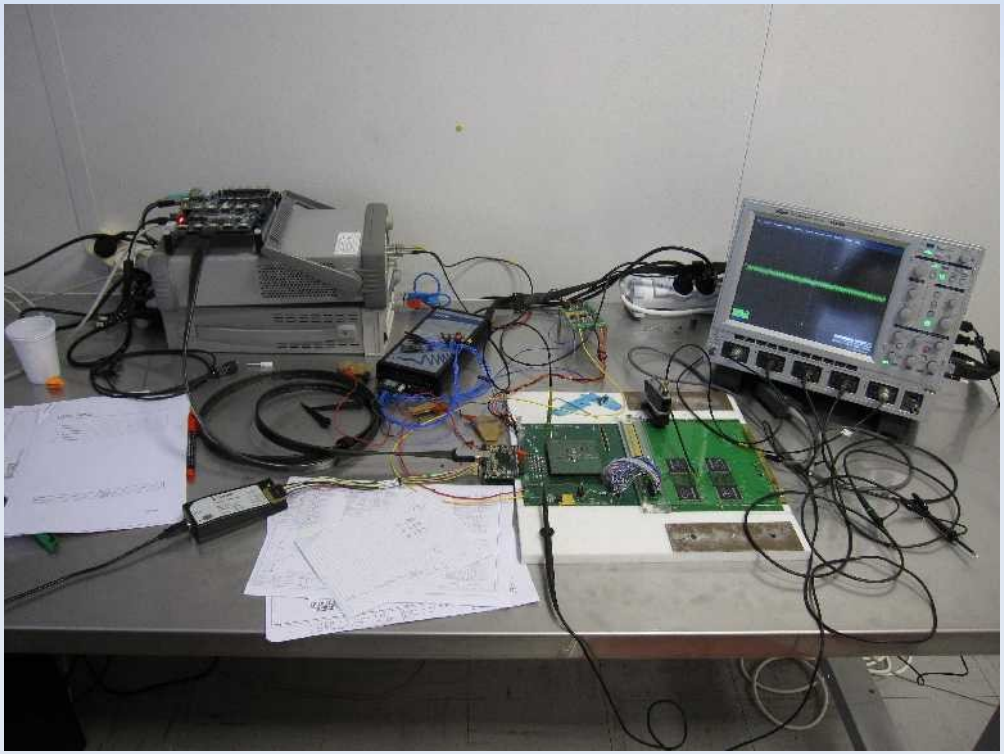
SW status

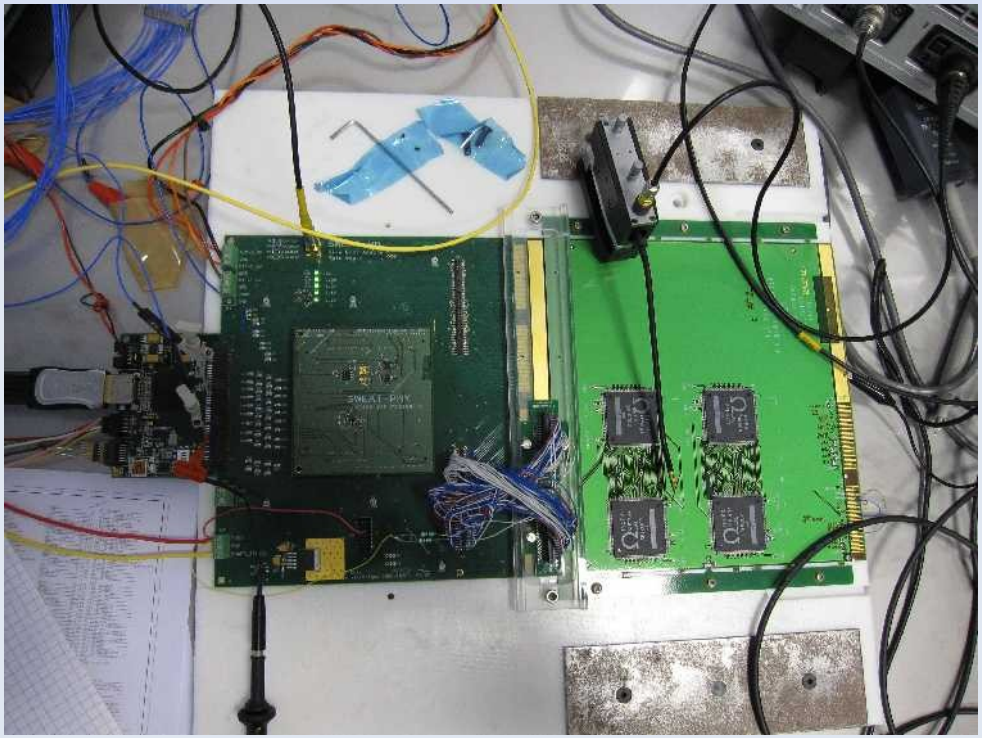
- Critical elements
  - Configuration DB : **nearly complete**
  - DAQ2 interface ↔ XDAQ : **nearly complete**
- Missing ancillaries
  - Semi-automatic noisy channels spotting & correcting (monitoring)
  - Clean Slow control
  - interface to CondDB;
  - event display : DRUID on LCIO file
  - interface to the GRID
  - interface to the machine (⊃ in AIDA WP8.6.2) Code exists in DAQv1



Test – ECAL

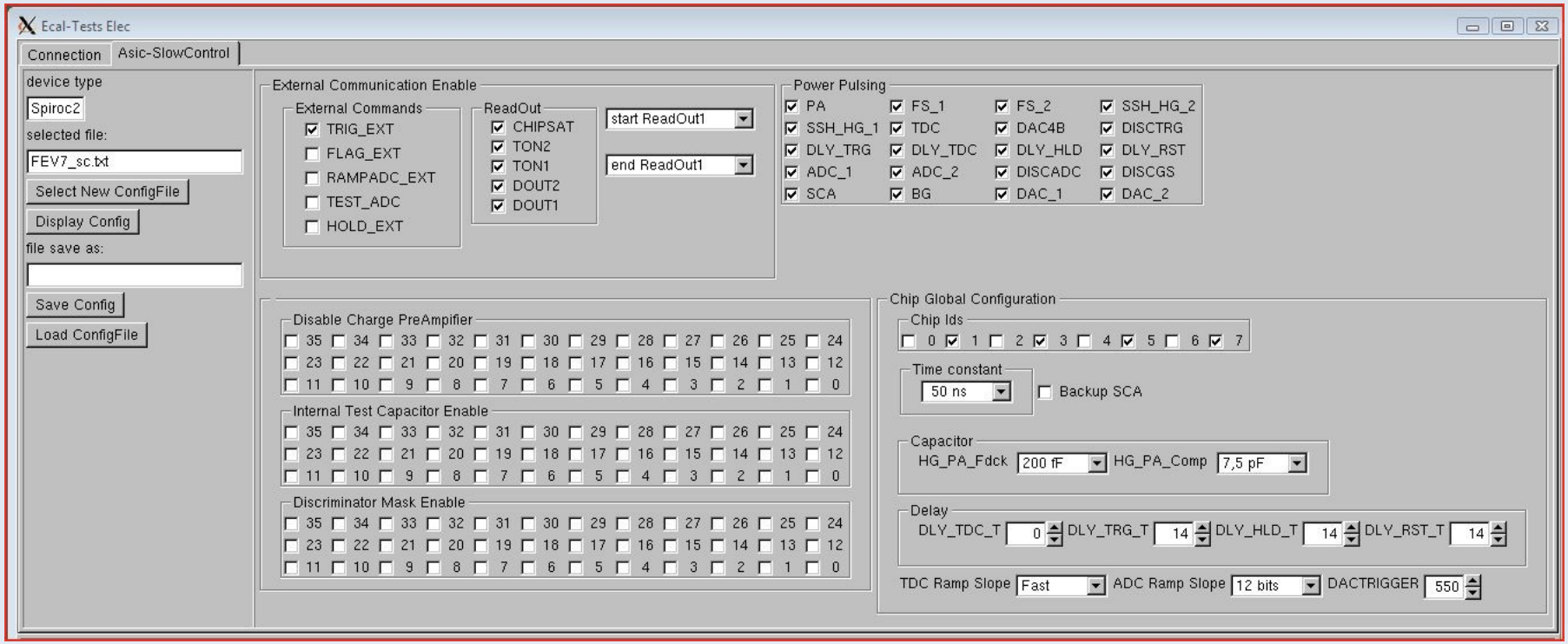
- Test of SpiRoc2: Rémi Cornat + Stéphane Callier
- Basic functionality OK
  - but require some joggling between Labview generated Config file on Stephane laptop ↔ Linux DAQ PC





Integration status : ECAL

- Python testing
  - Preliminary phase:
    - Configuration ✓
    - Locked after a triggers
    - Data packet being splitted randomly (≠ from the SDHCAL)
- Migration to libLDA for intensity tests & use of GUI for configuration management. (useful for debugging → e.g. AHCAL ?)



Vincent.Boudry@in2p3.fr

Plans

- HW: all is ready
  - syst. check of LDA “on demand”
- FW: (Hopefully) Final checks on critical FW
  - Still a bit of FW (data format...)
  - Glitches for ASUv3 to be tamed (next week)
- SW with XDAQ integration almost complete
- Implement automatic procedure on CCC

Installation in IPNL next week
(Rack + 3 LDA + 17 DCC
+ carte + cables)

- More emphasis to be put on SW
  - DB (config [IPNL] / condition [CALICE])
  - analysis tools
  - Beam interface from DAQ1
  - GUI
- Started regular meetings on this topic