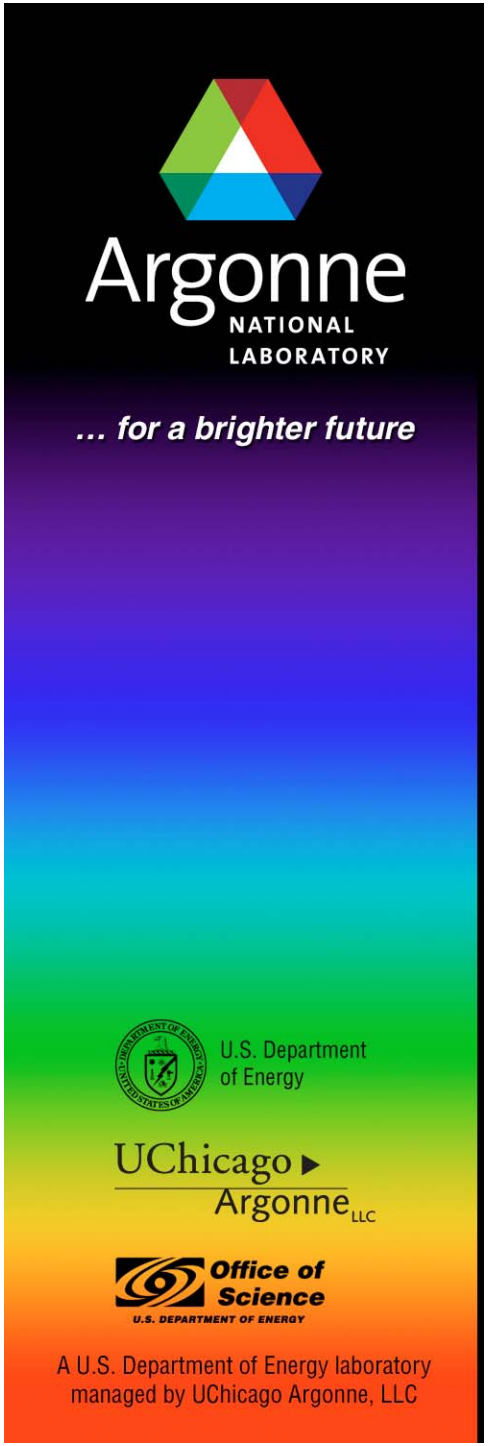


Digital HCAL Electronics
Summary of Electronics Production

Lei Xia

Argonne National Laboratory

Representing the DCAL Electronics Group

CALICE Collaboration Meeting

CERN

May 19, 2011

RPC DHCAL Collaboration: → 36 People, 7 Institutions

Argonne National Laboratory

Carol Adams
Mike Anthony
Tim Cundiff
Eddie Davis
Pat De Lurgio
Gary Drake
Kurt Francis
Robert Furst
Vic Guarino
Bill Haberichter
Andrew Kreps
Zeljko Matijas
José Repond
Jim Schlereth
Frank Skrzecz
(Jacob Smith)
(Daniel Trojand)
Dave Underwood
Ken Wood
Lei Xia
Allen Zhao

Boston University

John Butler
Eric Hazen
Shouxiang Wu

Fermilab

Alan Baumbaugh
Lou Dal Monte
Jim Hoff
Scott Holm
Ray Yarema

IHEP Beijing

Qingmin Zhang

University of Iowa

Burak Bilki
Ed Norbeck
David Northacker
Yasar Onel

McGill University

François Corriveau
Daniel Trojand

UTA

Jacob Smith
Jaehoon Yu

RED = Electronics Contributions
GREEN = Mechanical Contributions
BLUE = Students
BLACK = Physicists

Brief Overview of System

General Electronics System Specifications

- Front-end instrumentation to use 64-channel custom ASIC
  - 1 cm^2 pads, 1 $meter^2$ planes, 38+14 planes, → ***480,000 channels***
- Front-end channel consists of amplifier/shaper/discriminator
- ***Single programmable threshold*** → 1 bit dynamic range
  - Threshold DAC has 8-bit range
  - Common threshold for all 64 channels per ASIC
- ***2 gain ranges***
  - High gain for GEMs (10 fC - ~200 fC signals)
  - Low gain for RPCs (100 fC - ~10 pC signals)
- 100 nSec time resolution
- ***Timestamp each hit***
  - 1 second dynamic range → 24 bits @ 100 nSec
  - Synchronize timestamps over system
- ***Data from FE consists of hit pattern in ASIC + timestamp***
  - 24 bit timestamp + 64 hit bits = 88 bits (+ address, error bits, etc.)
  - Readout format: 16 bytes per ASIC

General Electronics System Specifications (Continued)

- Capability for ***Self Triggering*** → Noise, Cosmic rays, ***Data errors***
- Capability for **External Triggering** → Primary method for beam events
  - 20-stage pipeline → 2 μSec latency @ 100 nSec
- Capability of FE to source prompt Trigger Bit (simple OR of all disc.)
- Capability to store up to 7 triggers in ASIC output buffer (FIFO)
- Design for 100 Hz (Ext. Trig) nominal rate
- ***Deadtimeless Readout*** *(within rate limitations)*
- Zero-suppression implemented in front-end
- On-board charge injection with programmable DAC
- Design for 10% occupancy
- Concatenate data in front-ends
- Use serial communication protocols
- Slow controls separate from data output stream
- Compatibility with CALICE DAQ

General Electronics System Specifications (Continued)

- General Considerations
  - Readout system ***was not*** designed for use in a real ILC detector
    - *Not optimized for power consumption*
      - No power pulsing
      - Not a low-power design
      - Additional cooling was needed
    - *Not optimized for minimal DAQ links*
      - No token-ring readout
      - Each front-end board has a dedicated link to the DAQ
    - *Not optimized for minimal power links*
      - Each front-end board has a power connection to a remote DC power supply
    - *Not optimized for thickness*
      - Chip packaging 1.4 mm high
      - Separate pad board & front-end board
    - *Not optimized for low-cost*

General Electronics System Specifications (Continued)

- General Considerations (Continued)
  - Read-out system ***WAS*** designed to test fine-grained calorimetry
    - *Front-end chip was needed, which performed the basic functionality*
    - *Simple system design – No cutting-edge technologies*
      - No complicated token-ring read-out structures
      - Each front-end board had separate power & serial read-out links

      ⇨ *Was key in getting system up quickly and running reliably*
    - *Avoided difficult front-end board fabrication techniques*
      - No blind & buried vias
        - *Very costly*
        - *Low yield*
        - *Limited vendors*

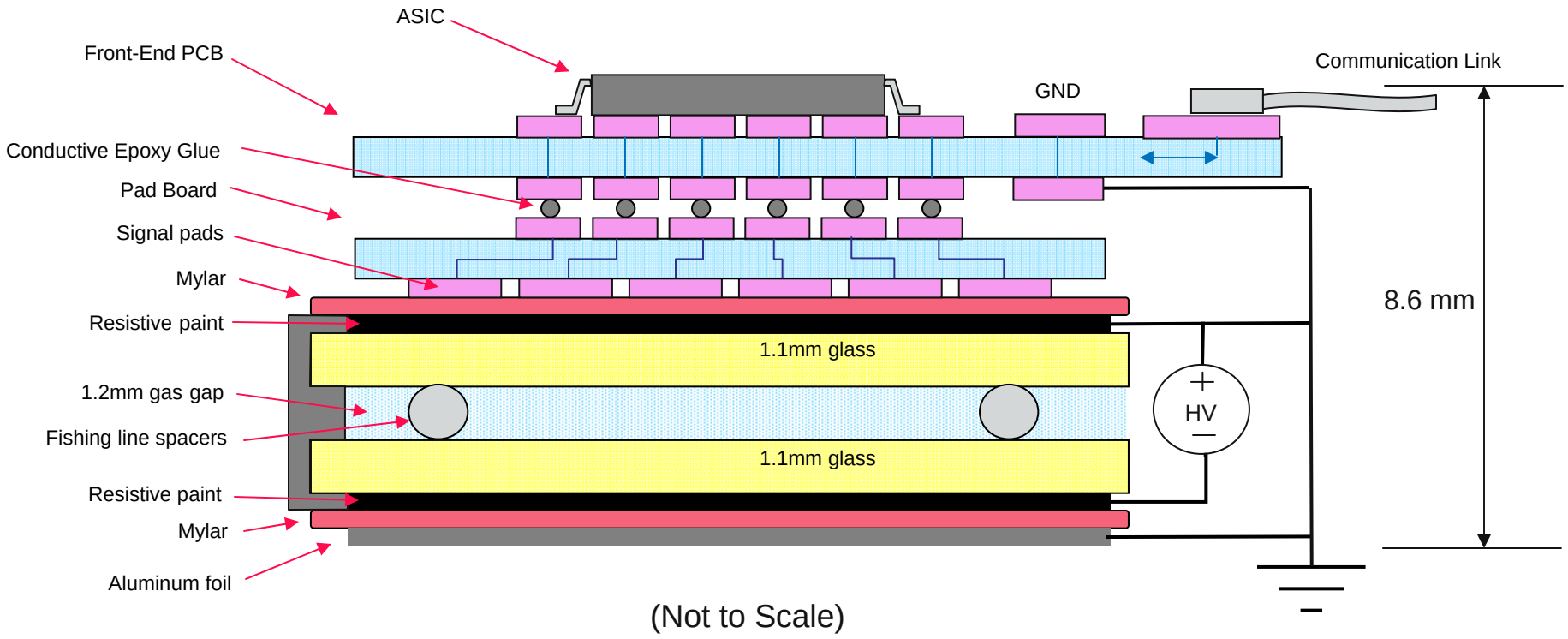
      ⇨ *Even without blind & buried vias, design of front-end board was a challenge…*
    - *System was designed capable of measuring cosmic rays*

      ⇨ ***Compromises aimed at proving detector concept***

      ⇨ ***Proved to be a good strategy***

Detector Configuration

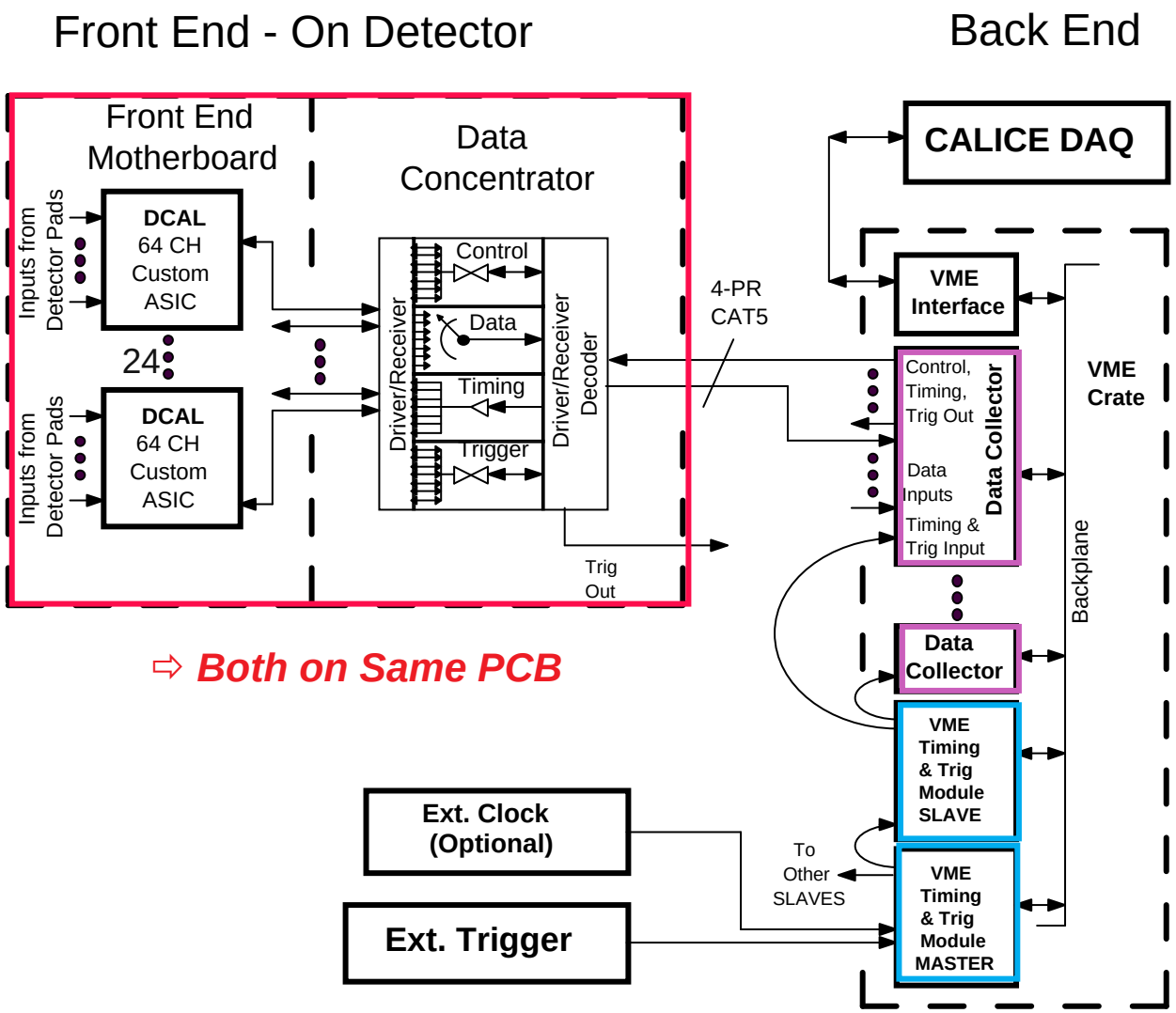
Chamber Construction with Electronics:



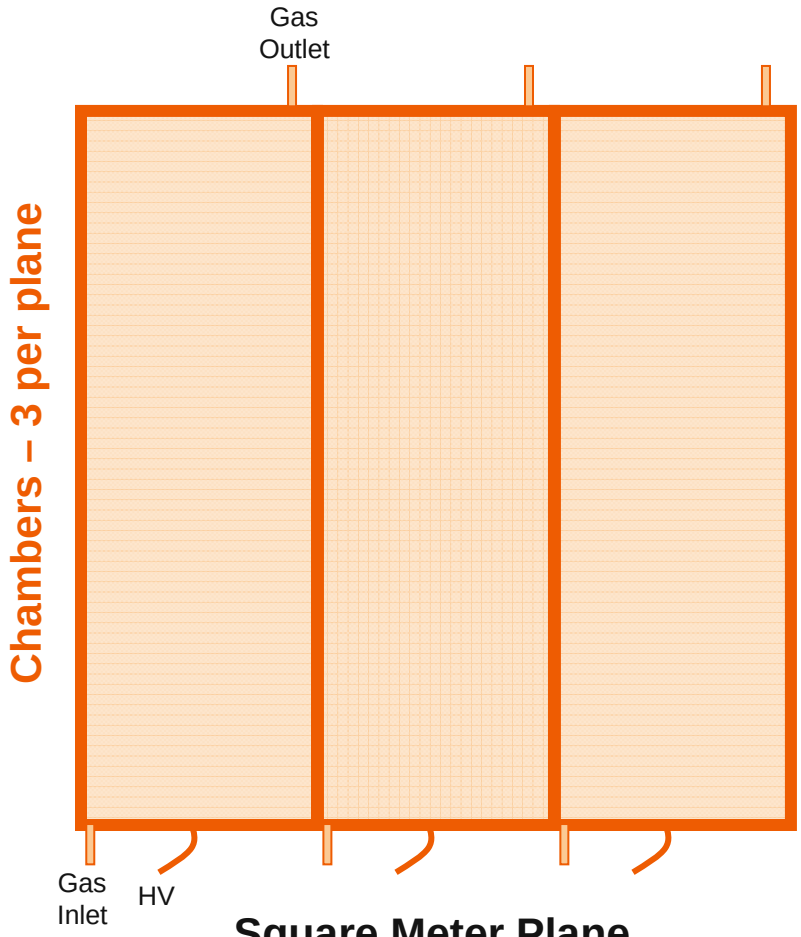
(Not to Scale)

Grounding is important…

System Block Diagram



System Physical Implementation

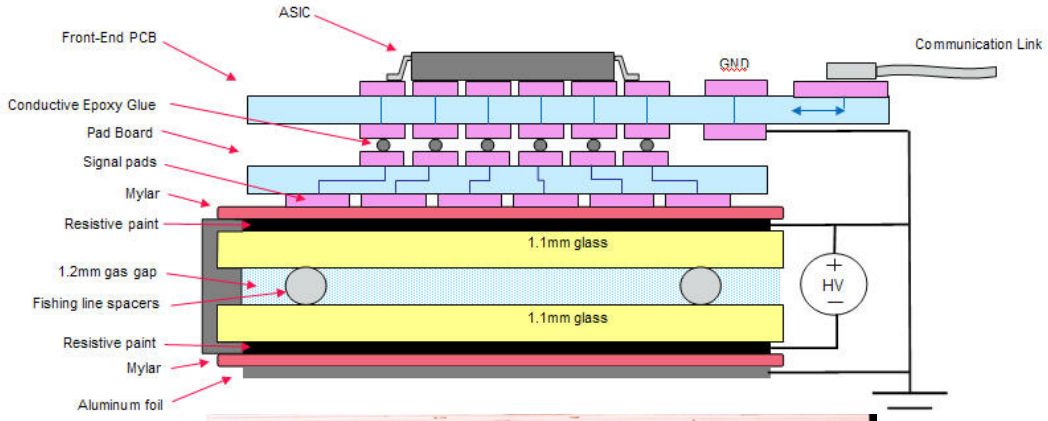


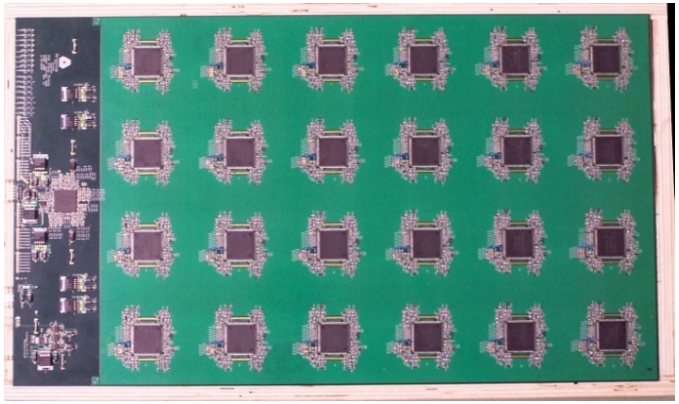
Square Meter Plane
(3) 32 cm X 96 cm chambers

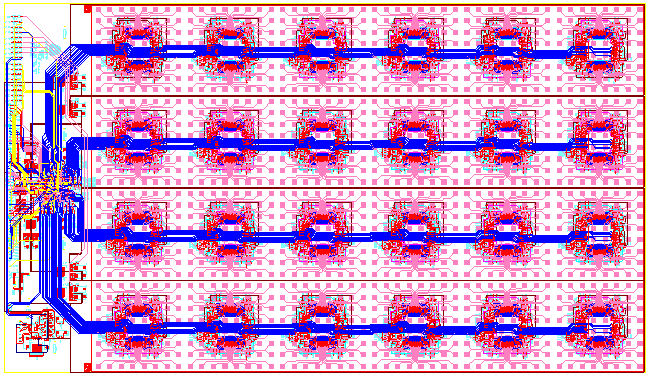
- Plane Construction
  - A plane consists of 3 independent chambers
  - Planes held together in frame

System Physical Implementation (Cont.)

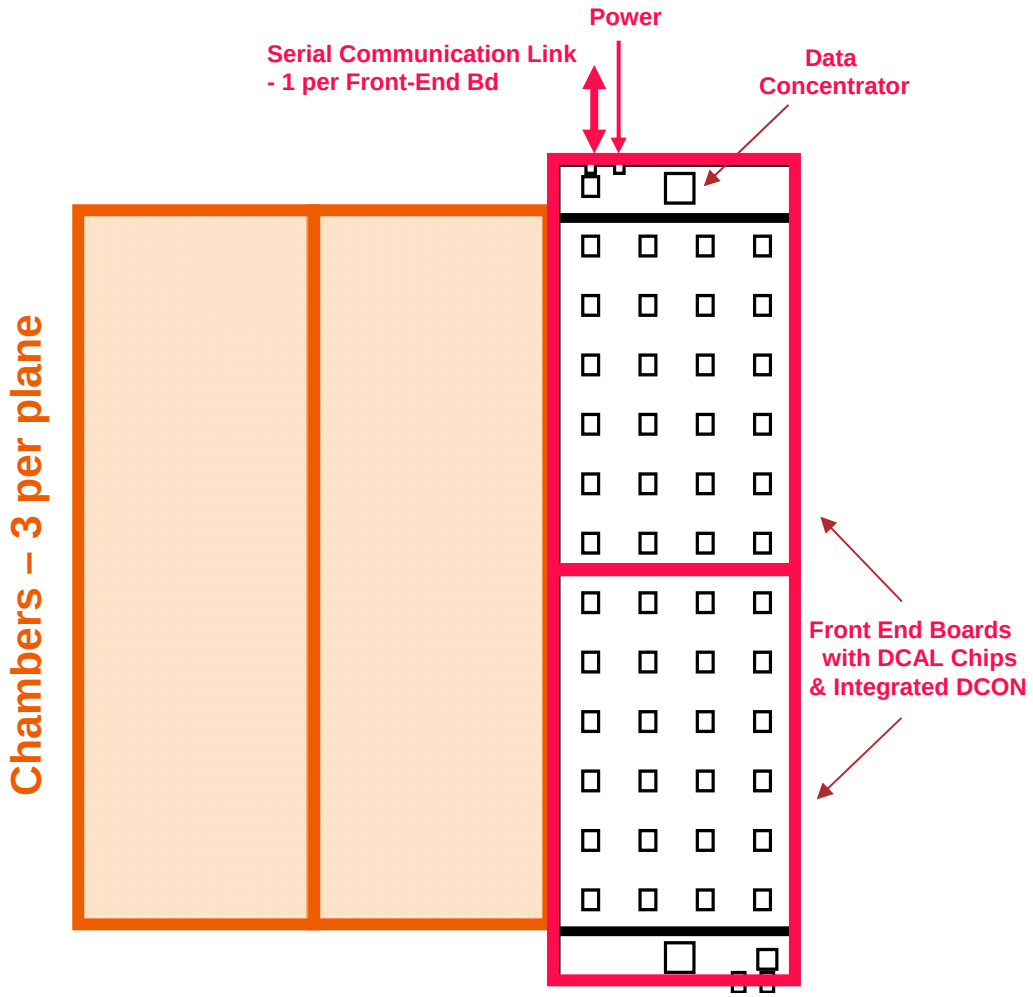
- **Design of Front-End Board**
  - Challenging design
    - *Via holes on pads not allowed*
      - 2 choices
        - *Blind/buried vias*
        - *2 boards glued together*
      - ⇨ Chose 2 boards glued together
    - *Simultaneous digital signals (continuous serial streams), through feed-throughs of low-level charge signals*
      - Must have all digital signals differential
      - Careful isolation & control of digital and analog grounds
  - We found a susceptibility for damage to FEB from Chamber Sparking
    - *Fixed using grounding and shielding techniques*
      → System Grounding Plan





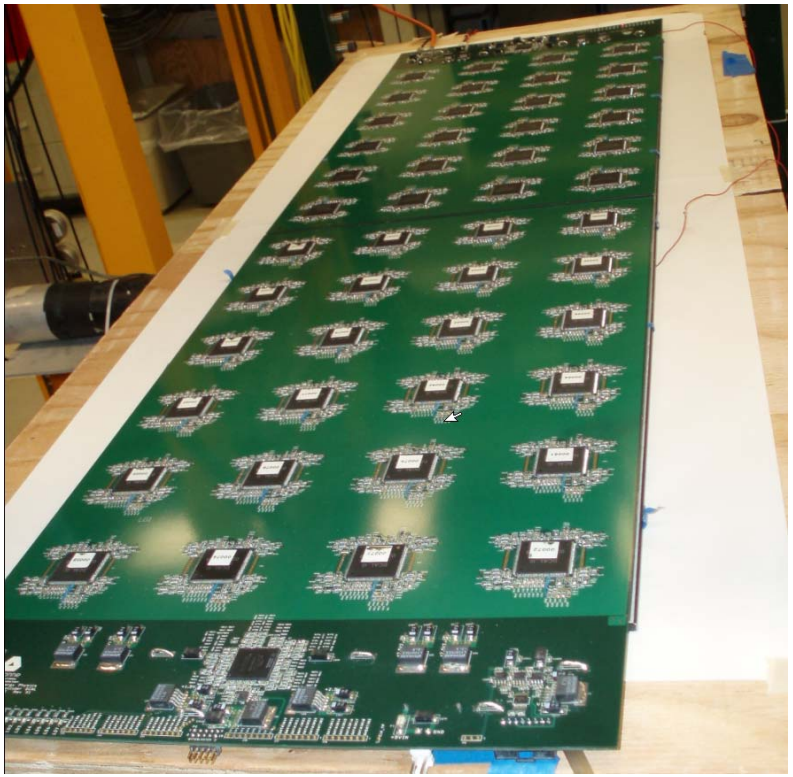


System Physical Implementation (Cont.)



Square Meter Plane

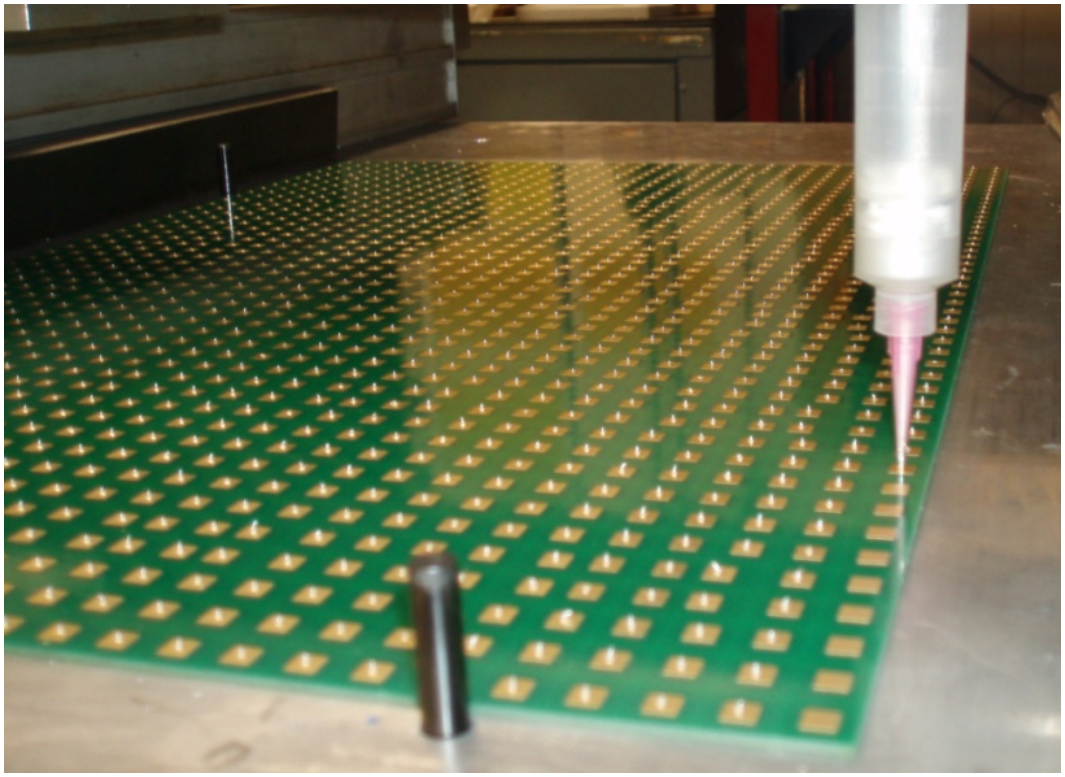
(2) 32 cm X 48 cm Front End Boards per Chamber



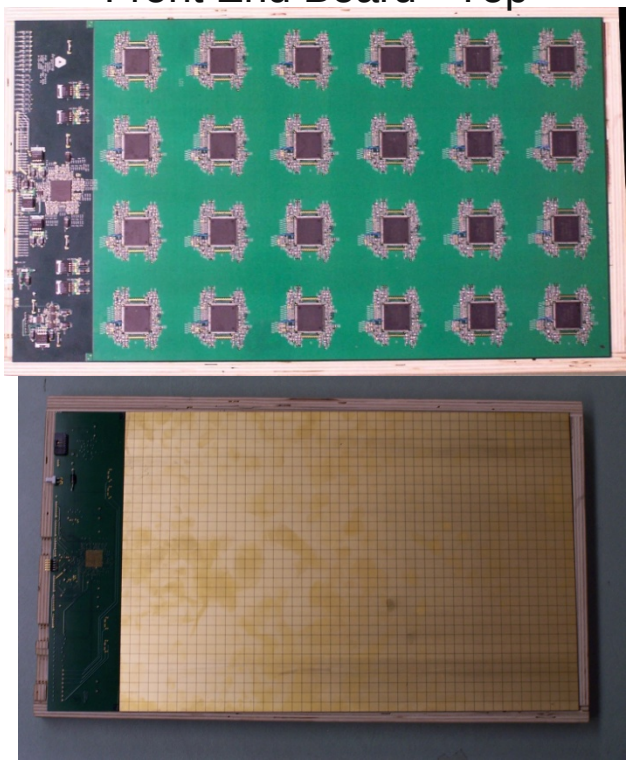
- Front End Board
  - (24) 64-Ch Chips / Bd
  - 1536 Channels / Bd
  - 2 boards/chamber

System Physical Implementation (Cont.)

- Pad Boards
  - Glued to Front End Board using Conductive Epoxy
  - Gluing done by robot, after FEB assembly and check out
  - Cured in oven

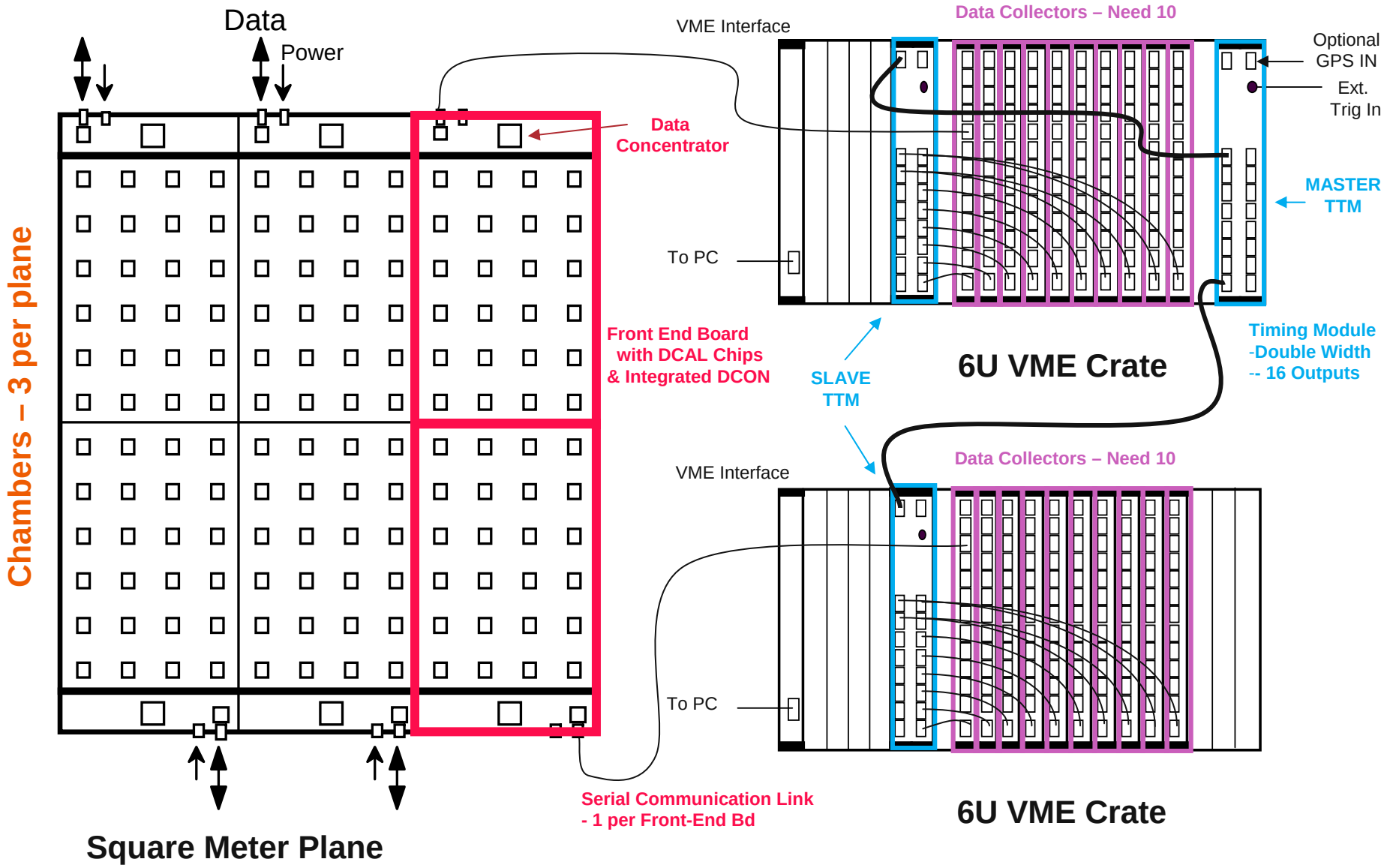


Front End Board - Top



Pad Board - Bottom

System Physical Implementation (Cont.)

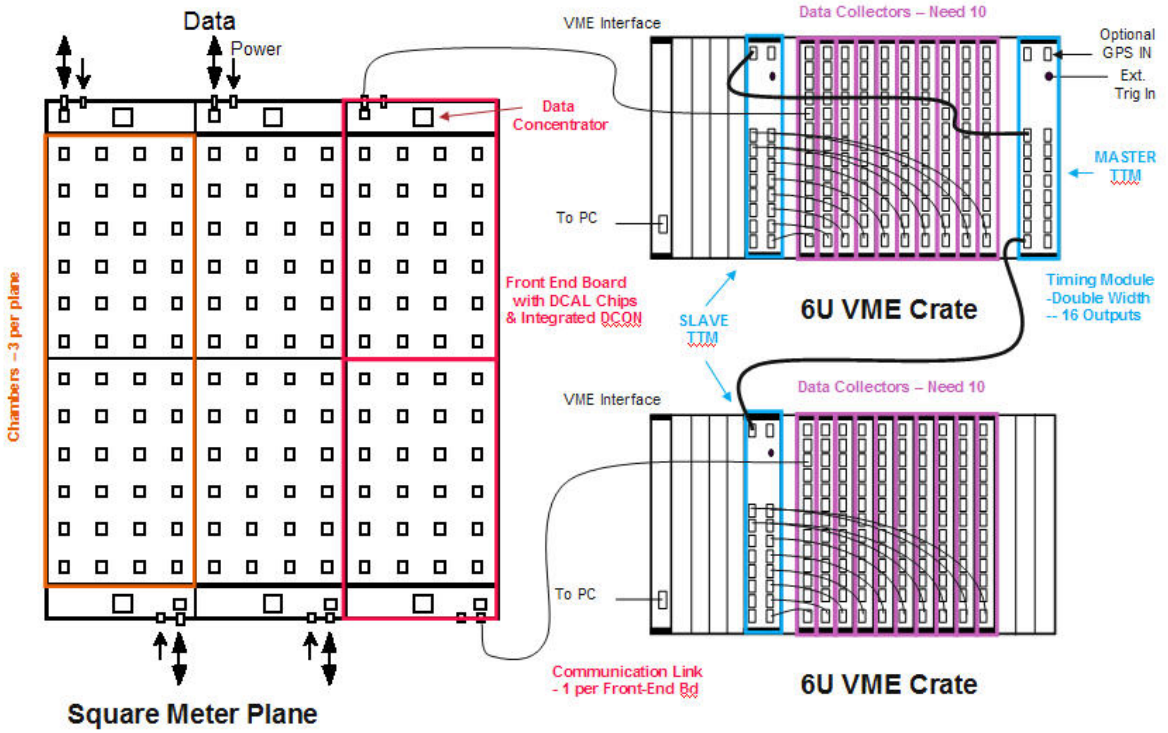


System Physical Implementation (Cont.)

- Square meter plane mounted on cassette using prototype Front End Boards

Some Numbers

- Planes
  - 38 + 14 planes
- Detector Granularity
  - 1 cm^2 pads
  - 10,000 pads/plane
  - **480,000 ch total**
- Front End Boards
  - 6 per plane
  - **312 total (+ spares)**
- Chips
  - 64 ch/chip
  - 24 chips/FEB
  - **7488 chips total**
- Data Collectors
  - 12 FEB/Data Coll.
  - **28 Data Coll. total**
- VME Crates
  - **3 crates total (1 per side + Tail Catch)**



- **Chip Rates (@ 1 TS/trig)**
  - 1 bit/100 nSec out of chips
  - 121 bits/TSlice
    - *64 hit bits → 8 bytes*
    - *24 bits timestamp → 3 bytes*
    - *3 ctrl bit/byte*
  - 12.1 uSec/TS/Chip
  - 24 chips operate in parallel
  - **→ 82.6 KHz max average event rate**
  - Use Zero Suppression…
- **DCON Output Rates**
  - 16 bytes/TSlice/chip
  - 25 nSec/nibble
  - → 12.8 uSec/TSlice/chip
  - **78 K Tslices/sec max rate**
  - Zero Suppression helps
  - Example:
    - *4 chips hit/event avg*
    - *Max event rate: 19KHz*
  - **WC: 78 K / 24 = 3.2 KHz**

Power Distribution System

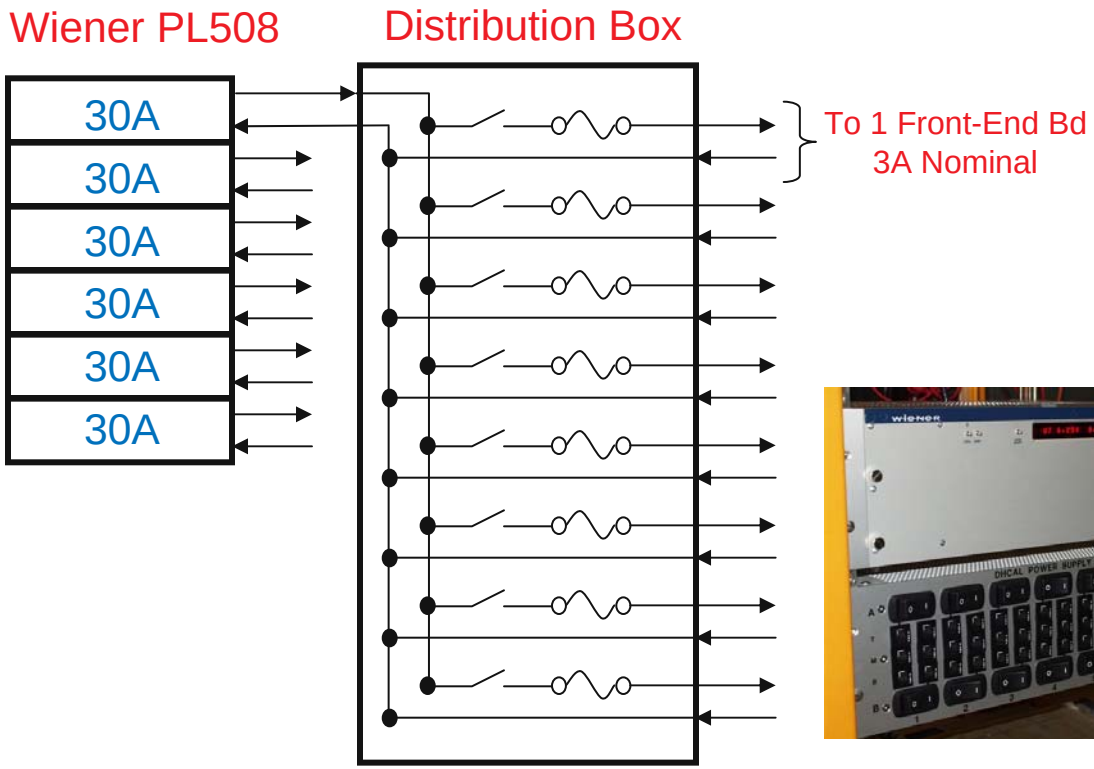
- **Cubic meter detector power requirements:**
  - 3A / FEB @ 5V
  - 40 planes * 6 FEBs/plane * 3.0 amps/FEB = 720 amps at 5V
- **Solution:**
  - 5 Wiener PL508 chassis
  - Each PL508 has six independent 5V at 30 amp subunits
  - 5 PL508 * 6 PS/PL508 * 30 amps/PS = 900 amps total ampacity
  - Operate at ~80% of capacity
  - 1 Wiener sub unit powers 8 Front End Boards

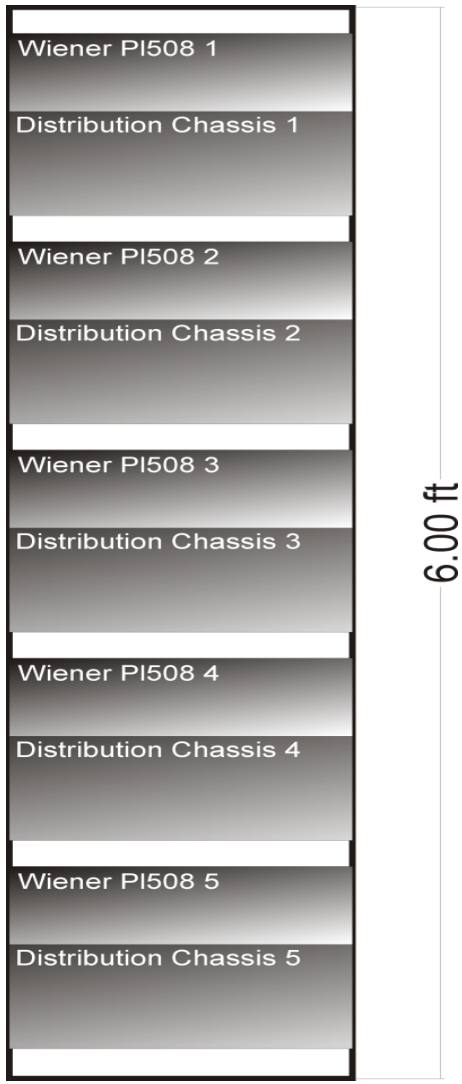
- **Power Numbers**
  - 100 mA/ASIC @ 2.5V
  - 3.9 mW/ch
  - 3A/FEB @ 5V (ASICs run at 2.5V)
  - 15W/FEB
  - 90W/plane
  - 3.6 KW/cubic meter

⇨ *Not designed for Low Power…*

Power Distribution System (Cont.)

- Need Power Dist. Box to distribute voltages to Front End Boards
- Rack Configuration
  - Power supplies will fit into one rack
- Power Distribution
  - Custom distribution boxes, with fuses, safe wiring, etc.





Production Quantities

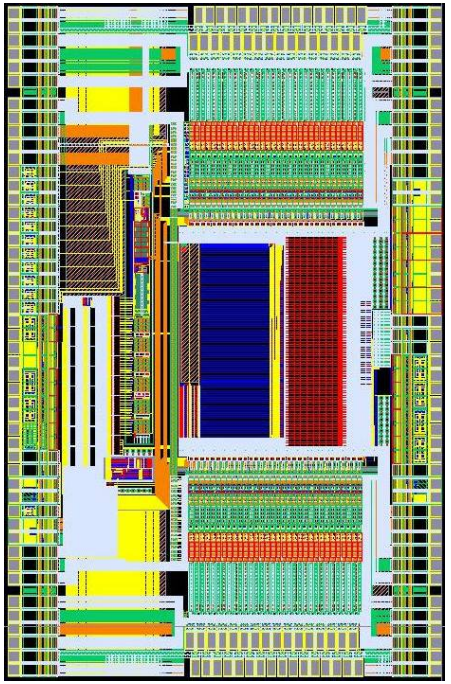
Item	Needed for Cubic Meter	Needed for Tail Catcher	Spares	Teststands	Total
DCAL Chips	5472	1008	2164	0*	8644
Front End Bds	228	42	54	0*	324
Data Collectors	20	4	3	1	28
VME Crates	2	1	1	1	5
VME Processors	2	1	1	1	5
Timing Module	3	1	2	3	8
Wiener Power Supplies	5	2	1	0	8
Power Dist. Boxes	5	2	1	0	8

* Use Prototypes

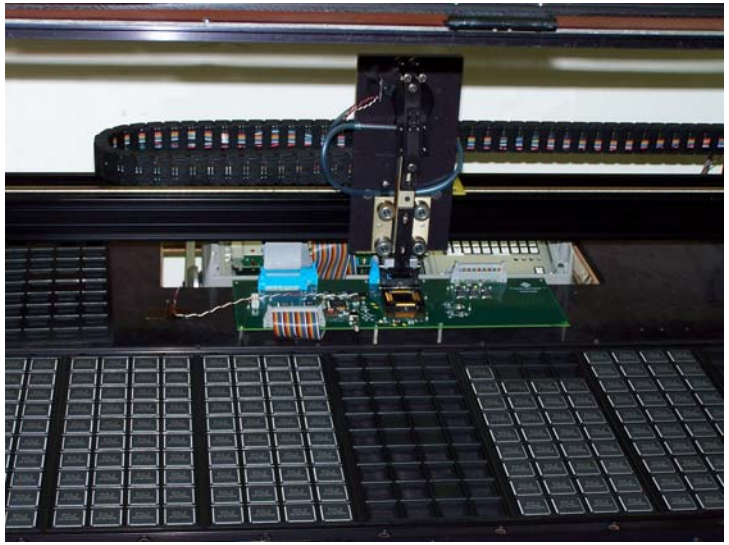
Summary of System Components Production

Summary of DCAL3 Production

- **Chip Fabrication:**
  - 11 wafers, 10,300 chips fabricated
  - Packaging 176-pin, 24mm x 24mm LQFP (ASAT)
- **Chip Testing**
  - All chips tested using robotic tester at Fermilab
  - Results:
    - *8644 good parts → 84% yield → ~Average yield*
    - *1 bad wafer → 25% yield → Did not use*



DCAL3 Layout



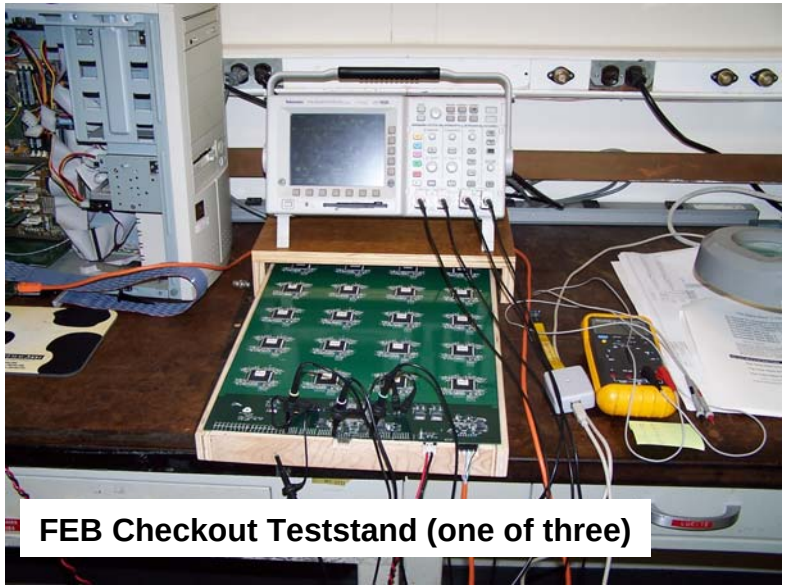
Robotic Chip Tester

Chip Storage (~1/2 total)

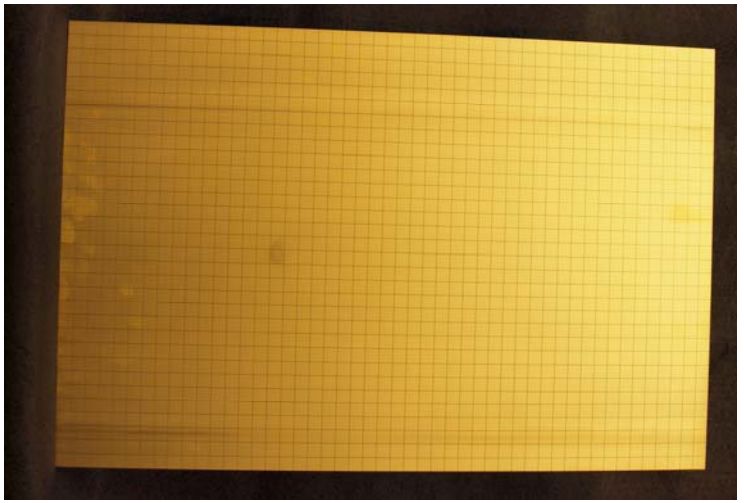
Fermilab

Summary of Front End Board Production

- **Front End Board Production**
  - Fabricated 280 + 80 boards
    - *100% yield → No rejects*
  - Assembly 260 + 64 boards
    - *100% yield → No rejects*
  - Testing
    - *215 passed 1st time, 65%*
    - *108 bad & repaired → 33%*
    - *6 bad & not repaired → 1.8%*
- **Pad Board Production**
  - Fabricated 280 + 80 boards
    - *10 rejects – Damage in shipping*
  - Assembly 260 + 64 boards
    - *No rejects*
  - Gluing
    - *~10 rejects – gluing mistakes*

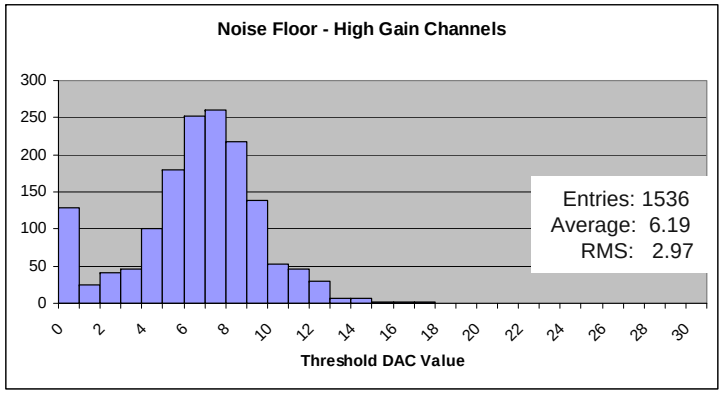


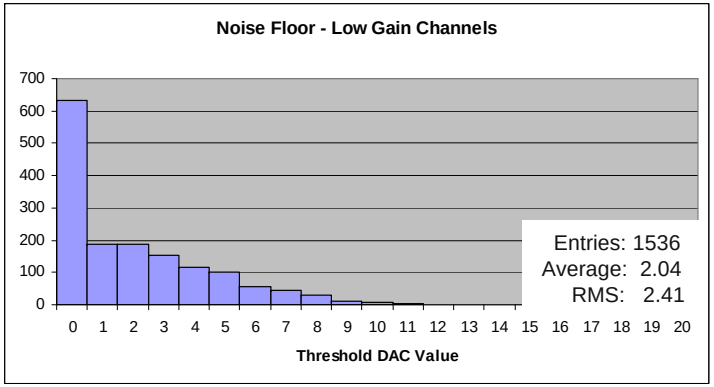
FEB Checkout Teststand (one of three)



Status of Front End Board Production (Cont.)

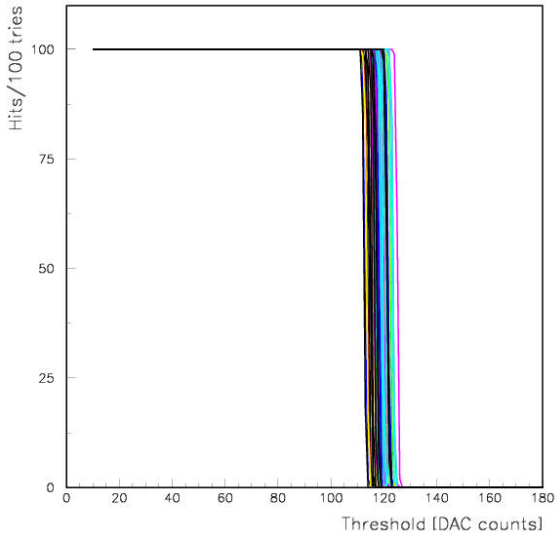
A Few Results



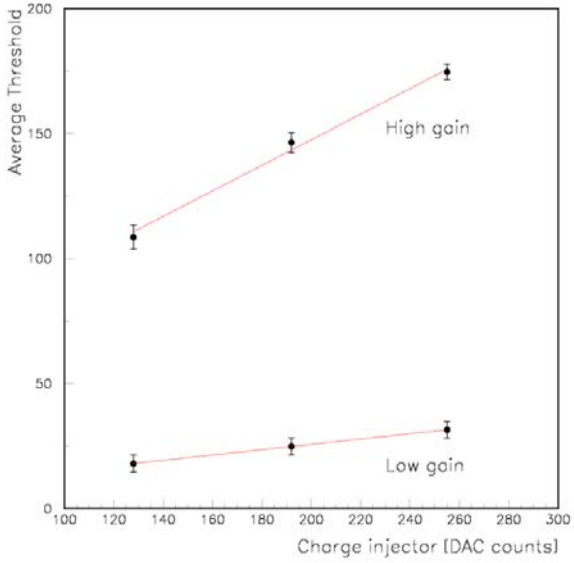


Measurements of Noise Floor
Single channel measurements, 24 Ch FEB
Ext. Trig, No Pad Bd, No Chamber, No HV
Entire Front End Board, 1536 Channels

⇨ Analysis of Production Data in Progress…



Channel Uniformity for Threshold Scans Using On-board Charge Injection



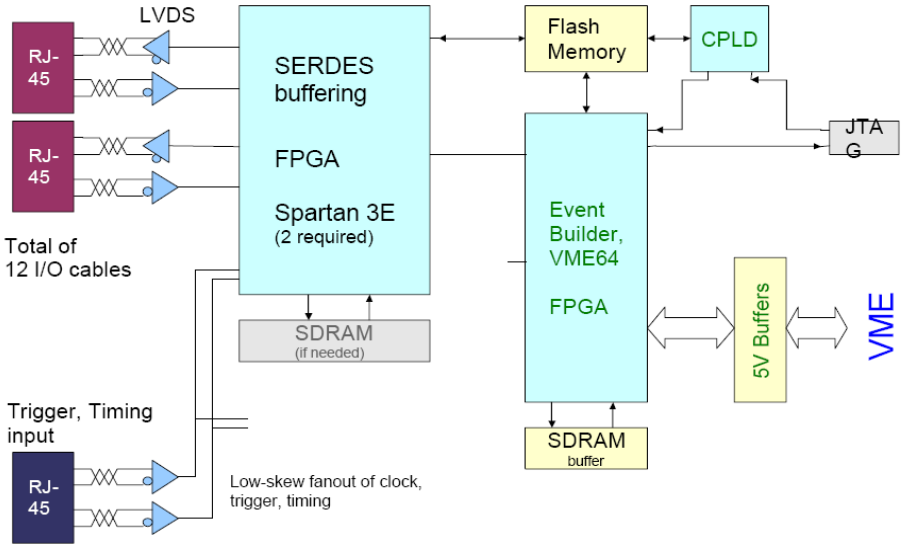
High Gain:
~0.3 fC / THR_DAC_CNT
→ 75 fC Range

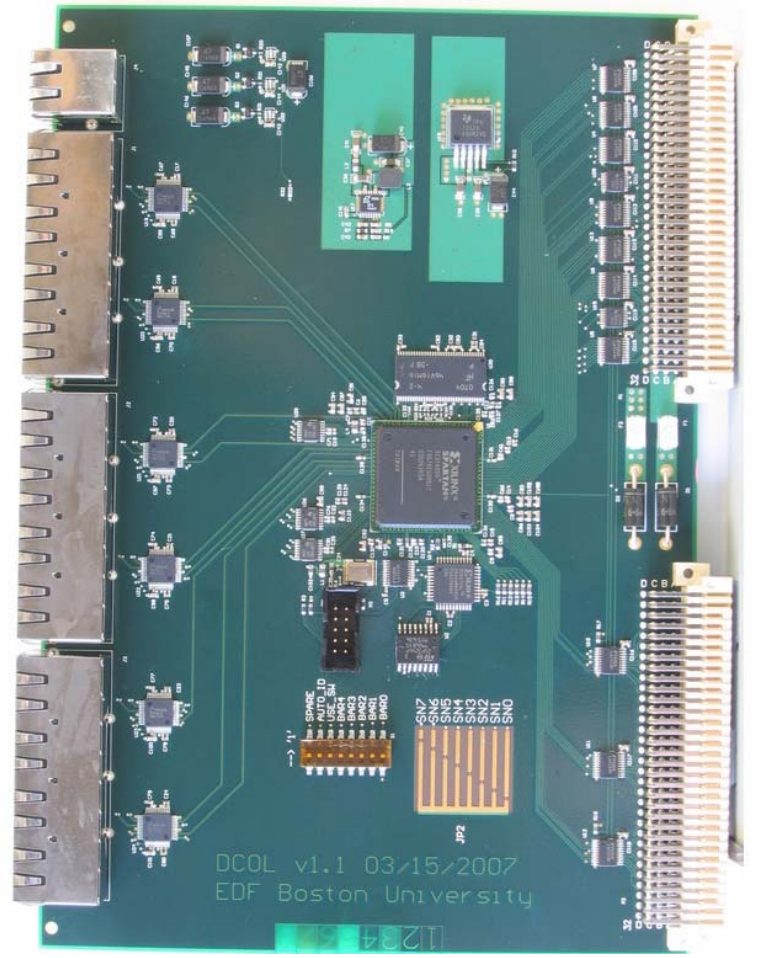
Factor of 6.4

Low Gain:
~1.9 fC / THR_DAC_CNT
→ 480 fC Range
→ Operate ~ 190 fC for RPC

Summary of Data Collector Production

- **Production**
  - 1st run: 38 boards fabricated & assembled, delivered to Argonne
  - 2nd run: 35 fabricated and assembled; testing in progress

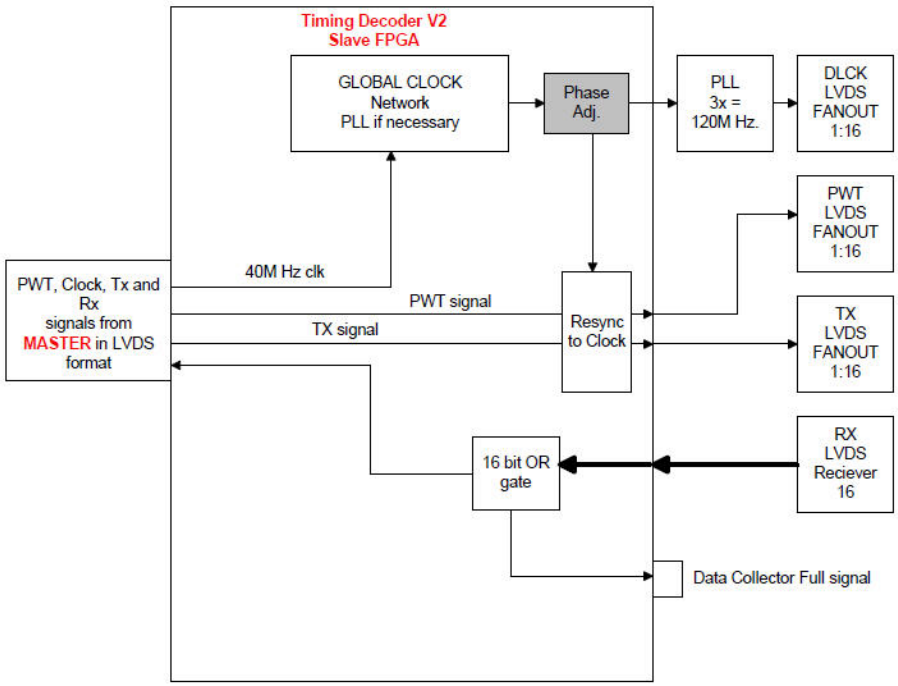


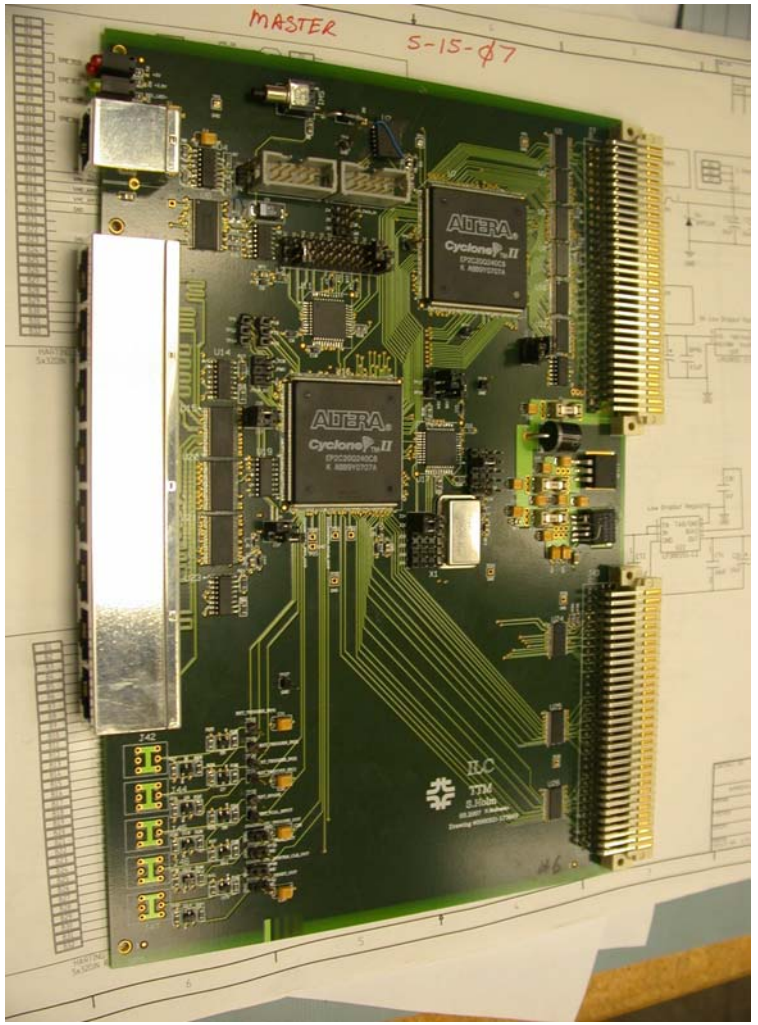


Courtesy Eric Hazen, BU

Summary of Timing & Trigger Module (TTM) Production

- Production
  - 11 boards fabricated
  - 6 boards assembled & checked out to date
  - Configurable
    - *Master (source of signals)*
    - *Slave (crate distribution)*





Fermilab

Summary of Electronics Performance on Detector

- First Run – Oct., 2010
  - 3 failures of front-end boards
  - ~20-30 chips observed to go dead randomly through the course of a run
    - *Believed to be due to heating*
    - *Added additional fans for subsequent runs*
- Second Run – February, 2011
  - No failures of front-end boards
  - ~12 bad chips in detector; stable number
  - 1 power supply failure – fuses were fast blow → changed to slow blow
- Third run – April, 2011
  - No failures of front-end boards
  - ~16 bad chips in detector; stable number
  - 1 power supply failure; swapped; cause under investigation

Summary

- **We have completed an extensive development program for the DCAL Read-out**
  - The design of the Front End Board was by far the most difficult aspect of the project
  - The prototype system has been thoroughly tested
    - *Good electronics noise performance → Careful layout & circuit design*
    - *Good measurement of cosmic rays*
    - *Data error rate < 1E-12 → through extensive testing*
- **Production, installation, & commissioning completed**
  - DCAL ASICs
    - *10,300 chips fabricated → 84% yield*
  - Front-end Board & Pad Board
    - *300 boards fabricated, assembled, & tested*
  - Data Collector
    - *38 boards fabricated, assembled, & tested; 35 more in progress*
  - Timing Module
    - *11 boards produced, 7 built & tested*
  - Power System
    - *8 units produced, based on Wiener power supply*

⇨ ***3 successful test beam runs completed***
⇨ ***Physics papers coming out***
⇨ ***Planning for next stage of R&D in progress***