

Klaus version 2.0 :

Design and Measurements

Wei Shen

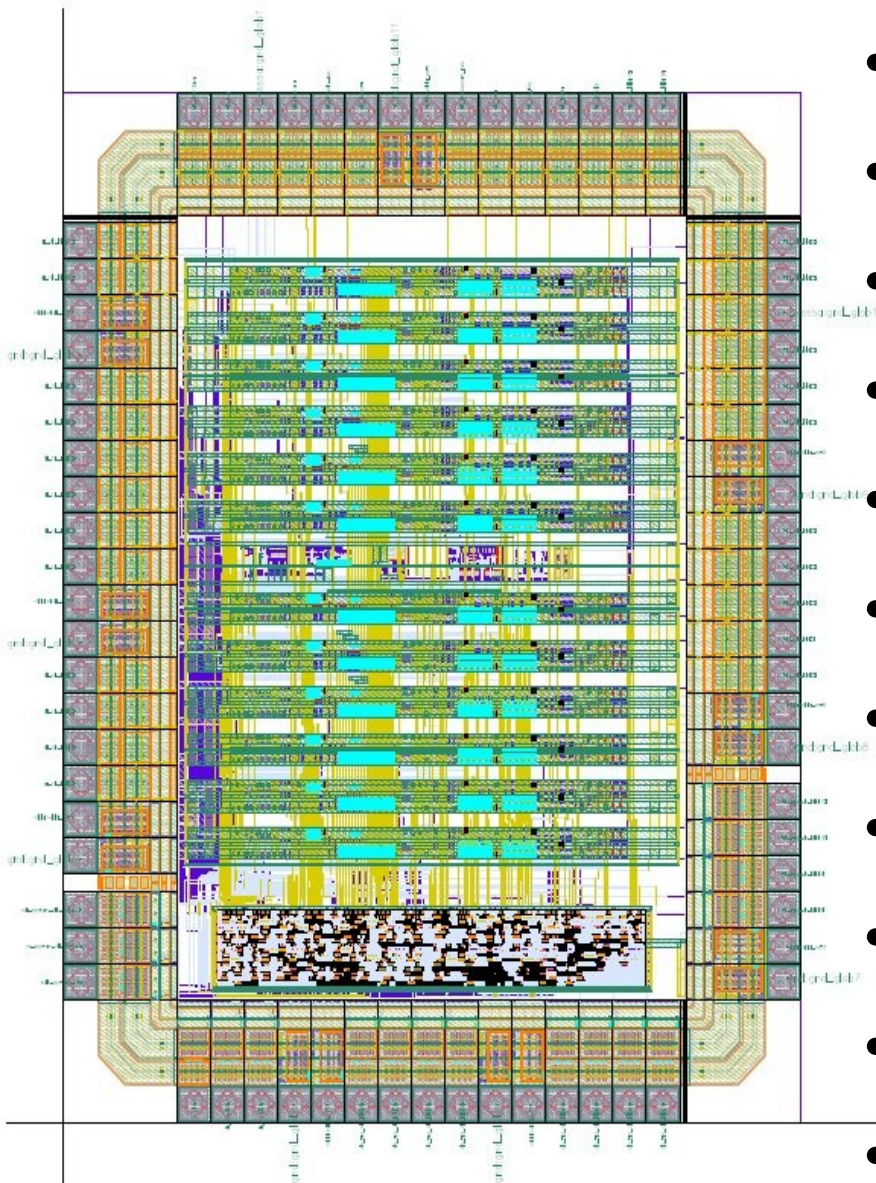
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outline

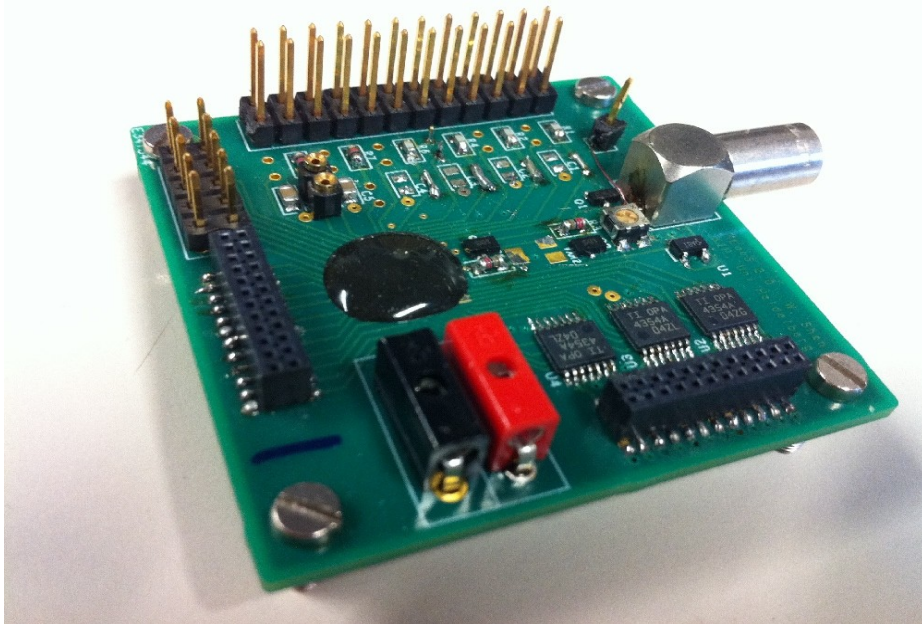
- **Chip overview**
- **Channel block**
- **Measurement results**
- **spectrum with SiPMs**
- **summary**

chip overview



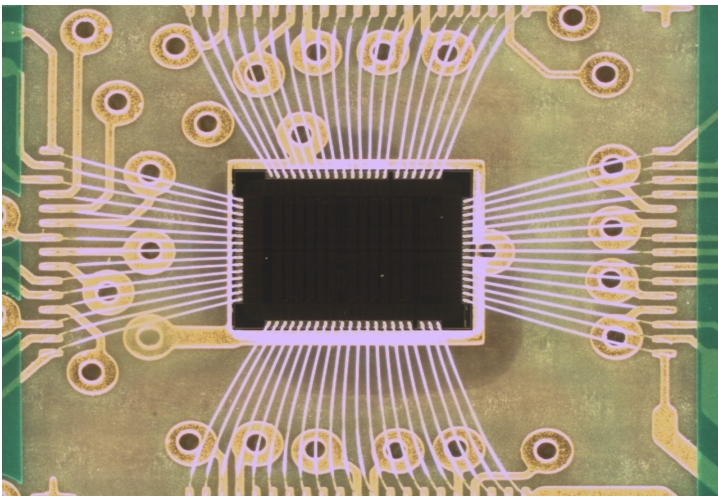
- Solution for low gain SiPM
- AMS Bicomos 350nm
- 1st version @ Oct. 2009
- 2nd version @ Nov. 2010
- Back @ Feb. 2011
- 12 channels
- Same layout width as SPIROC
- Power pulsing
- Individual analog output
- Individual trigger output
- SPI block re-designed

chip overview

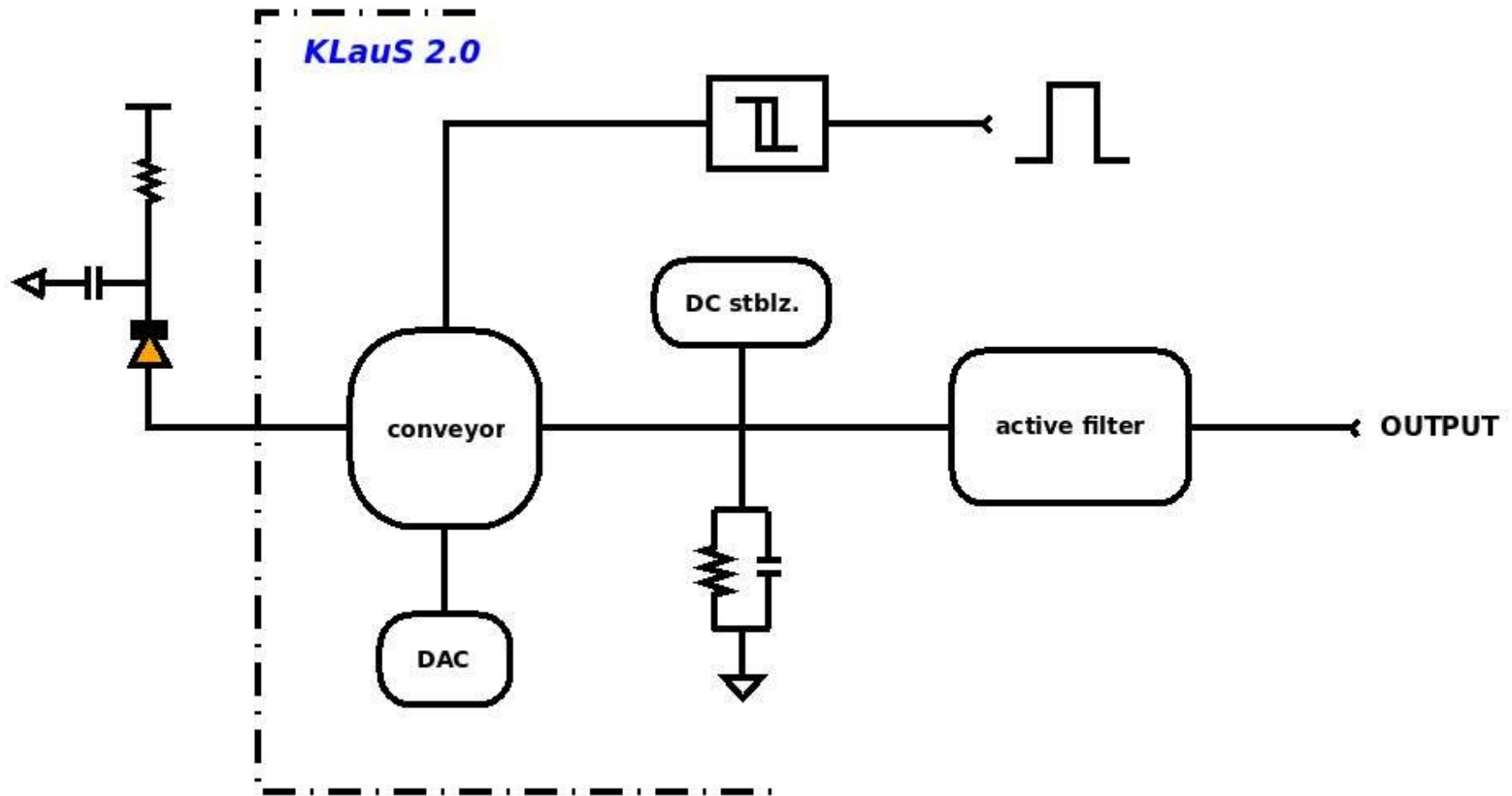


specifications

Dynamic range	20fC - 200pC
SNR	~ 10 (SiPM gain = $2.75 \cdot 10^5$)
Analog INL	$< \pm 1.5\%$
ENC	$2.5 \cdot 10^4$ @ 40pF, 50ns shaping
Time walk	$< 1\text{ns}$ @ $\frac{1}{2}$ MIP
Time jitter	$< 50\text{ps}$ @ $\frac{1}{2}$ MIP
Trigger effc.	100% @ $\frac{1}{2}$ photon electron
DAC INL	$< \pm 2\%$
DAC range	2 V
Power	$< 2\text{mW}$

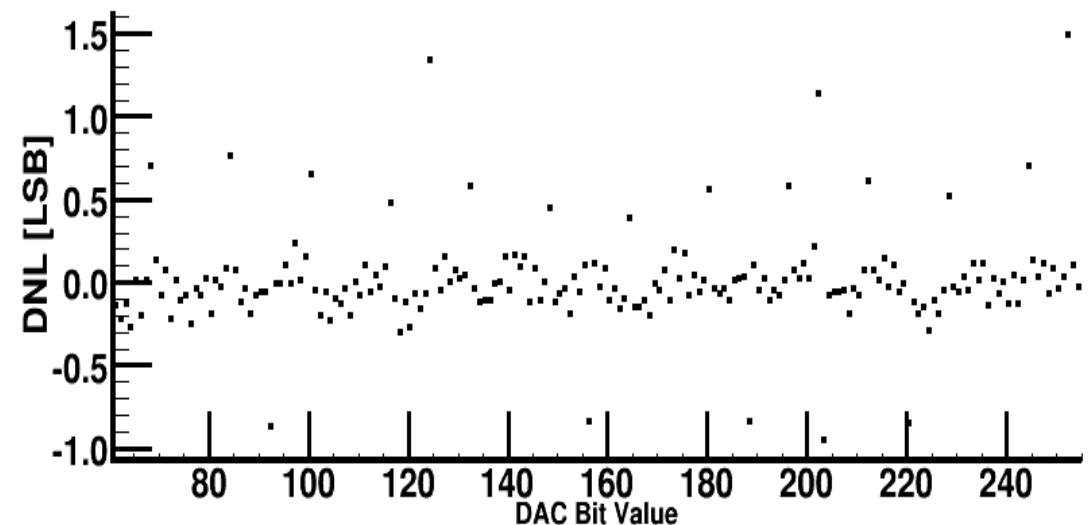
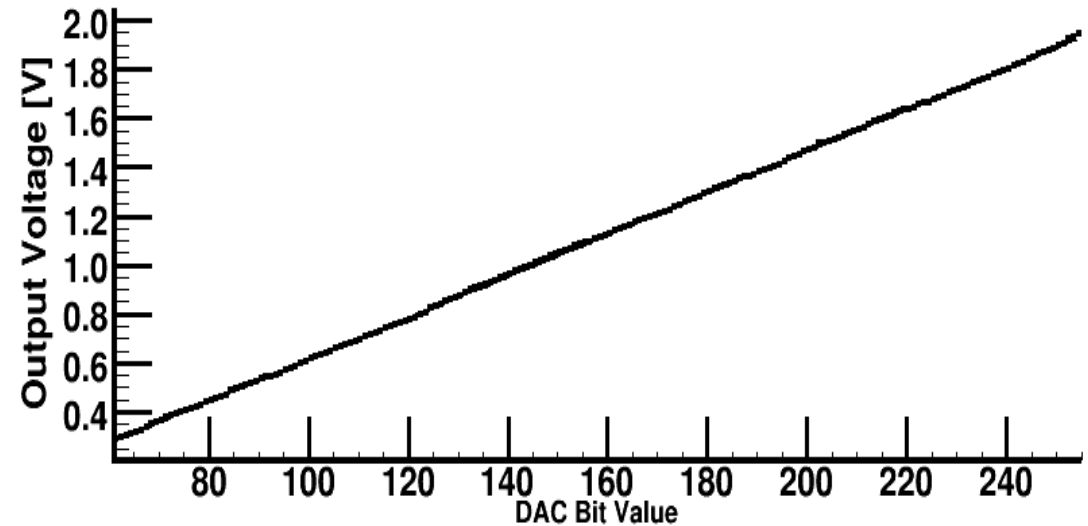


channel block

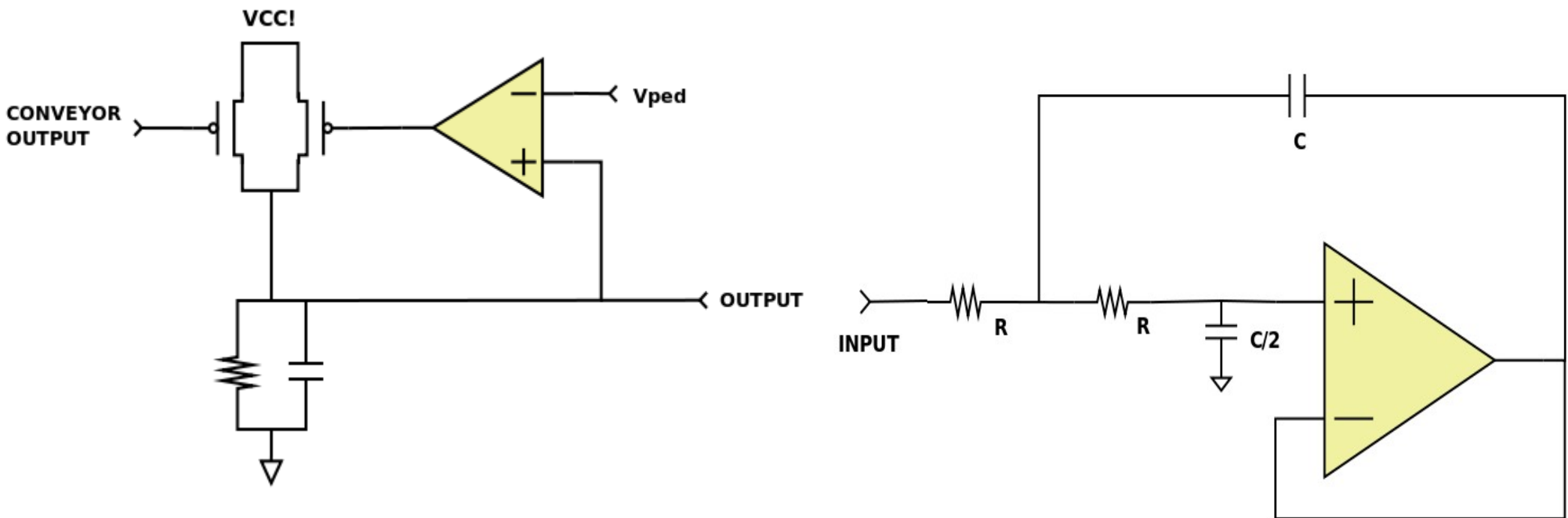


DAC - measurements

- 8 bit binary DAC
- 3.3 V CMOS
- 2V range
- $DNL < 1 \text{ LSB}$
- 10nA bias current
- Minimum voltage tuned by off-chip R



Signal processing chain



- Passive charge integration
- Pedestal stabilized with LF feedback
- Active filter adds 2 complex poles
- No undershoot

Noise

Charge injection through 33pF



Measure	P1:min(C1)	P2:rise(C1)	P3:max(C1)	P4:max(C3)	P5:freq(C2)	P6:mean(C3)	P7:delay(C3)	P8:delay(C2)	P9:---	P10:---	P11:---	P12:---
value	27 mV		1.79 V	13.9 mV	--	2.57 mV	46.015 ns	--				
mean	25.2 mV		1.7955 V	13.545 mV	--	2.4251 mV	44.66813 ns	--				
min	4 mV		1.78 V	11.2 mV	--	1.25 mV	-184.239 ns	--				
max	37 mV		1.82 V	18.5 mV	--	3.75 mV	66.336 ns	--				
sdev	4.8 mV		4.5 mV	687 μ V	--	375.8 μ V	9.12830 ns	--				
num	1.311e+3		1.311e+3	1.311e+3	0	1.311e+3	1.311e+3	0				
status	✓		✓	✓	⚠	✓	✓	⚠				

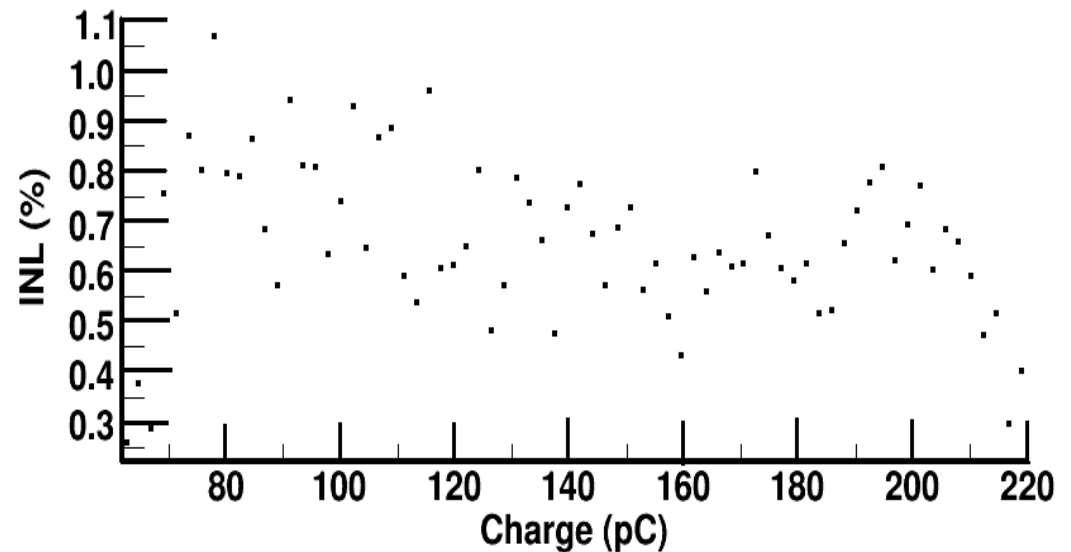
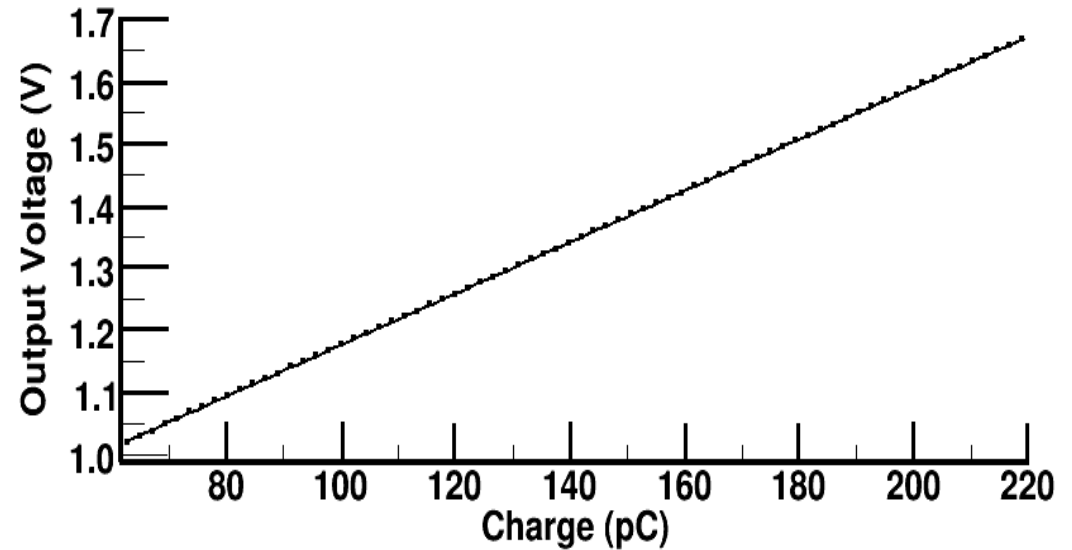
C1 DC50
500 mV/div 5.00 mV/div
0 mV offset -15.60 mV

Timebase -300 ns Trigger C1 DC
100 ns/div Stop 950 mV
40.0 kS 40 GS/s Edge Negative

- SNR > 10
- Output V 9mV
- Noise 800 μ V
- ENC $2.4 * 10^5 e^-$

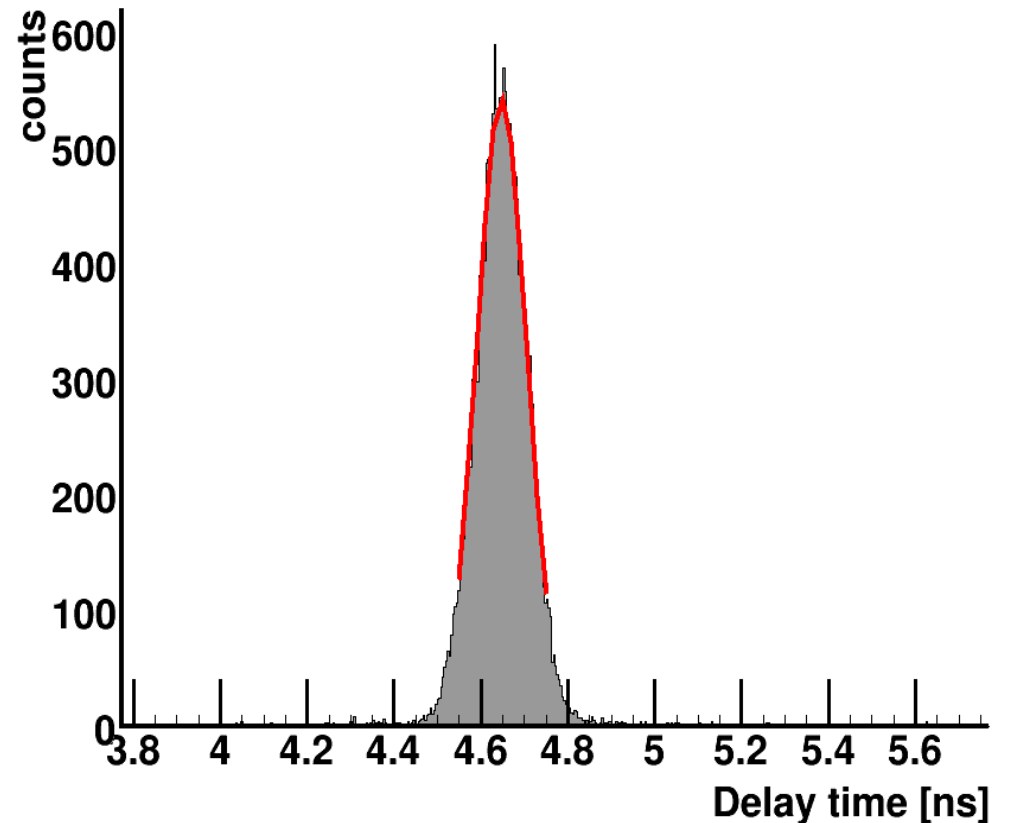
Dynamic range

- Gain setting
1, 10, 40
- INL varies @
different DAC
- $INL < \pm 1.5\%$



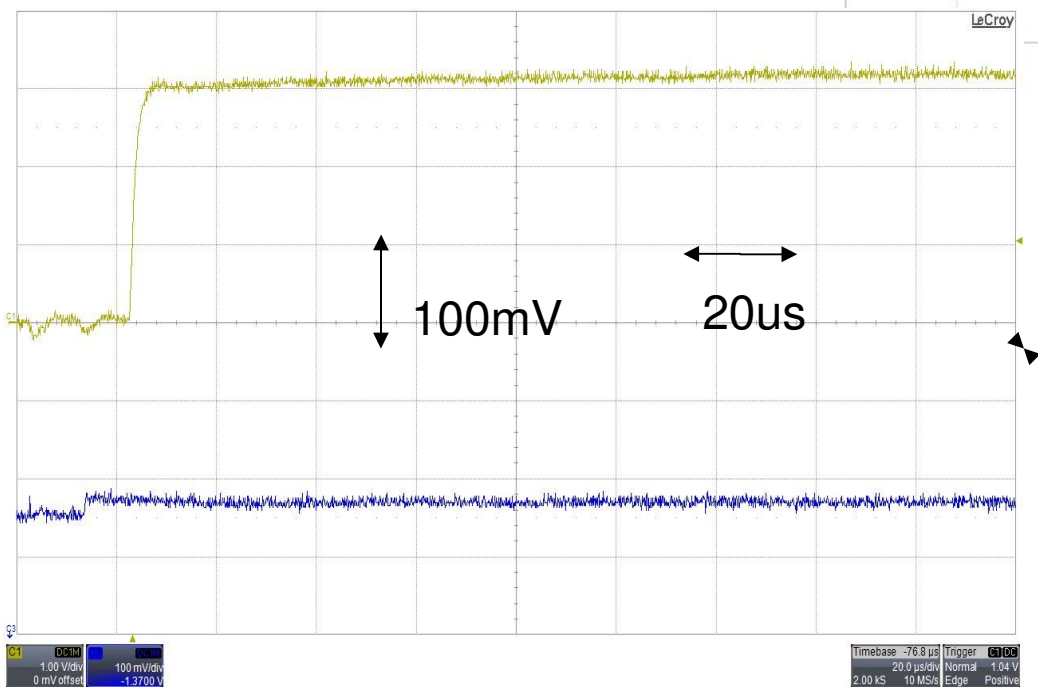
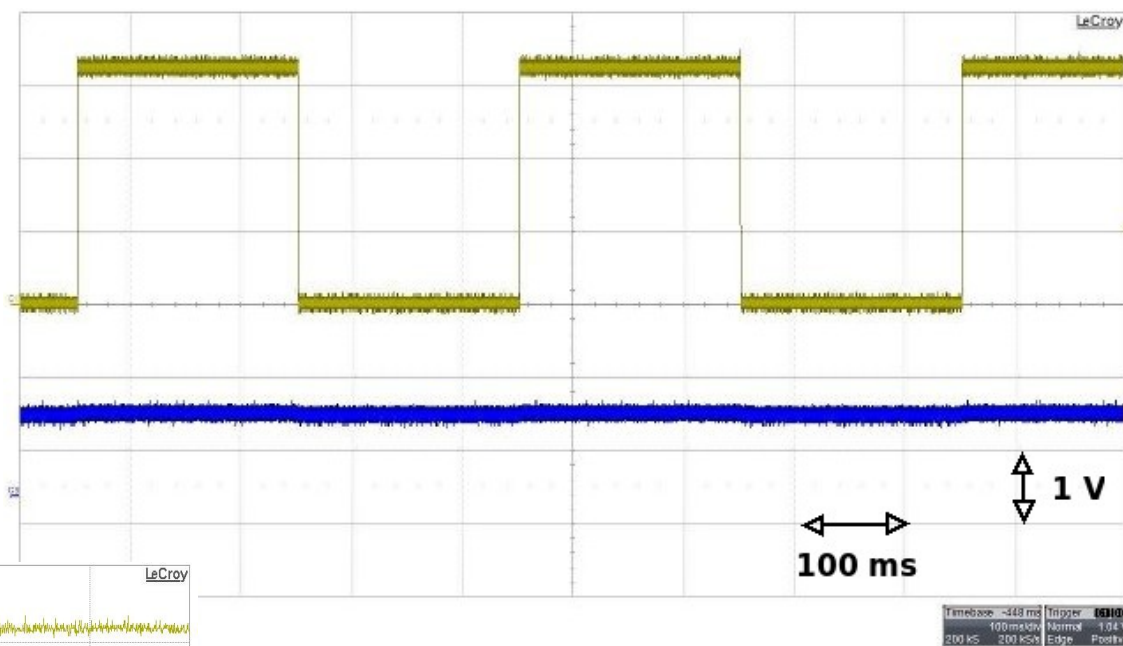
jitter

- MIP : 52ps @ 0.5 MIP
- 15 pixel (gain $2.75 \cdot 10^5$)
- Threshold with off-chip poti
- DACs available
within NEW ASIC
- Effic. 100% @ 0.5 p.e.
- Walk < 1ns @ 0.5 MIP



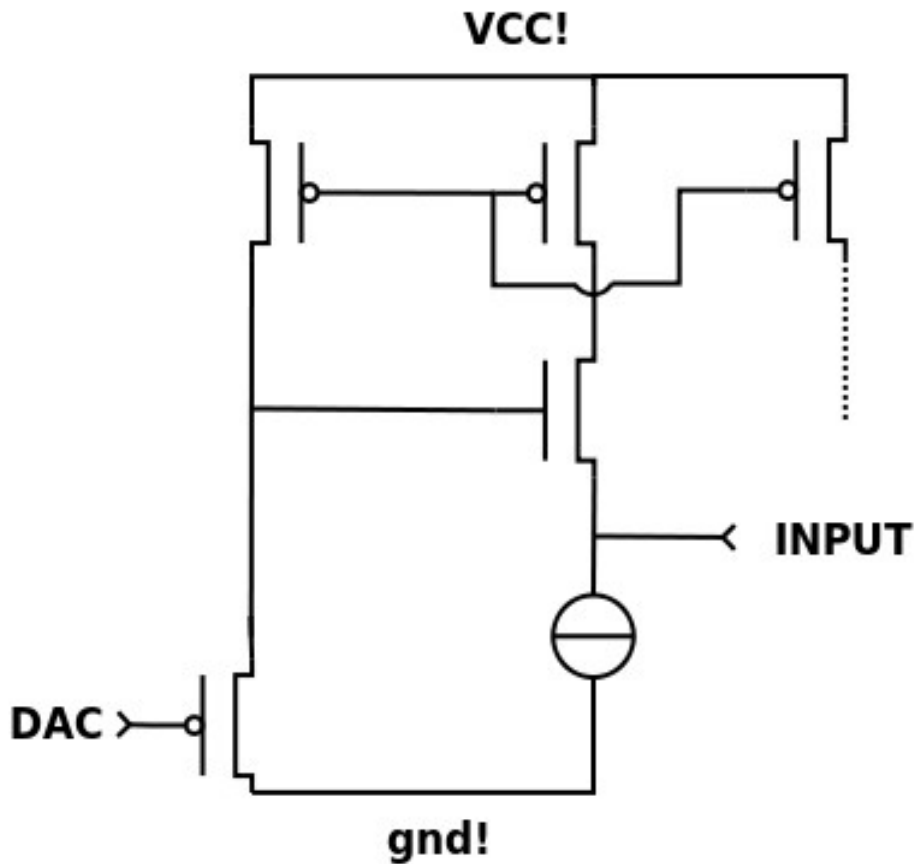
Power pulsing

Input voltage during power pulsing



- ✓ Voltage difference $< 20\text{mV}$
- ✓ 1-2% SiPM overvoltage
- ✓ 20us recovery time

Power pulsing

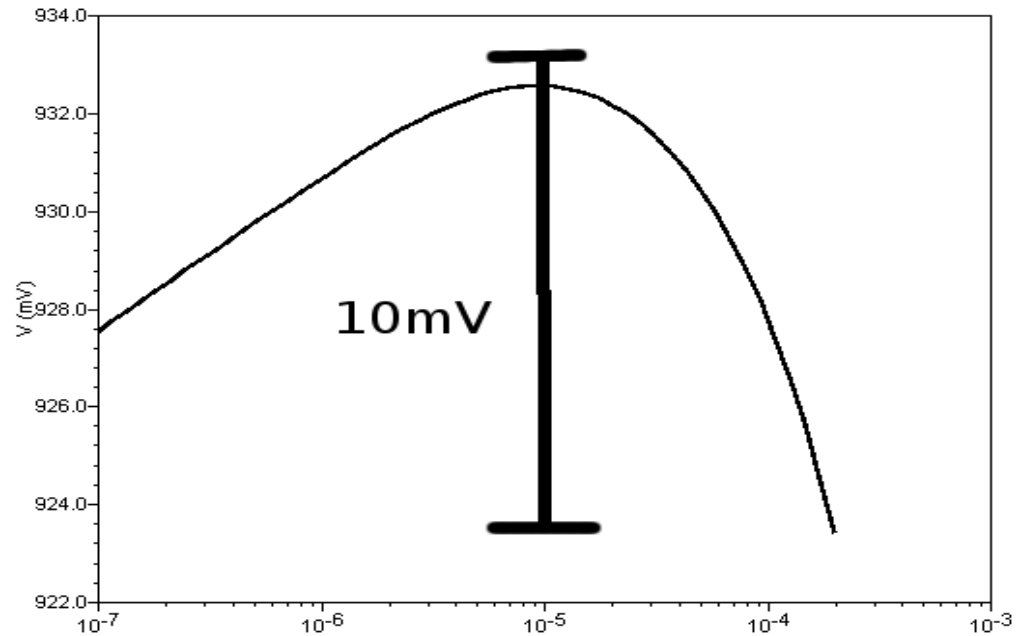


SPICE simulation

Input voltage remains fixed at different bias current due to input stage feedback

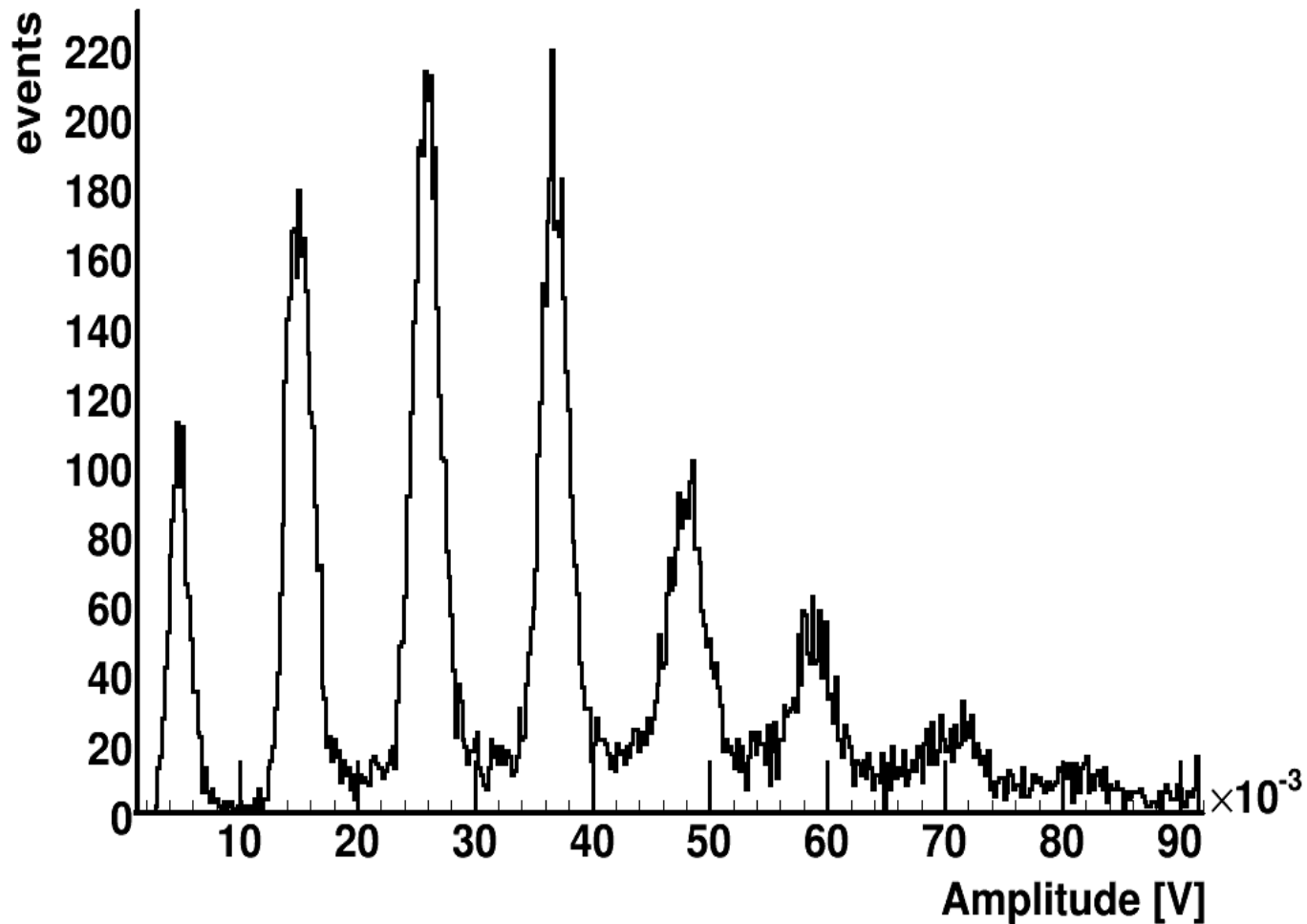
Power off, bias current off

Voltage @ input pin



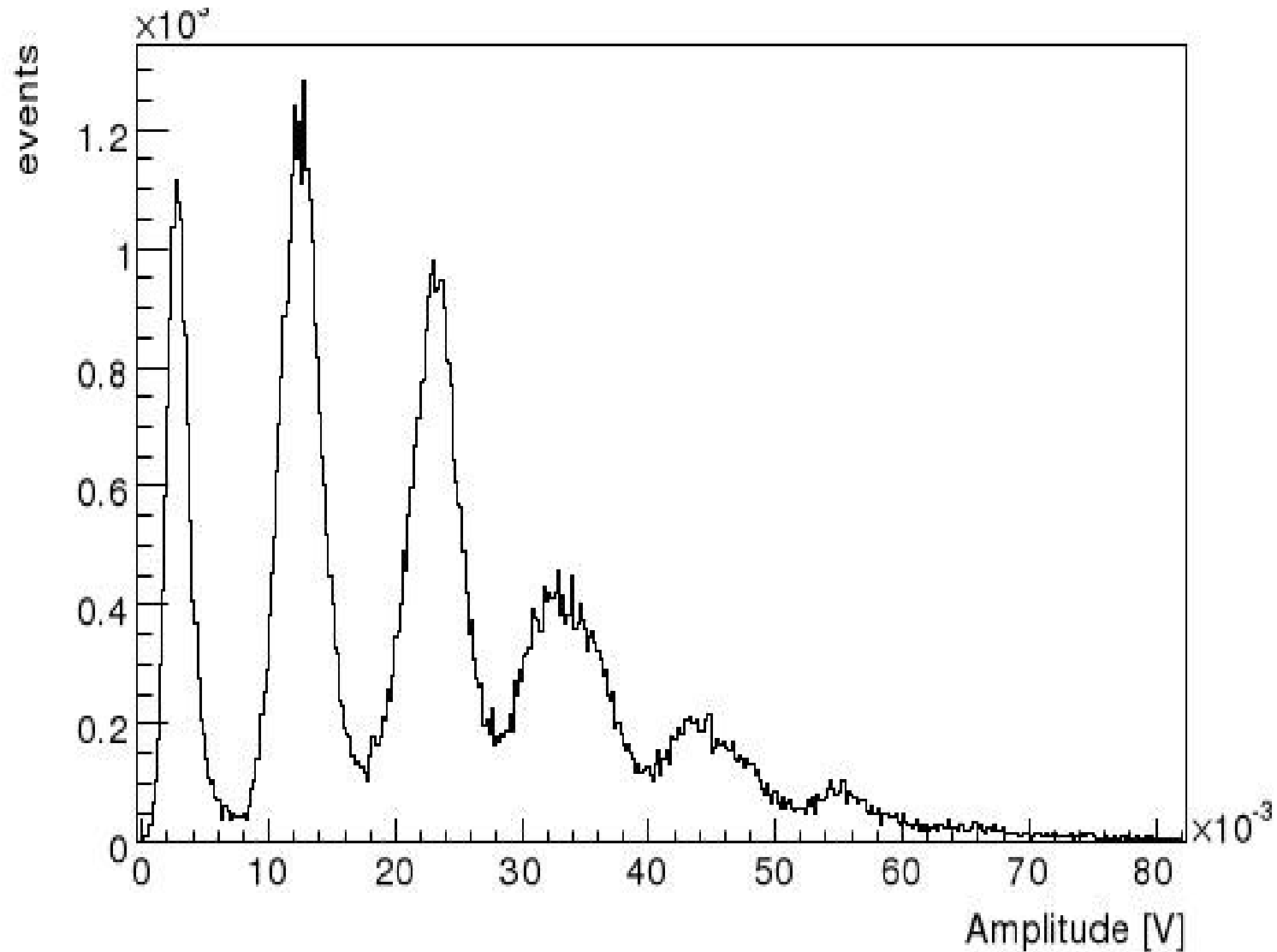
SiPM spectra

MPPC 1600pxl 25um @ nominal voltage



SiPM spectra

CPTA SiPM @ low overvoltage



summary

Summary

KlauS2v0 is functional, performance similar to simulation results

functional with different SiPMs

SNR > 10 for low gain SiPM

jitter ~ 50 ps for MIP signal

Outlook

more results on uniformity, power pulsing

possible integration into SPIROC