KlauS version 2.0 :

Design and Measurements

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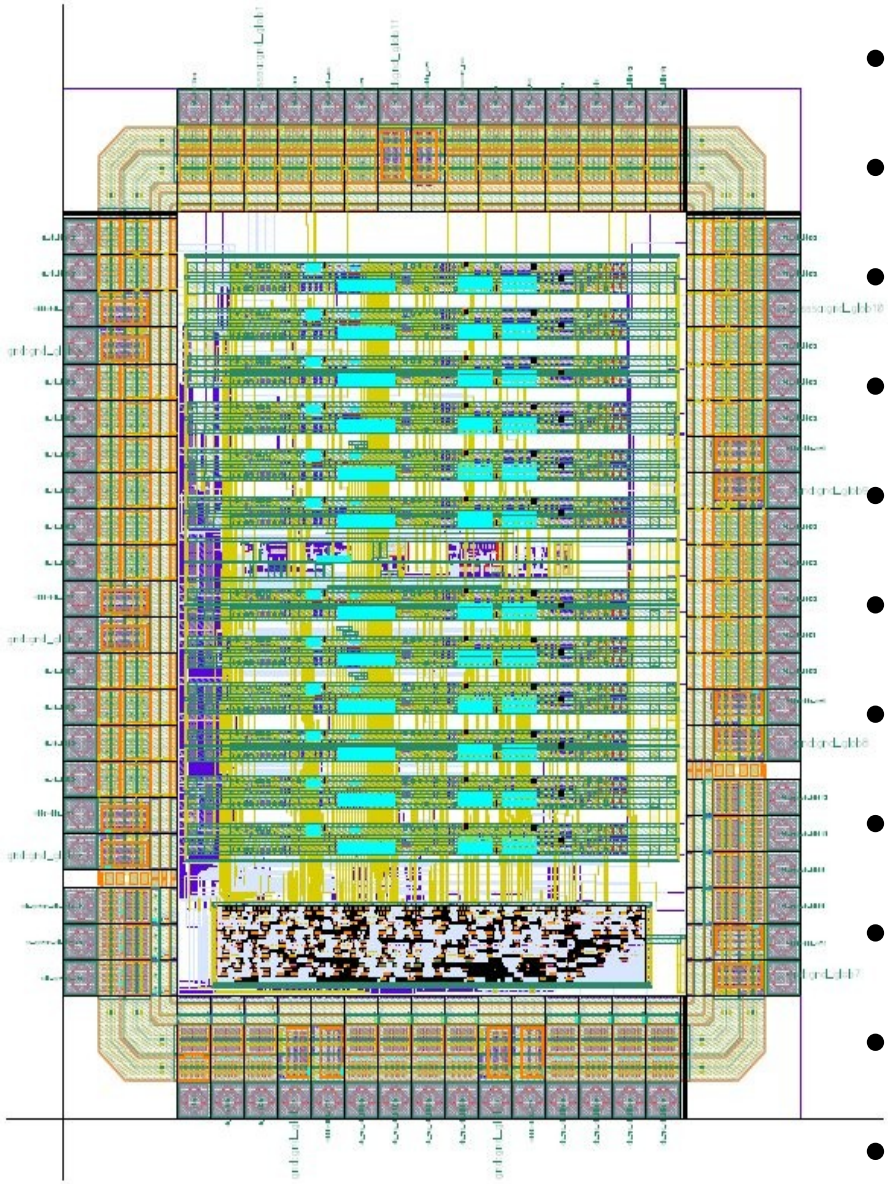
outline

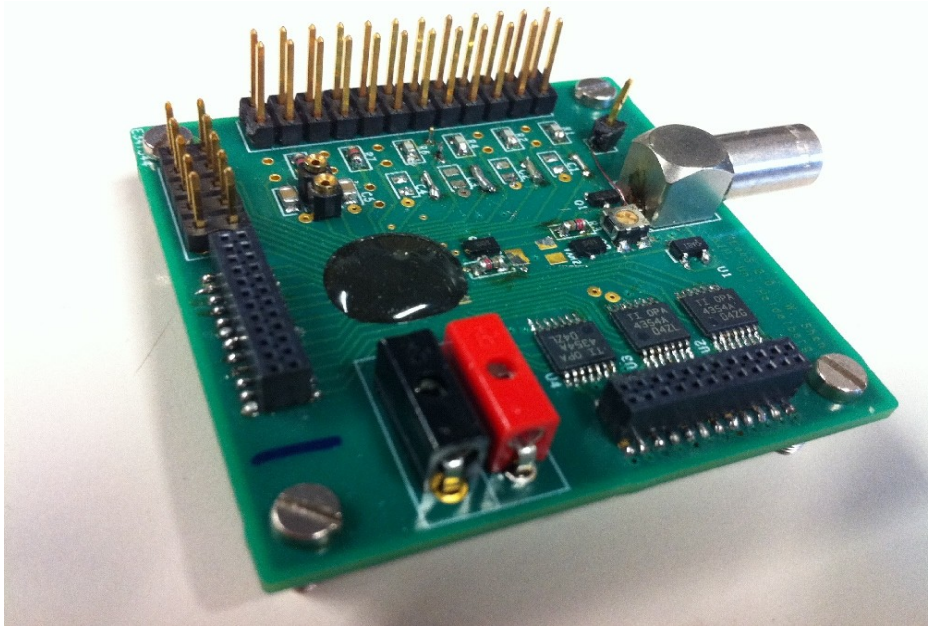
- Chip overview
- Channel block
- Measurement results
- spectrum with SiPMs
- summary

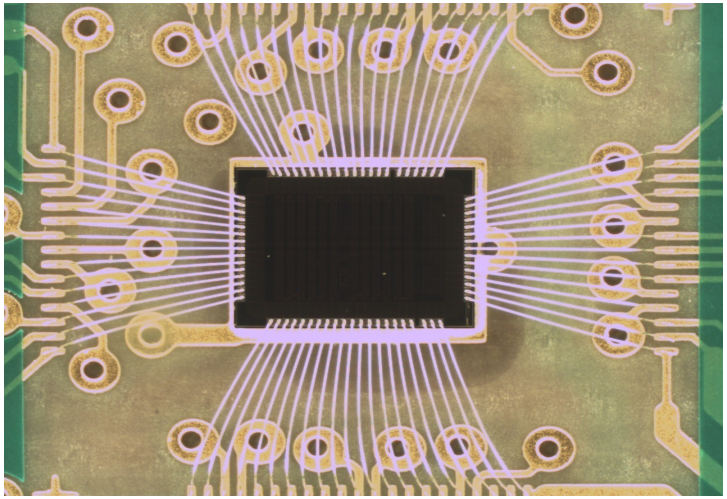
chip overview



- Solution for low gian SiPM
- AMS Bicmos 350nm
- 1st version @ Oct. 2009
- 2nd version @ Nov. 2010
- Back @ Feb. 2011
- 12 channels
- Same layout width as SPIROC
- Power pulsing
- Individual analog output
- Individual trigger output
- SPI block re-desgined

chip overview

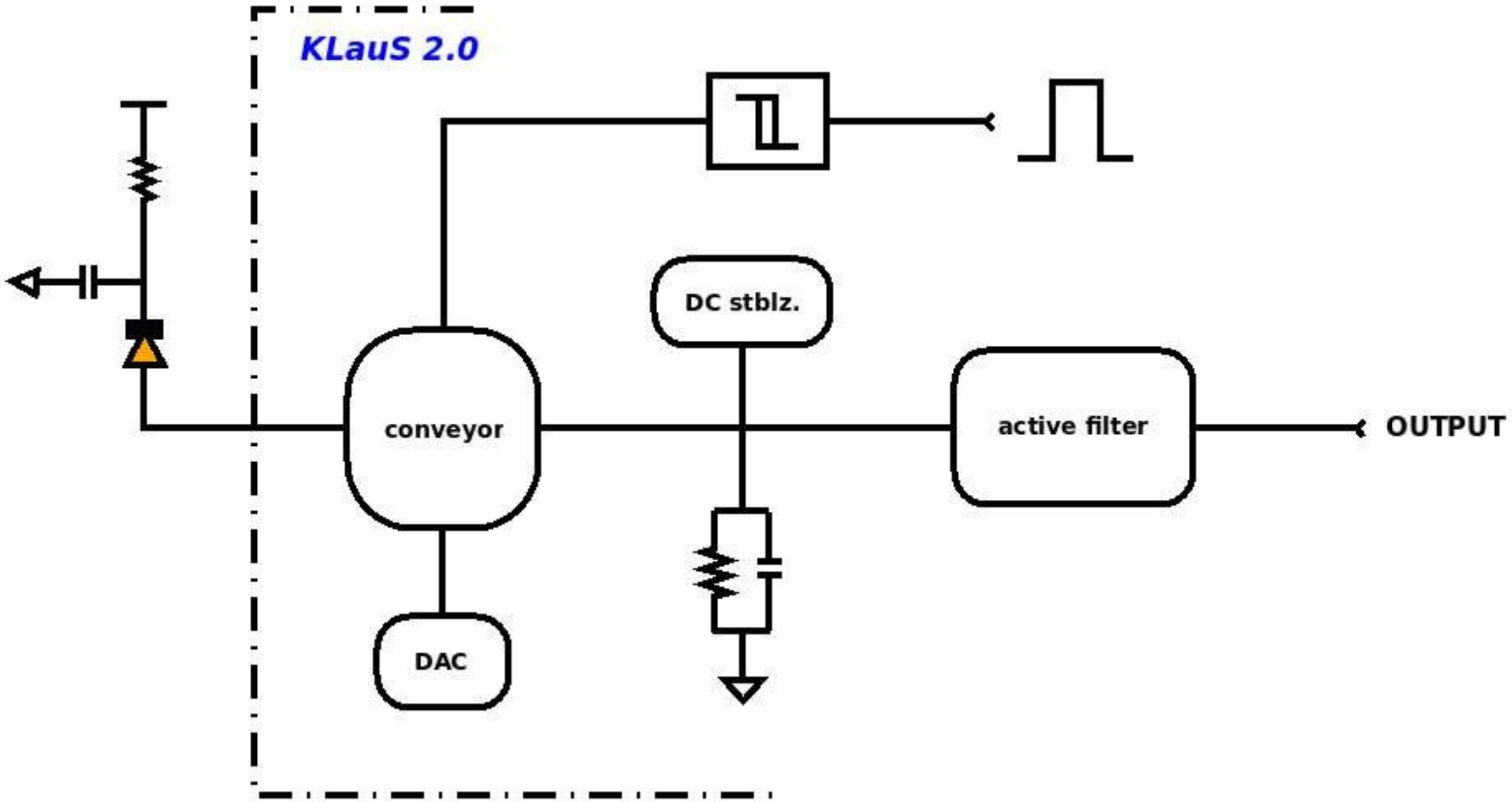




specifications

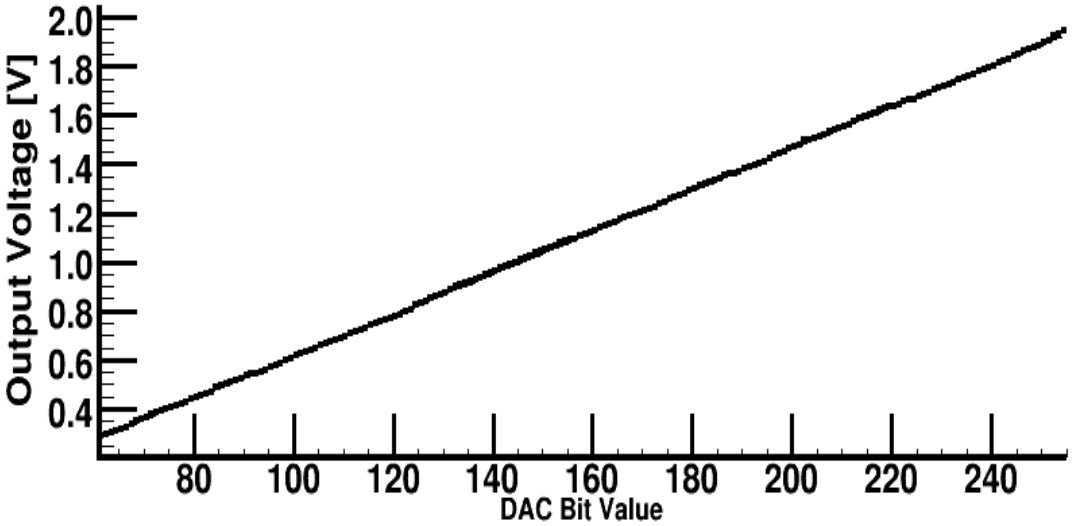
Dynamic range	20fC - 200pC
SNR	~10 (SiPM gian= $2.75*10^5$)
Analog INL	< ±1.5%
ENC	$2.5*10^4$ @ 40pF, 50ns shaping
Time walk	< 1ns @ ½ MIP
Time jitter	< 50ps @ ½ MIP
Trigger effc.	100% @ ½ photon electron
DAC INL	< ± 2%
DAC range	2 V
Power	< 2mW

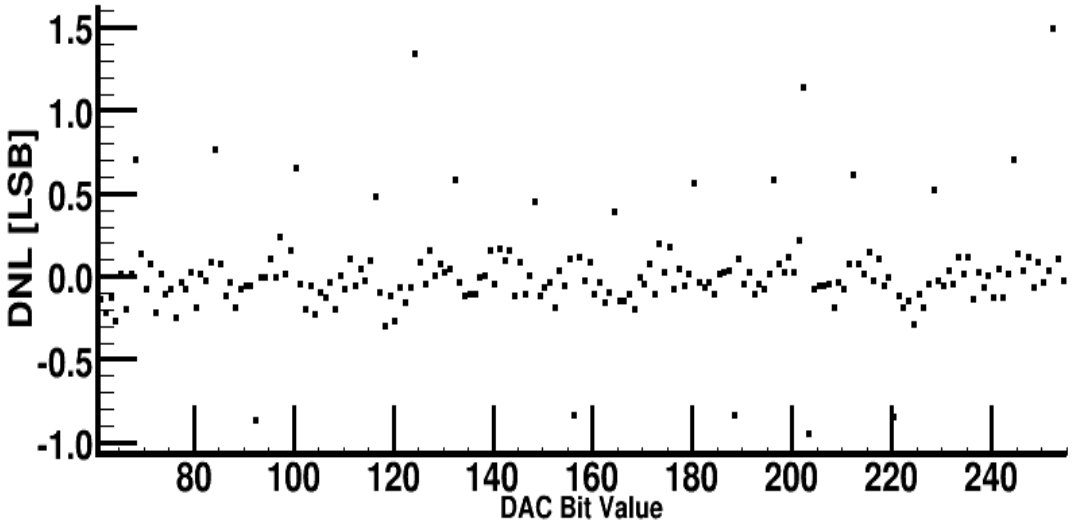
channel block



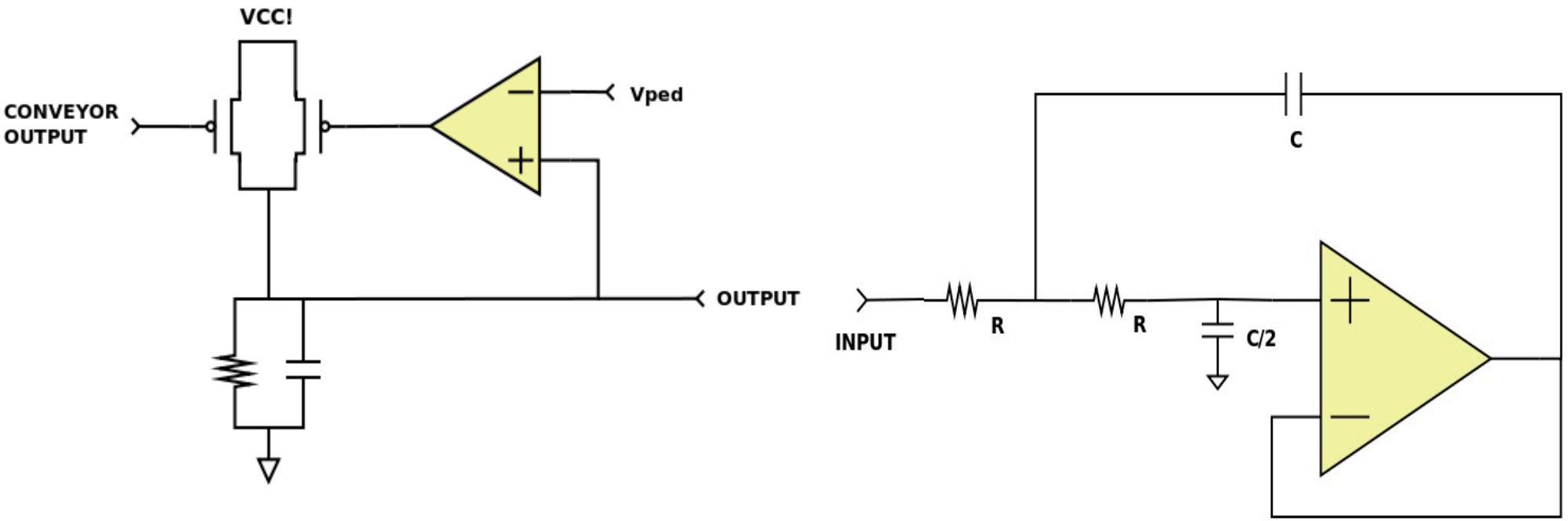
DAC – measurements

- 8 bit binary DAC
- 3.3 V CMOS
- 2V range
- DNL < 1 LSB
- 10nA bias current
- Minimum voltage tuned by off-chip R





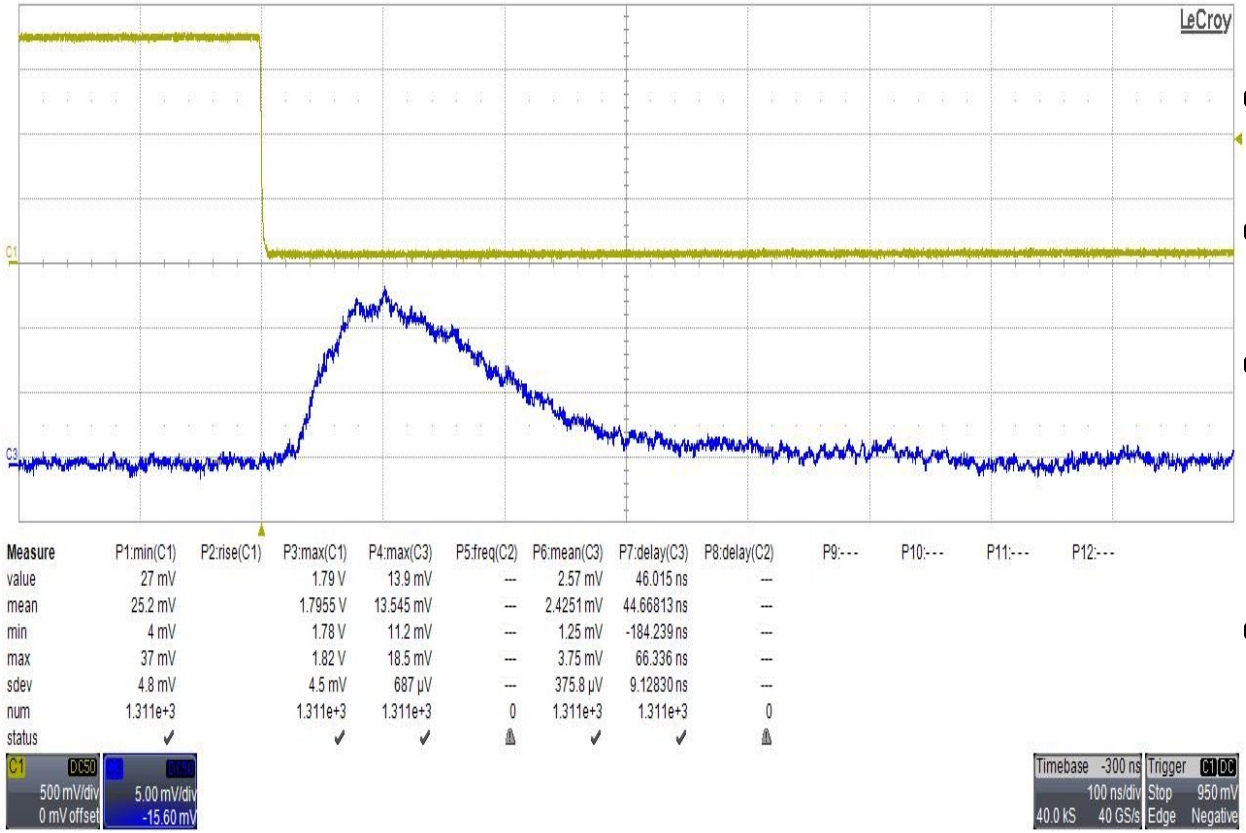
Signal processing chain



- Passive charge integration
- Pedestal stablized with LF feedback
- Active filter adds 2 complex poles
- No undershoot

Noise

Charge injection through 33pF

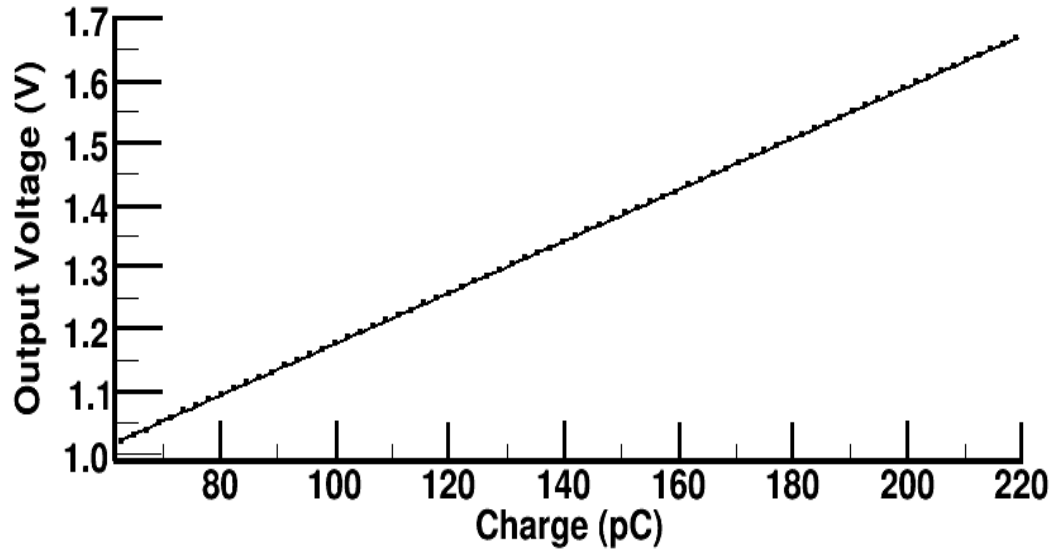


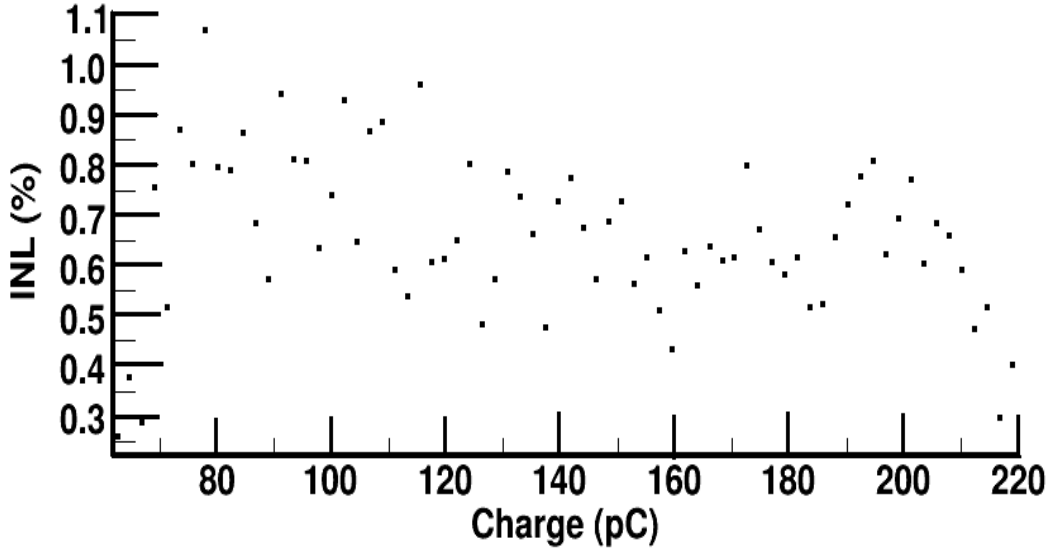
- SNR > 10
- Output V 9mV
- Noise 800uV
- ENC 2.4 $*10^5$ e^-

Dynamic range

- Gain setting

  1, 10 , 40
- INL varies @ different DAC
- INL < ±1.5%

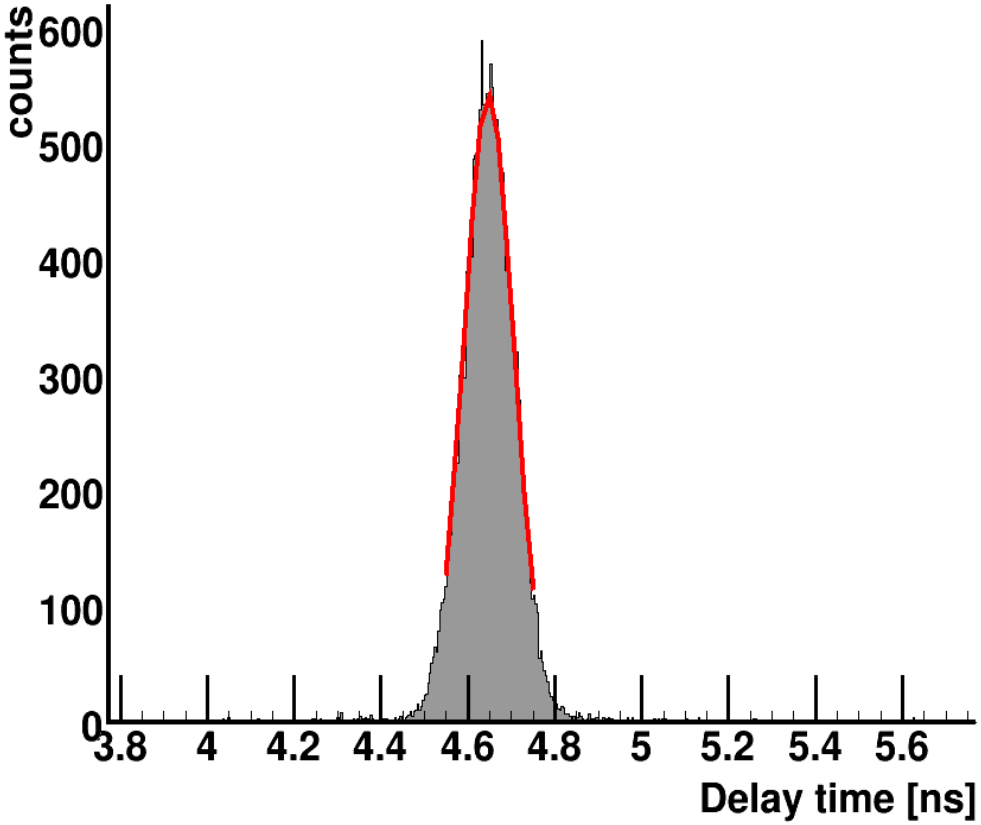




jitter

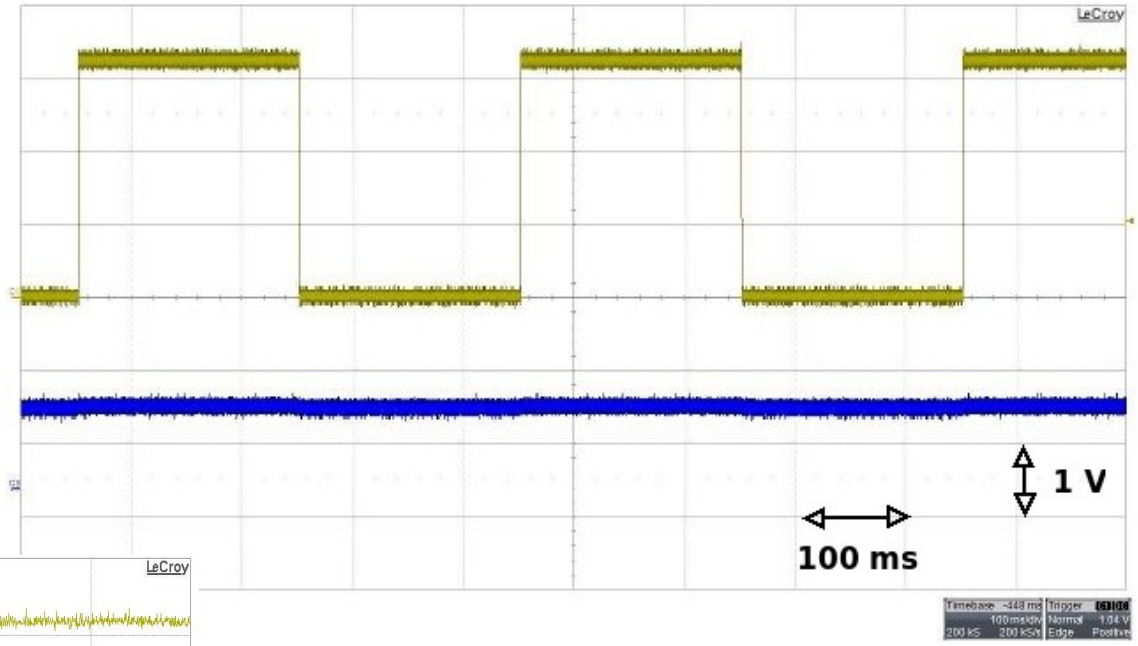
- MIP : 52ps @ 0.5 MIP
- 15 pixel (gain 2.75*105)
- Threshold with off-chip poti
- DACs available

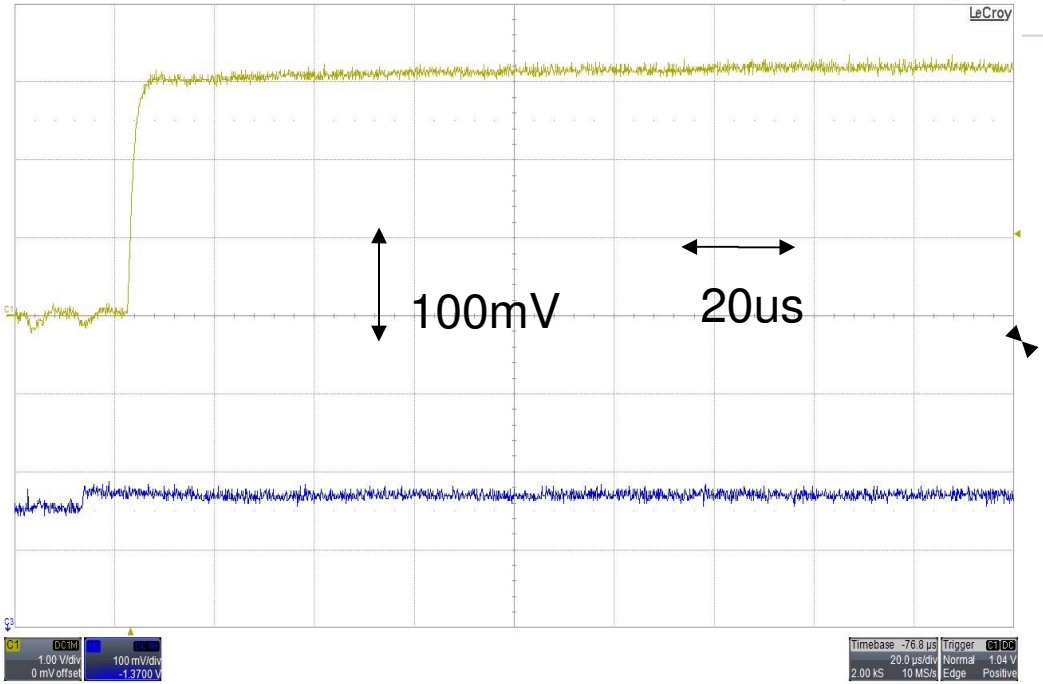
  within NEW ASIC
- Effic. 100%@ 0.5 p.e.
- Walk < 1ns @ 0.5 MIP



Power pulsing

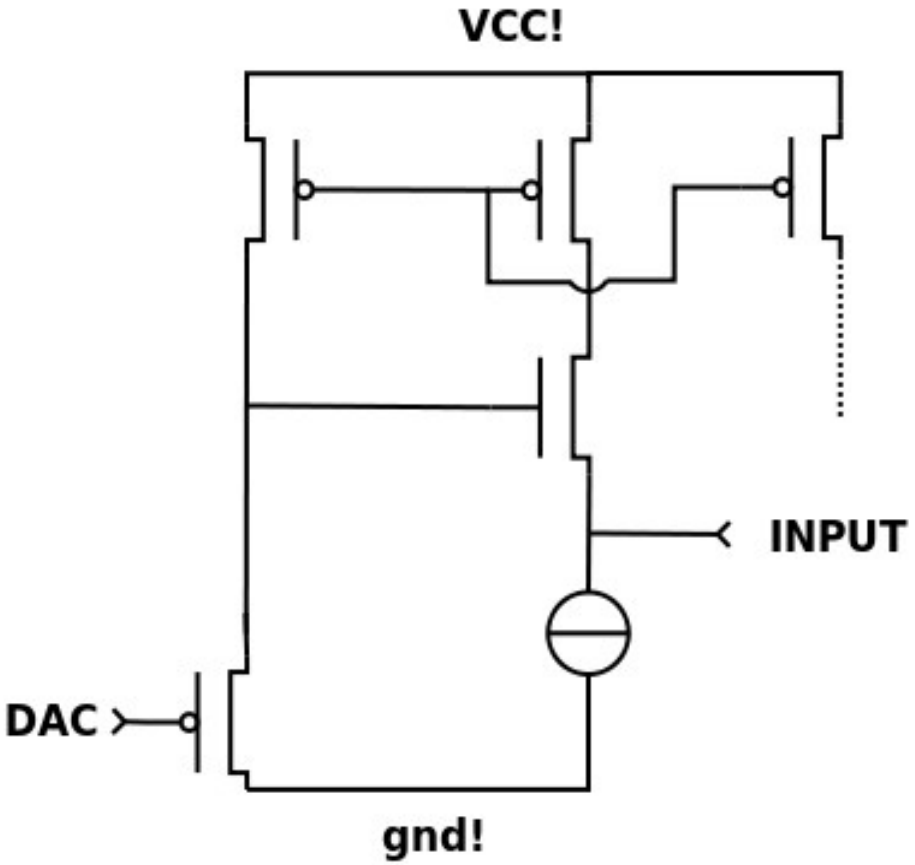
Input voltage
during power pulsing





- ✓Voltage difference < 20mV
- ✓1-2% SiPM overvoltage
- ✓20us recovery time

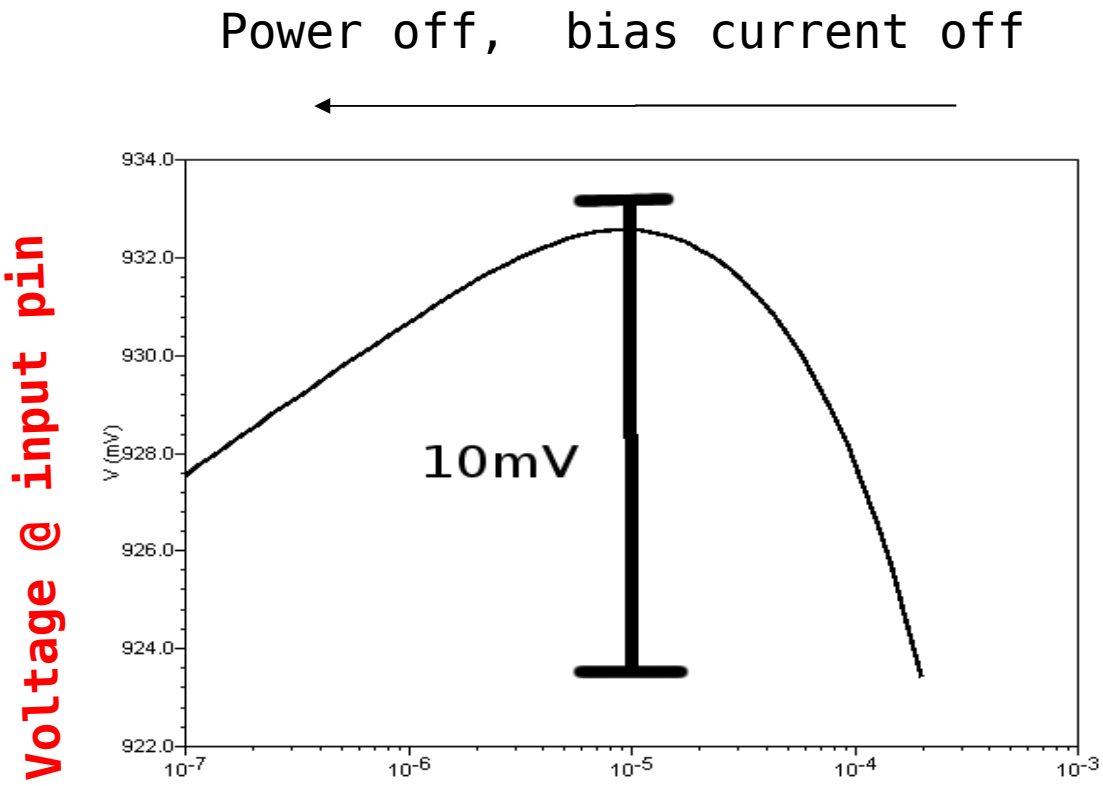
Power pulsing



Input voltage remains fixed at different bias current

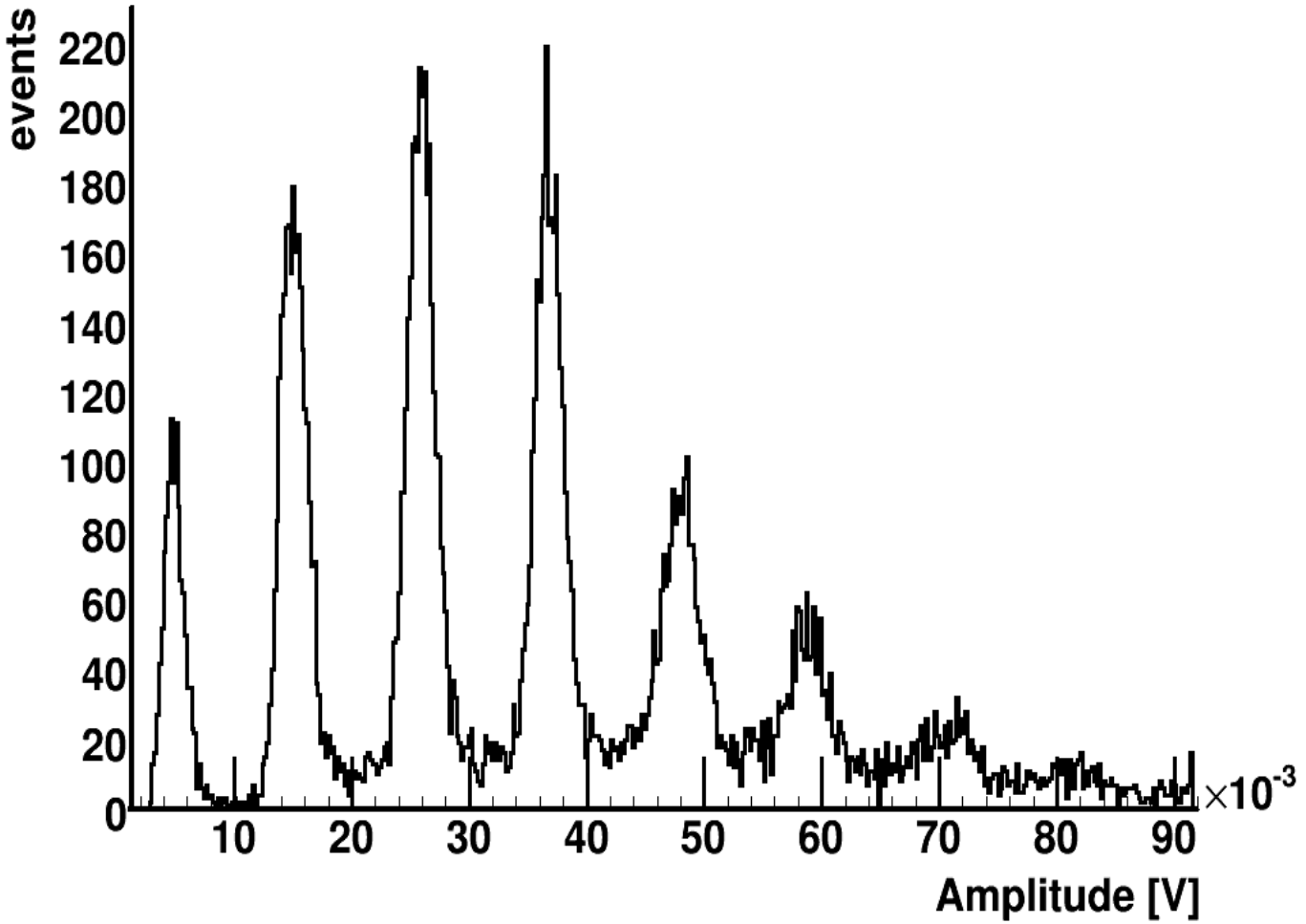
due to input stage feedback

SPICE simulation



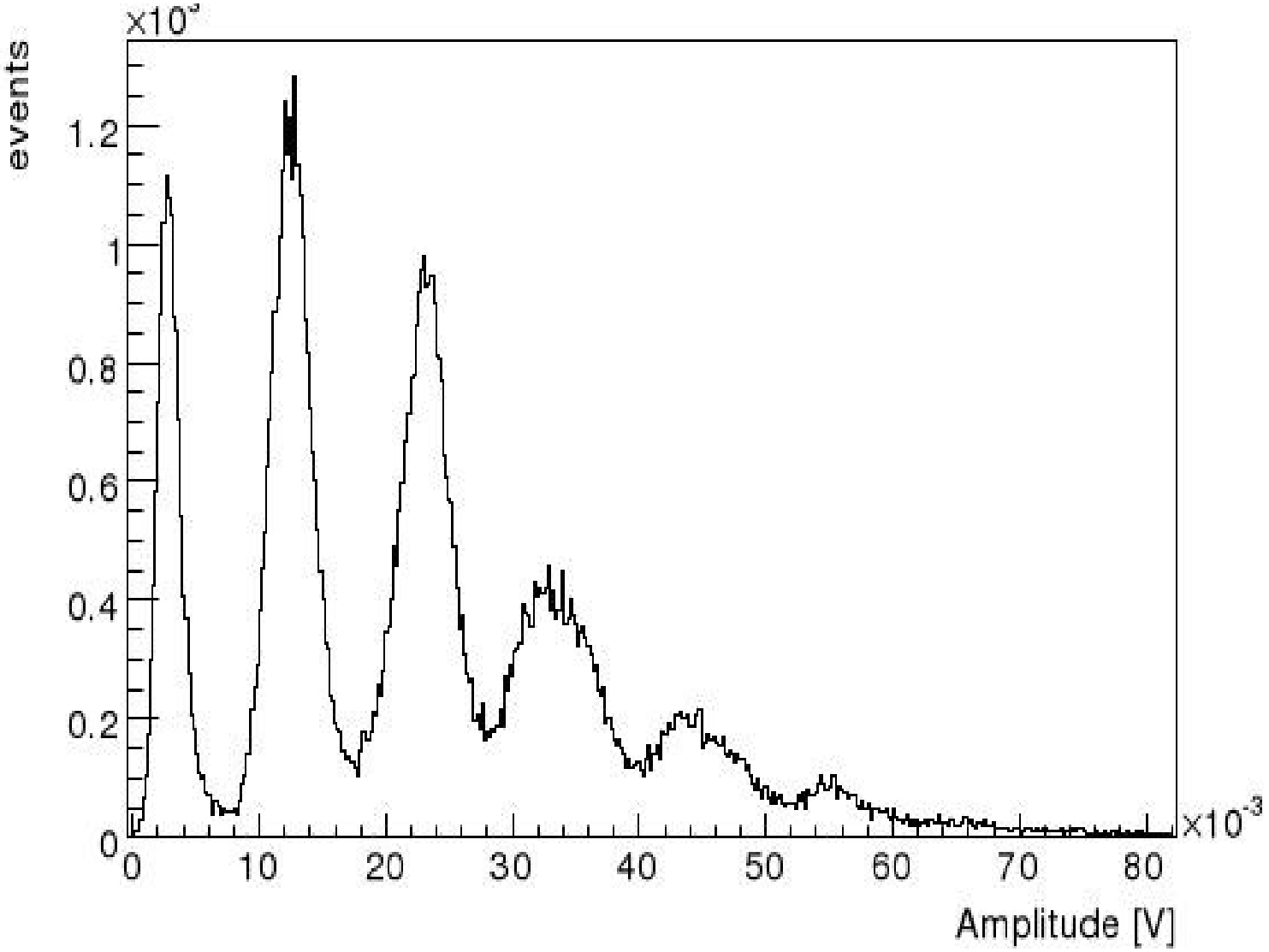
SiPM spectra

MPPC 1600pxl 25um @ nominal voltage



SiPM spectra

CPTA SiPM @ low overvoltage



summary

Summary

- KlauS2v0 is functional, performance similar to simulation results
- functional with different SiPMs
- SNR > 10 for low gain SiPM
- jitter ~ 50ps for MIP signal

Outlook

- more results on uniformity, power pulsing
- possible integration into SPIROC