Update on the BPM study for Run 2c

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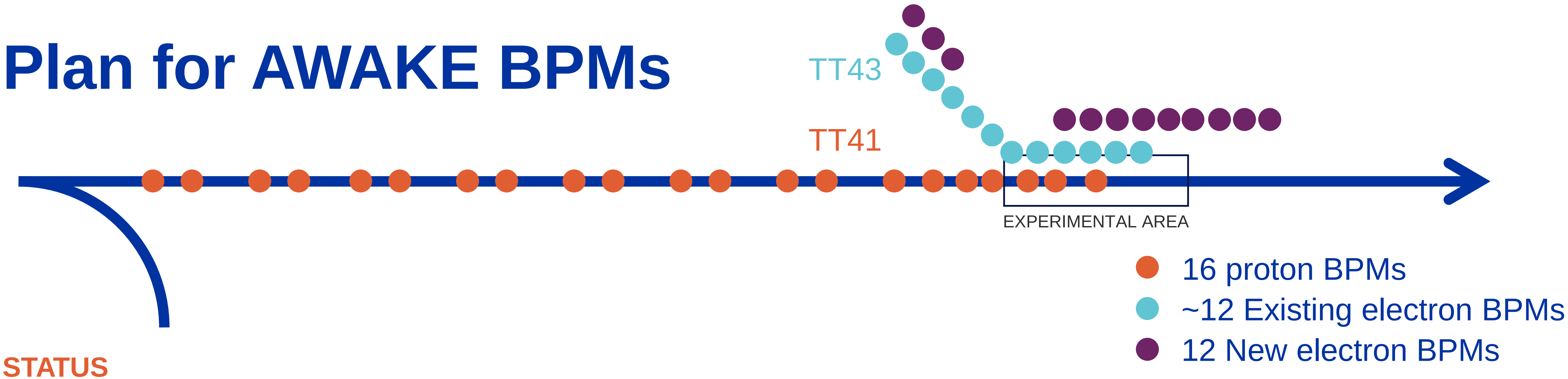
Plan for AWAKE BPMs



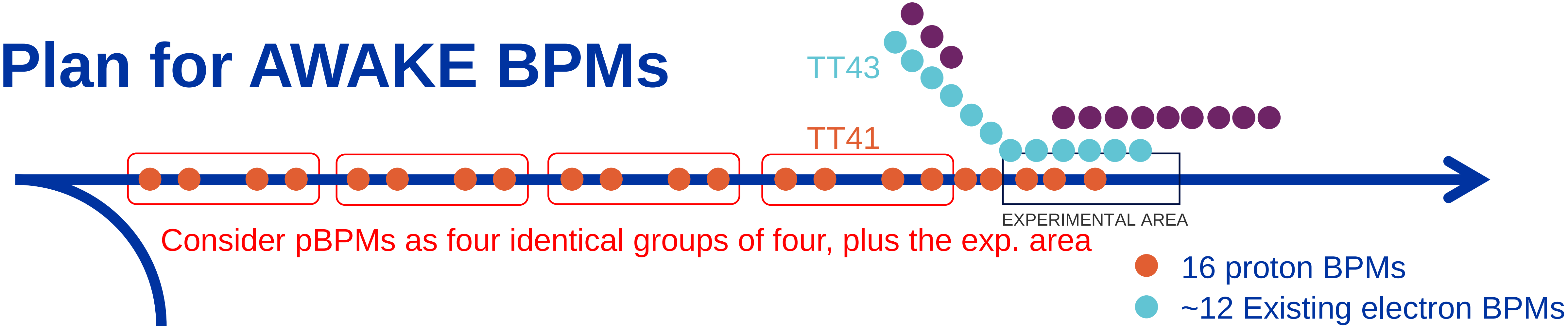
STATUS

- We want to improve the proton BPM resolution from 70 um to around 20 um.
- We need to add 12 electron BPMs plus 3 spares for the Run 2c layout.
- The TRIUMF agreement for producing and maintaining eBPMs has expired and software/firmware support is not available.

PROPOSAL

- Develop a new integrated pBPM frontend/backend based on RF system-on-chip technology being developed for other CERN BI projects (such as HiLumi LHC BPMs).
- Develop new eBPM electronics similar to that for the pBPM and therefore bring in-house to CERN.

Plan for AWAKE BPMs



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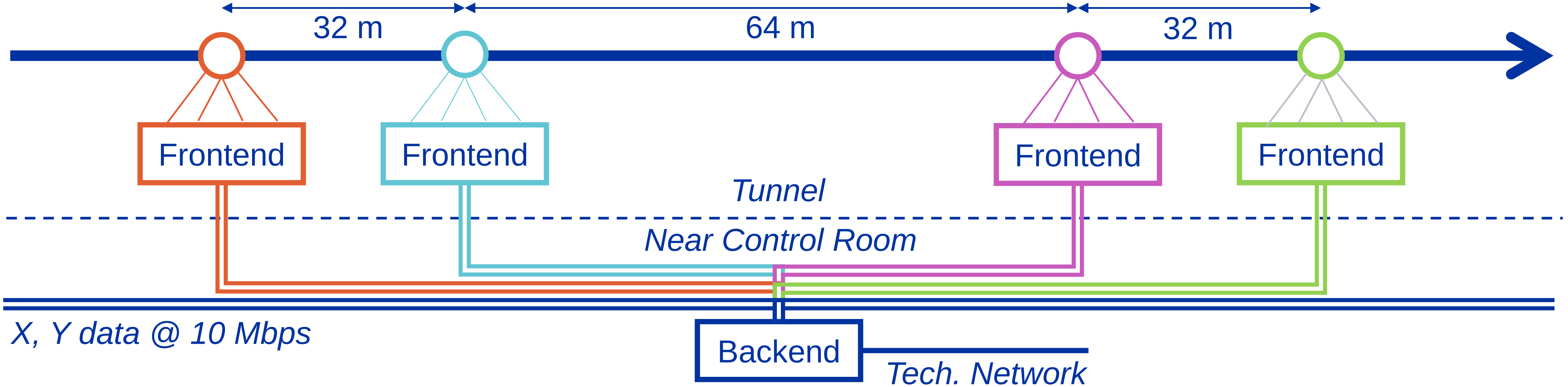
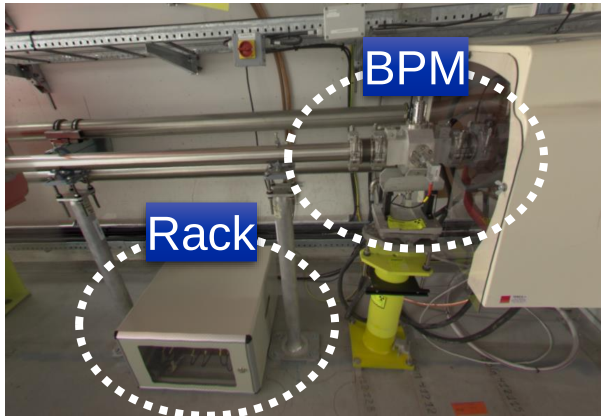
Proton BPM Layout - Existing



- **Each of the 16 transfer line pBPMs uses a local frontend below the beam.**
- **Position information is sent over a coaxial cable to a shared backend located near the AWAKE control room.**



- **The five pBPMs located in the experimental area are connected to frontends grouped in a rack in the adjacent corridor.**

SoC Platform – Fronted *and* Backend

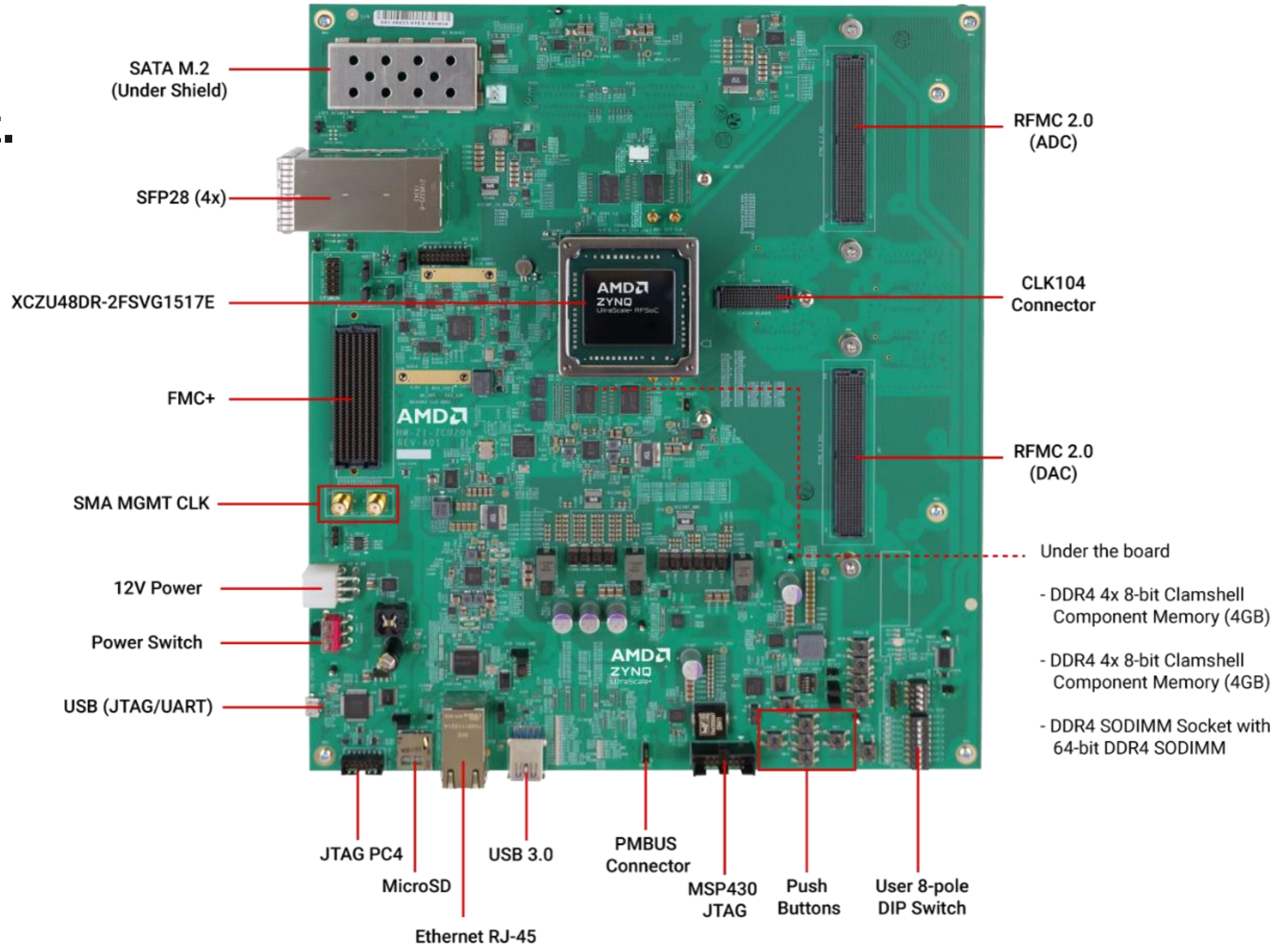
Development shared with LHC HiLumi project.

Xilinx/AMD Zynq RFSoC featuring:

- **Ultrascale+ FPGA fabric**
- **8x 5 GSPS 14-bit ADC channels**
- **8x 10 GSPS 14-bit DAC channels**
- **High performance ARM processing cores**
- **Flexible timing and integration options**

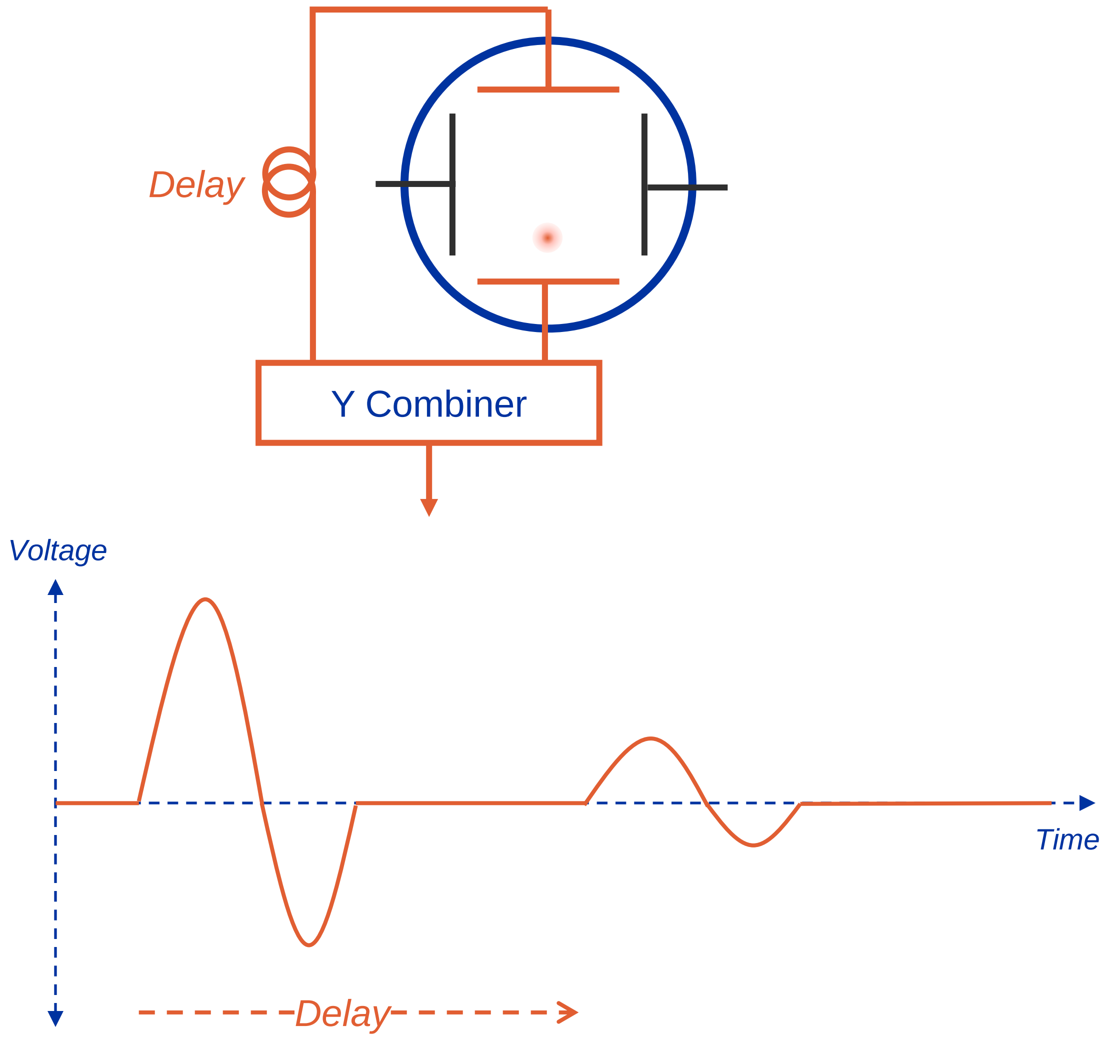
Procurement

- **ZCU208 development board**
- **Researching system-on-module for production, with CERN-built carrier.**

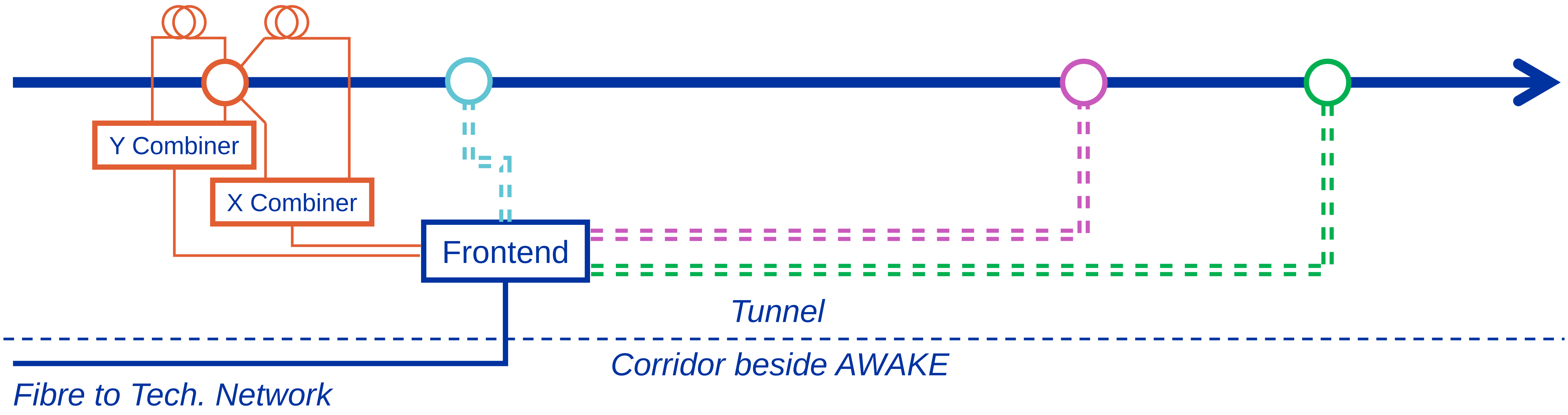


Time Multiplexing

- **Because of the very high sampling rate of the RFSoC, we don't need to time-stretch pulses (via lowpass filtering) to achieve adequate signal to noise ratios.**
- **This means we can time multiplex multiple pickups using cable delays and reduce the required number of ADC channels.**
- **Using this technique, we can also remove systematic errors (position offsets) arising from any difference between channel gains for the same axis:**
  - Cable drift
  - Component response variation
  - ADC drift



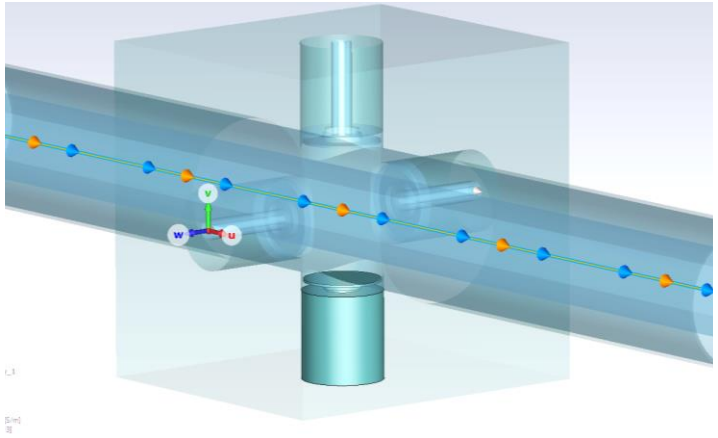
Proton BPM Layout - Proposed

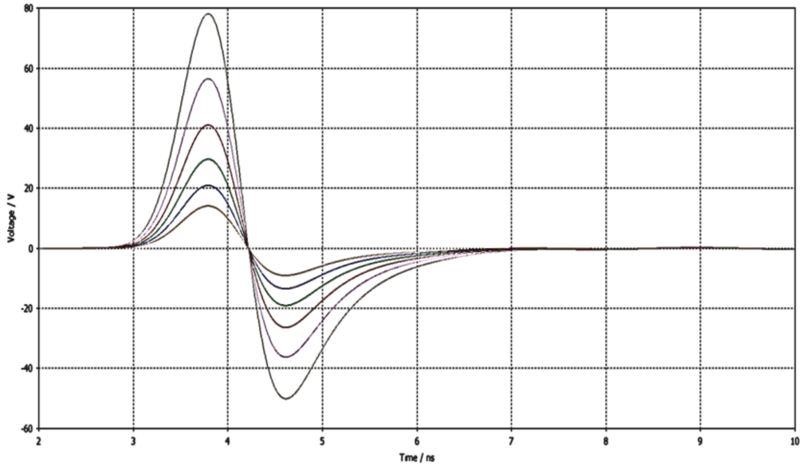


- **New RFSoC frontends cover four pBPMs each.**
- **Position data is calculated onboard as before, but is now available directly to the technical network through FESA (the plan is for one FESA device per BPM).**
- **Ethernet connection runs over fibre to adapters in the eBPM racks which connect to a network switch.**
- **Experimental area frontends located in eBPM racks as space will be made with the new eBPMS.**

Beam Simulation via CST and Python

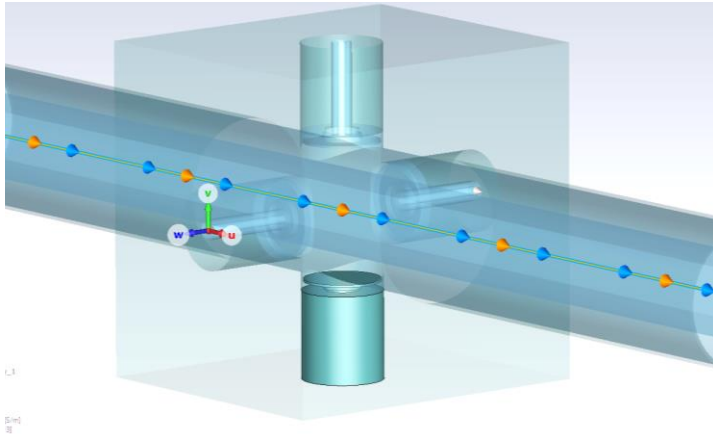
- **Simulate pilot and 3E11 proton beams in CST and create fits for intensity and position from pickups.**
- **Simulate each step of the analogue signal path from pickup to ADC.**

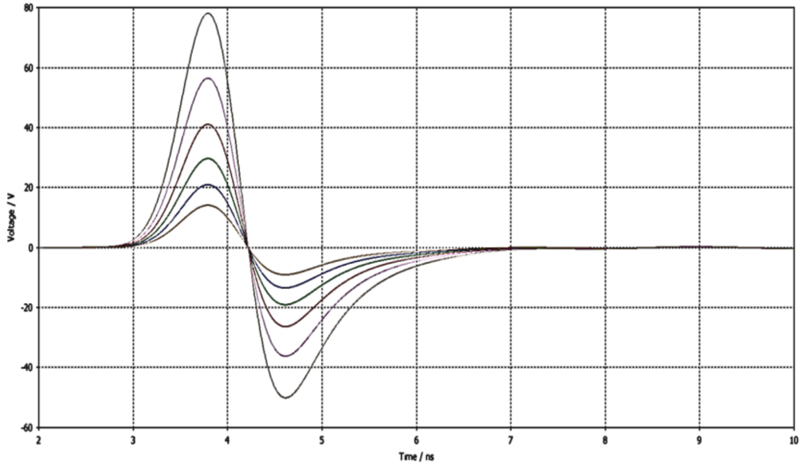


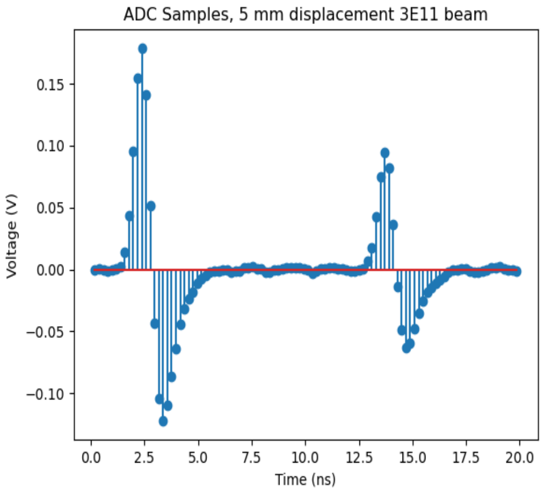


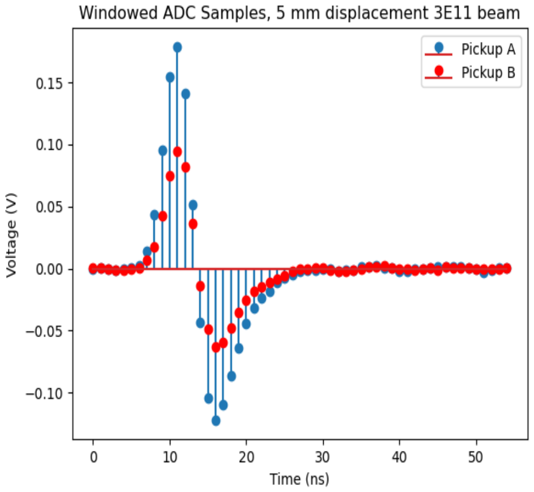
Beam Simulation via CST and Python

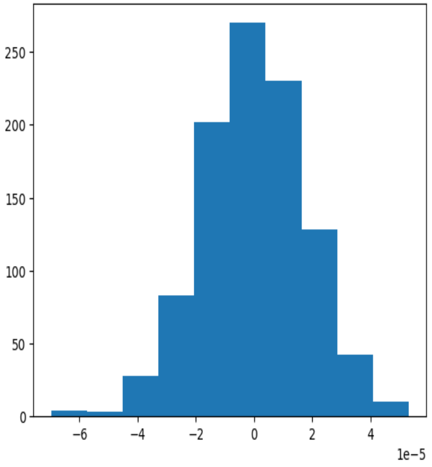
- Simulate pilot and 3E11 proton beams in CST and create fits for intensity and position from pickups.
- Simulate each step of the analogue signal path from pickup to ADC.
- Sample 1000 pulses with random quantisation noise from ADC based on datasheet values and lab measurements of sinusoids (8.5 to 9.5 ENOB).
- Calculate position using Δ/Σ on RMS of samples with high order sensitivity fit and obtain standard deviation as "resolution".











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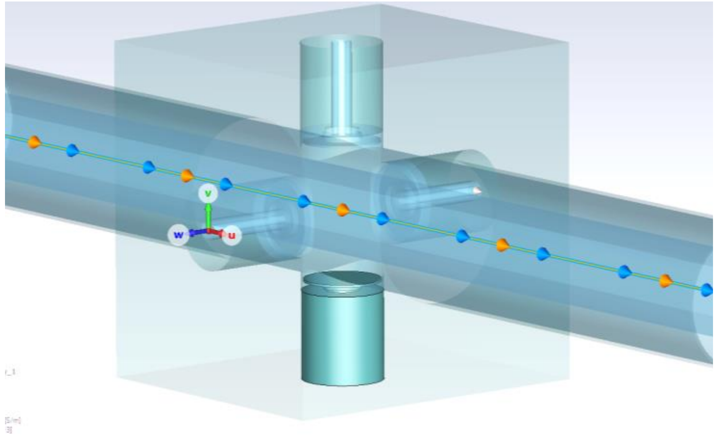
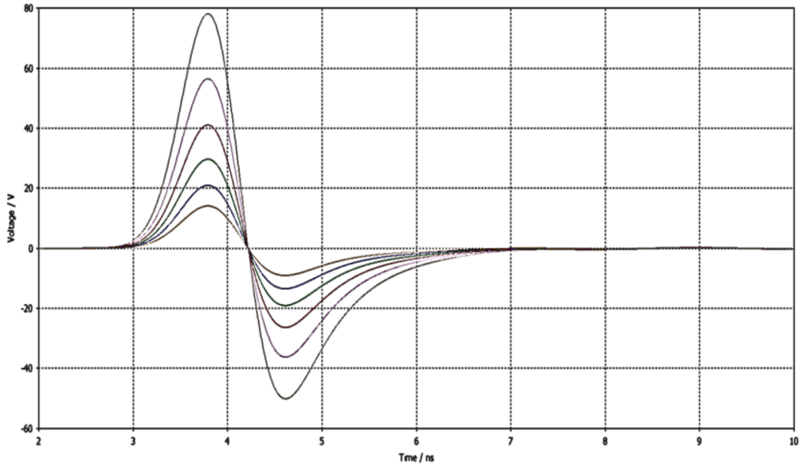
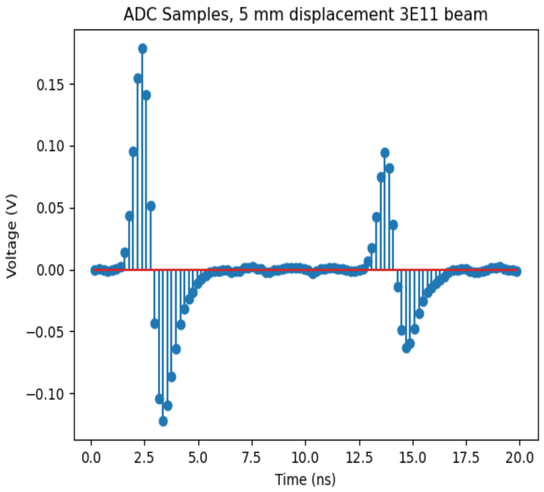
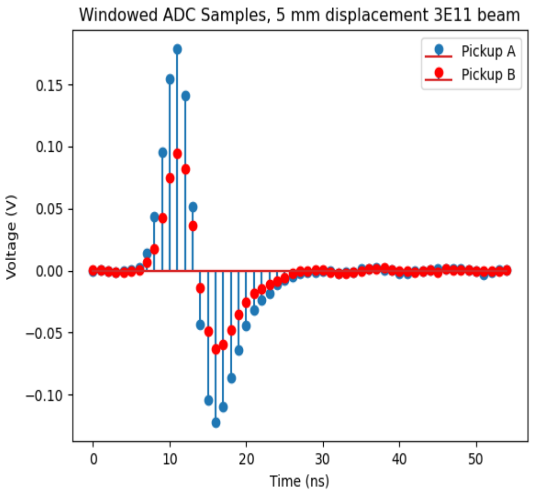
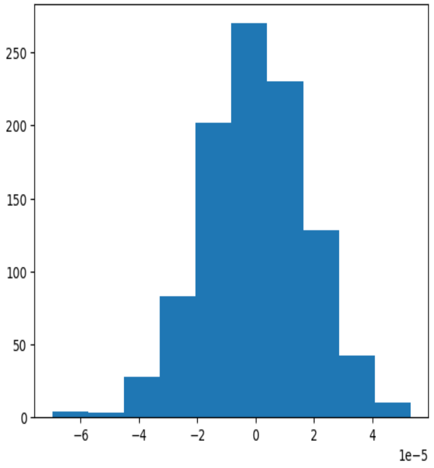
- Sample 1000 pulses with random quantisation noise from ADC based on datasheet values and lab measurements of sinusoids (8.5 to 9.5 ENOB).
- Calculate position using Δ/Σ on RMS of samples with high order sensitivity fit and obtain standard deviation as "resolution".
- Vary bandwidth of frontend from 800 MHz to 100 MHz.
- For all simulations, set input attenuation such that ADC is 70% full scale at ¼ aperture beam offset.



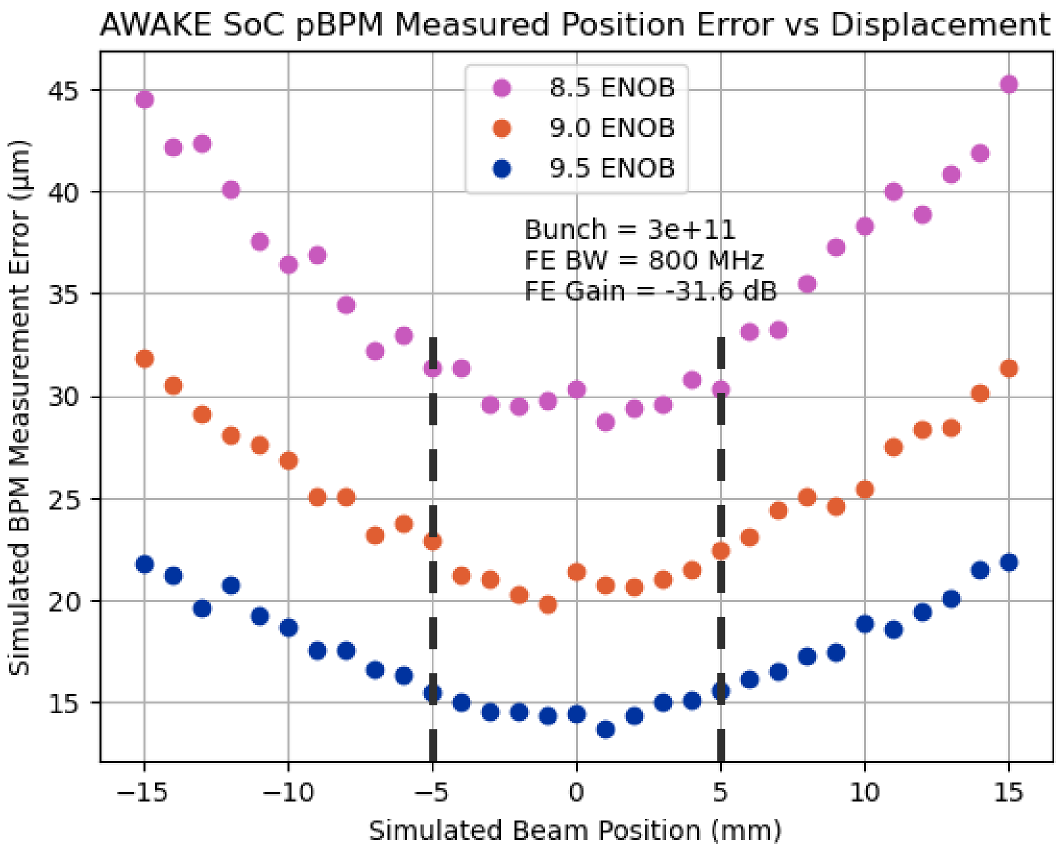


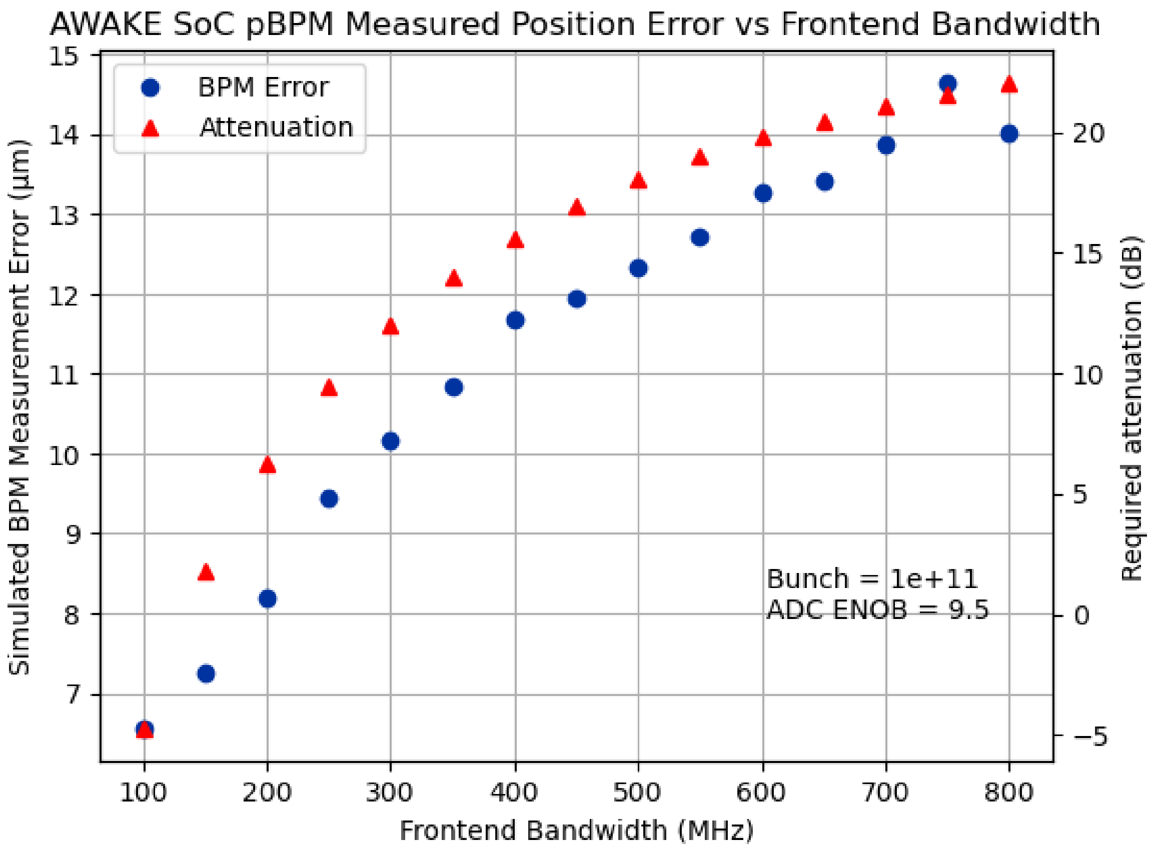






Simulation Results – Science Beam

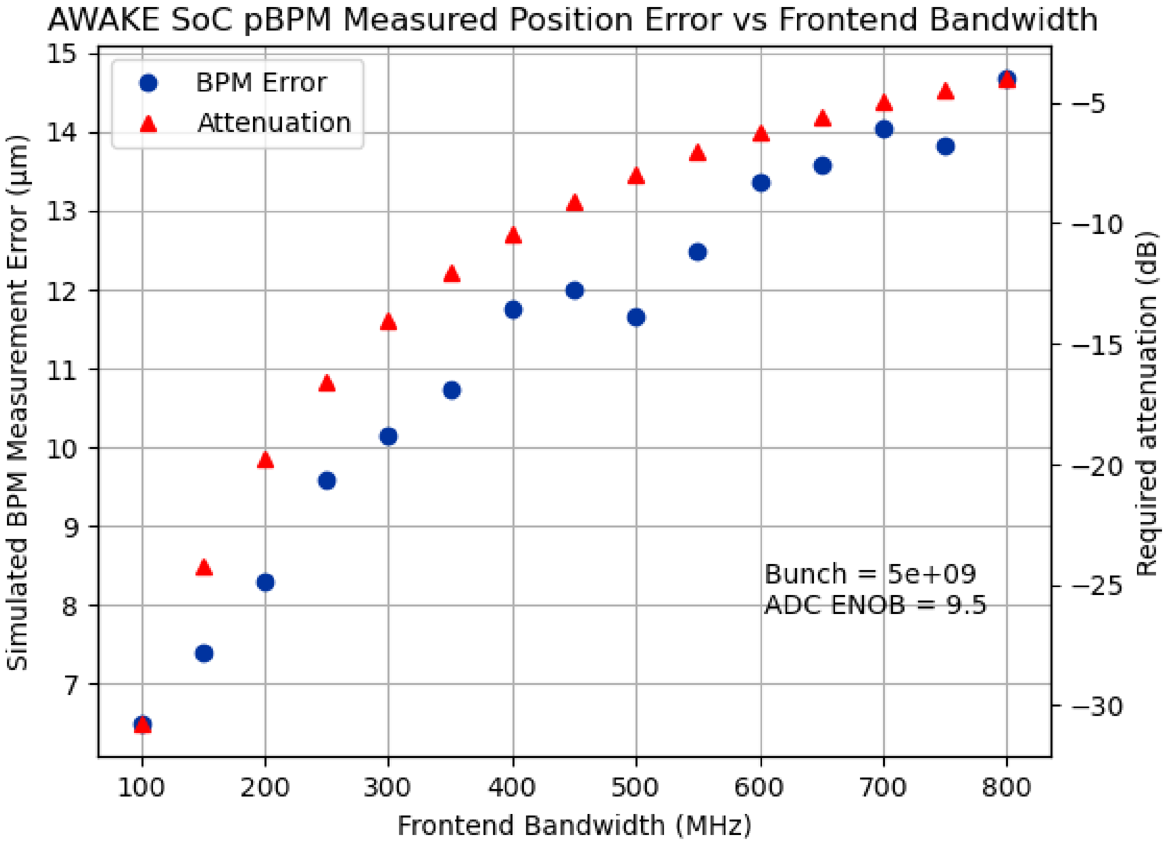


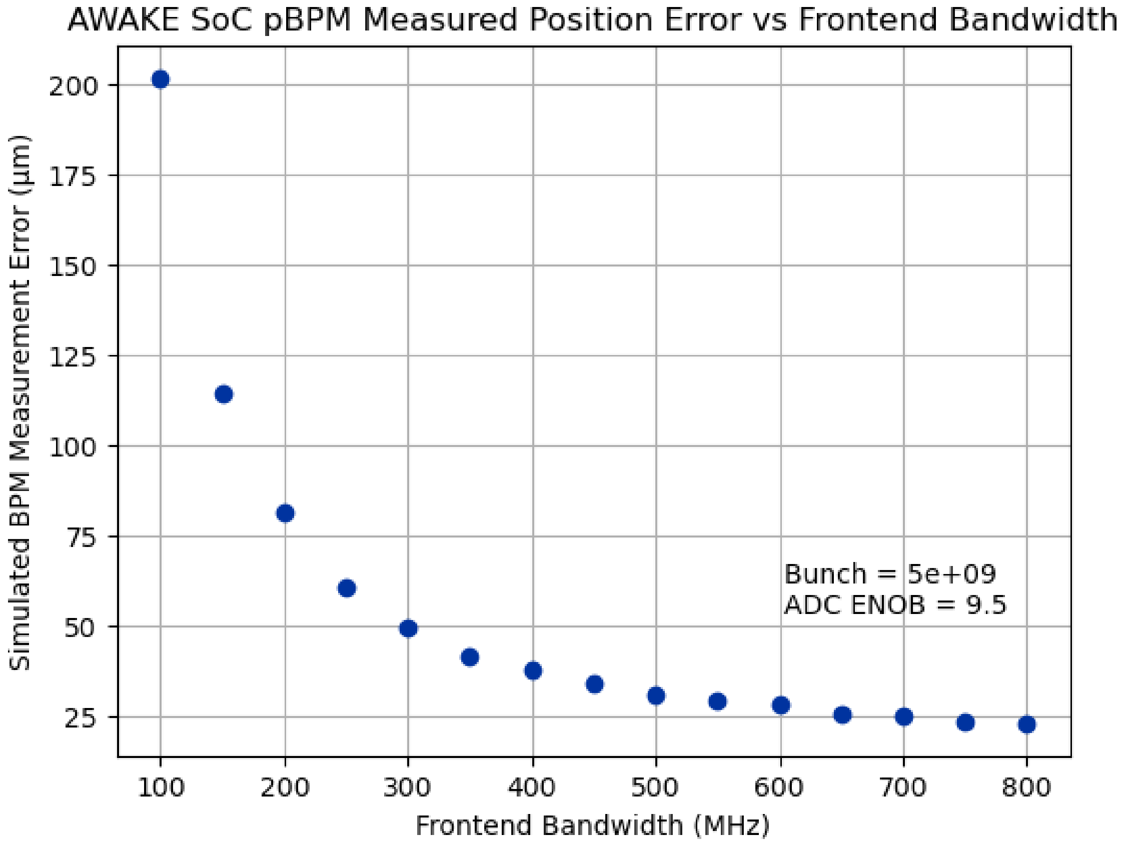


Error increases with beam offset due to increasing pickup sensitivity coefficient. Typical beam offset within 5 mm.

We can improve resolution by reducing bandwidth. This stretches the pulse and gives more samples for the RMS. The stretched pulse is weaker but still no amp needed for 1E11 beam.

Simulation Results – Pilot





For the pilot beam we would require amplification to achieve the same resolution. For low bandwidths this becomes significant.

If no amplification is used the resolution will degrade. We envisage ~200 MHz bandwidth so this would reduce to ~100 µm.

Lab Results from Pulse Generator

- **Simulated waveforms were exported to a pulse generator and measured by the RFSoC, then run through the same processing as before.**
- **Noise/resolution was shown to be limited by pulse generator, but we must be close to the ADC effective resolution so I would not bet on any improvement over these numbers.**
- **Filters *should* improve the resolution as attenuation was removed to match the amplitude with the 800 Mhz signal.**

σ of 1000 acquisitions

Beam Offset	800 MHz	Filter 1 (300 MHz)	Filter 2 (220 MHz)	Filter 3 (180 MHz)
0 mm	15 µm	17 µm	--	18 µm
5 mm	16 µm	--	--	--
10 mm	21 µm	--	--	--
15 mm	26 µm	24 µm	28 µm	28 µm

This agrees well with 9.5 ENOB simulation

Next steps for pBPM

- **Perform more lab testing to check filter behaviour.**
- **Measure delay effect on pulse crosstalk and hence accuracy (beam offset).**
- **Measure some real LEP button signals on SPS with the RFSoC hardware.**
- **Attach a complete combiner setup to an AWAKE pBPM plane and measure during this run. This would be simple on an experimental area pBPM in the grouped rack as network access is adjacent.**

AWAKE Electron BPMs

- About to begin the study into these.
- Planning to share as much of the pBPM design as possible.
- Should achieve similar performance to the pBPM, especially as we would not use combiners and so can match amplitudes of each channel to better utilise the ADCs.
- Reuse of TRIUMF frontends is possible, but this would require updating the design against components obsoleted especially after the global chip shortage.
- We would then need to onboard production, test and maintenance for a board which we will not use anywhere else!

Conclusion

- **Promising results from initial pBPM studies with RFSoC frontend.**
- **We should achieve around 15 μm resolution on the pBPM with this setup.**
- **New eBPM configuration will now be studied, with the objective of a shared design and resolution matching the existing system.**

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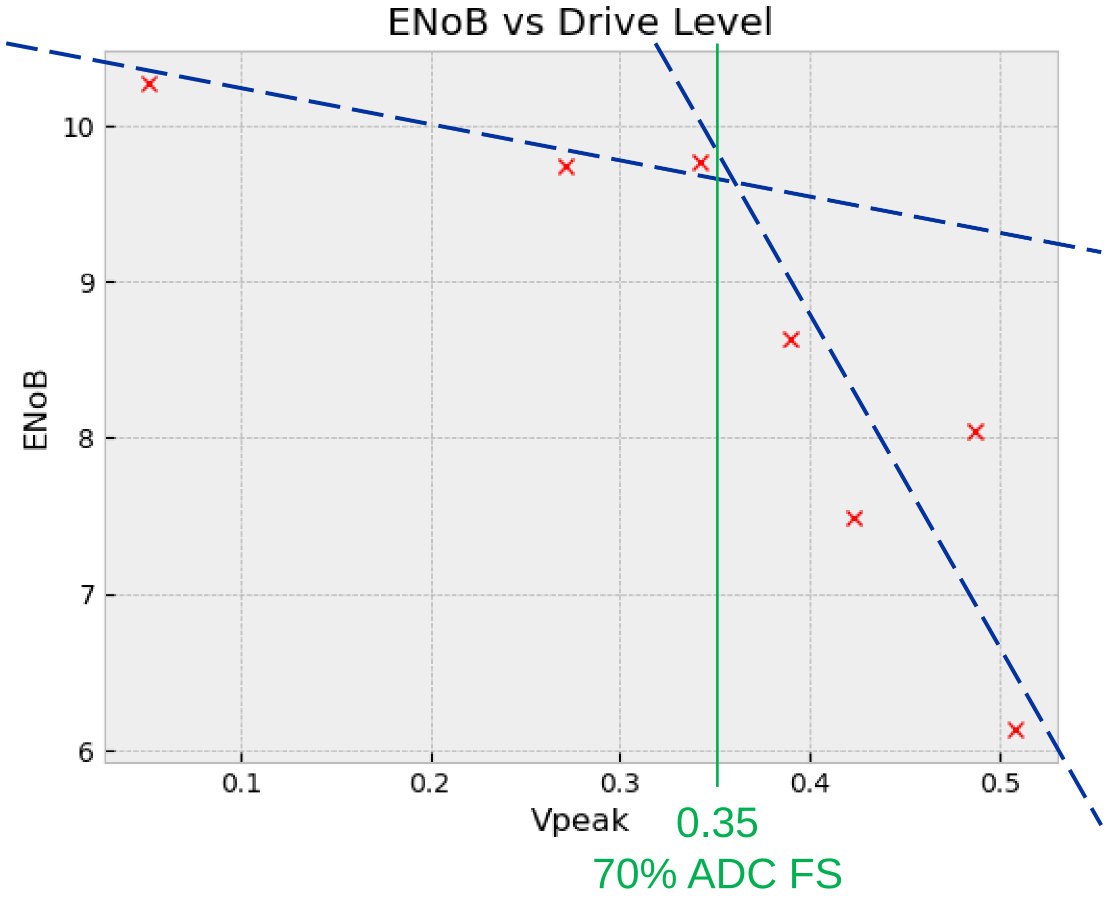
ADC ENOBs

- **Lab measurements of ENOB with sinusoids show there is a knee just above 70% ADC full-scale, after which the signal is distorted.**
- **However for our RMS detector we are not sensitive to this distortion.**
- **So, we should expect an ENOB between 9 and 10.**
- **This value is used when simulating the quantisation noise in the virtual ADC.**



Rack space

- New BPMs should be 2U plus 1U gap.
- Four pBPMs per 3U.
- For exp. area (5 pBPMs) this means 6U.

- Retain 14 eBPMs, add 12.
- Two eBPMs per 3U.
- So this is 39U.
- Should not require RF distribution kit.

- So total for both racks = 39U + 6U = 45U.
- Racks are 35U. Space in right for rest.