Development of Silicon-On-Insulator PHoton Imaging Array Sensor (SOPHIAS) for X-ray Free-Electron Laser

PIXEL2012 Inawashiro, Japan

Motohiko Omodani[A], Togo Kudo[B], Kazuo Kobayashi[A, B], Toshifumi Imamura[C], Takafumi Ohmoto[C], Atsushi Iwata[C], Shun Ono[B], Yoichi Kirihara[B], Masao Okihara[D], Motoyuki Nagasaki[E], Kazuharu Morita[F], Yosuke Nagai[F], Takaki Hatsui[A, B]

Japan Synchrotron Radiation Research Institute[A], RIKEN[B],A-R-Tec Corp.[C], LAPIS Semiconductor Co., Ltd.[D], ARKUS Inc.[E], TOKYO ELECTRON DEVICE LIMITED[F]

Introduction

SPring-8 Angstrom Compact free-electron LAser (SACLA), which is the second X-ray free-electron laser (XFEL) facility after LCLS at SLAC National Accelerator Laboratory achieved laser amplification on June 7th, 2011. In the first user run of SACLA starting in March 2012, 25 proposals from domestic / international institutions will be conducted, where more than half of the proposals will use the currently deployed Multiport CCD (MPCCD) detectors.

We are developing another novel X-ray 2D detector, Silicon-On-Insulator PHoton Imaging Array Sensor (SOPHIAS), for SACLA to cover the scientific cases, where the currently deployed MPCCD detector does not able to reach. The pixel structure of SOPHIAS is based on multi-via concept; the closely spaced implant regions within a single pixel is used for signal charge division. This structure provides a wide dynamic range.

Last year, we have introduced stitching and backside processing onto KEK multi-project wafer run process. We have succeeded in manufacturing with an area of 66 mm x 30 mm by stitching 5 shots of reticule size. The production is carried out by 0.2 um FD-SOI CMOS technology. Handle wafer, which is the photodiode for x-ray detection, has backside implanted, laser-annealed, and aluminum coated surface so to shield the optical light without sacrificing the quantum efficiency. The handle wafer is made of floating zone silicon which enables us to fully deplete 500 um thick handle wafer. The characterization as well as the development of readout system of the sensor is now under progress.

SOI Pixel Detector *Monolithic* Si *Pixel Sensor with VLSI*

Collaboration of KEK, Lapis Semiconductor, A-R-Tec and RIKEN

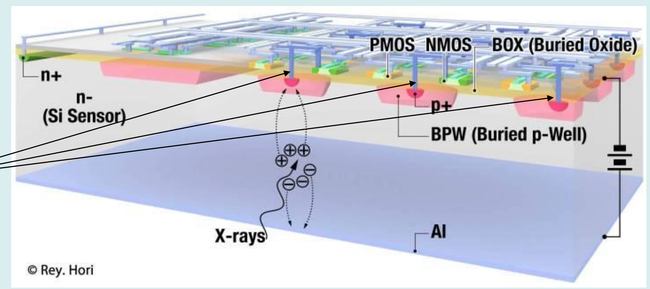
Advantages Summarized by KEK

- Bonded wafer → Thick High Resistivity Sensor + CMOS
- Monolithic Detector → High Density, Low material
- Standard CMOS → Complex functions in a pixel
- No mechanical bump bonding
  → High yield, Low cost
- Small input capacitance
  → ~10fF, High conversion gain, Low noise
- Based on Industrial standard technology
  → Cost benefit and Scalability
- No Latch Up, Low SEE
- Low Power
- Operate in wide temperature (4-570K) range.

RIKEN joined SOIPIX collaboration from the end of 2007

Control of charge collection *SOPHIAS*

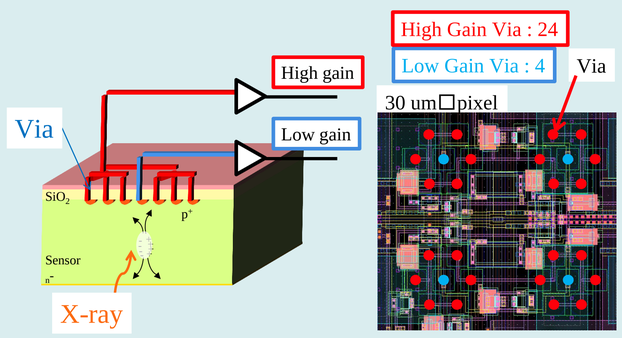
Sample Hold Electronics With 20 ENC at close to GHz rate



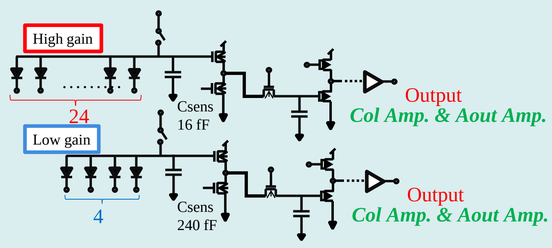
CMOS layer is fabricated by standard process flow onto SOI wafer. The handle wafer, normally used as mechanical support, is used as photodiode. Between the pn photodiode and the CMOS layer, we introduced "via" through BOX layer to transport the charge from the photodiode to CMOS layer. Since the through via are made by CMOS technology, the charge collection step can be easily controlled. Another point that we would like to address is the small input capacitance. Simple sample and hold electronics have already gave 20 ENC performance with sampling rate of ~GHz.

Y. Arai, et al., Nuclear InstrumentsandMethodsinPhysicsResearchA636(2011)S31–S36

SOPHIAS Pixel Layout by Multi-Via Concept



SOPHIAS In-pixel Schematics



Gain	Csens [fF]	Via #	Gain [uV/e]
High	16	24	7.2
Low	240	4	0.15

Left figures show Multi-Via Concept. Each implant region is connected to the readout circuitry by metal via. By connecting non-equal number of via metal, unproportional charge collection is possible. Large portion of the signal is transferred to high gain amplifier sensitive to small signal regime, whereas small portion of the charge is transferred to low gain amplifier. This pixel with size of 30 um square is realized by using silicon-on-insulator (SOI) sensor technology.

Right figure shows In-pixel Schematics. Signal from the photodiode inputs the source follower, and the charge is stored in a capacitor. The signals are transmitted to Col. Amp. and A out Amp.

SOI Pixel Technology Process/Device/Simulation

2007 when RIKEN joined SOIPIX collaboration

Back-gate effect

Handle wafer resistivity was low after CMOS process.
- **~400 ohm/cm**

Small sensor chip size compared to other technology
- **20 mm x 20 mm**

Devices were for digital, not for analog circuitry.

X-ray Radiation hardness was not evaluated.

Current Status

- Buried P-well proposed by KEK, and now extensively used.
- New Developments
  - Nested well proposed by Fermilab
  - Double SOI proposed by KEK
- FZ with > 3 kohm/cm
- Stitching
  - 66 mm x 30 mm achieved
  - 130 mm x 130 mm is possible
- 4M to 5M, MIM Cap onto 3M
- 1/f noise suppression by Source-tie and body-tie Tr.
- Simulation environment improvement.
- Currently upto 150 krad for Tr.
  → SOPHIAS is for < 7 keV with back-illumination
- Systematic study of the radiation damage has been started
  - new process,
  - prediction by radiation damaged device models

SOPHIAS

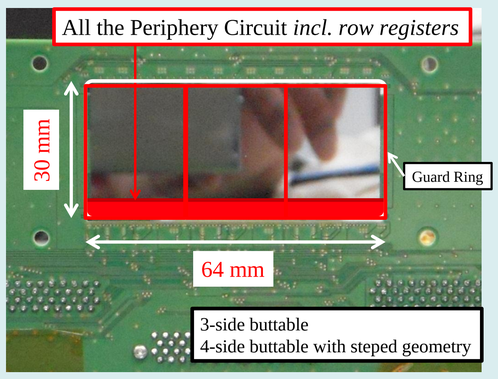
A SOPHIAS mounted on a PCB package for evaluations.

The optical image is taken by high gain video chain, and He-Ne laser spot. In between the lithography shots, we have a spacing without pixels, of which the width is equivalent to one column. The spacing will be filled by interpolation in the down stream. In the optical image for shown above left, any apparent dead pixel are not recognized. It is one of the advantages of SOI sensor technology as it uses only the processes at commercial production level.

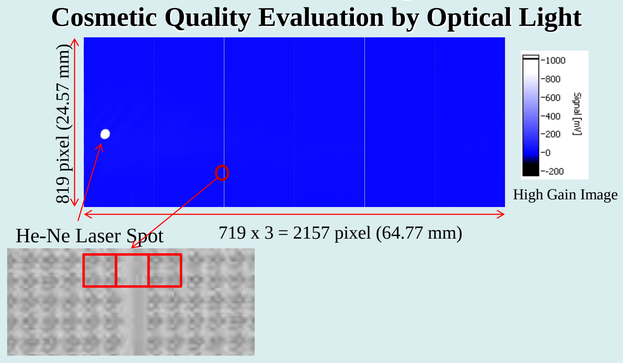
The optical image was statistically analyzed to evaluate the distribution of the dead pixels. There were no dead pixel in the large area of the SOPHIAS! We are now investigating pixel yield as well as chip yield.

By long time exposure to He-Ne laser spot, we confirmed that multiple gains are realized in one pixel of the SOPHIAS.

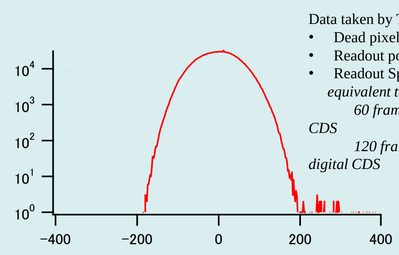
SOPHIAS mounted on a PCB evaluation package



Full Sensor Chip Cosmetic Quality Evaluation by Optical Light



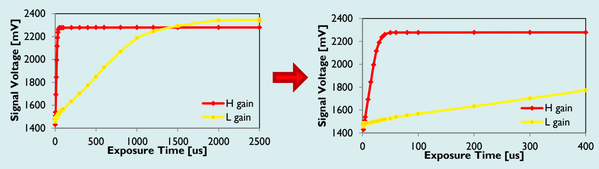
Full Sensor Chip Offset Variation



Dead Pixel: None
Defect Pixel defined as offset > 200 meV
ratio 2.7 x 10^-5
53 pixels /1.9 Mpixel

Full Sensor Chip Gain Responsively

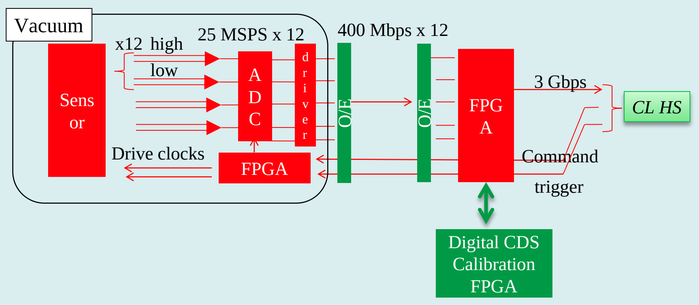
- Design guideline of SOPHIAS pixel
  - Calibration easy pixel
    - Identical behavior against pulse and cont. X-ray sources
  - linearity of raw signal is not mandatory



Qualitatively consistent with physical model
Calibration algorithm is now under progress

Data Processing and Detector Deployment

The recording speed was 25 MHz per pixel, which is equivalent to the 60 frame/sec with off-chip digital CDS. To attain this performance, the chip itself is read at 120 frame/sec.

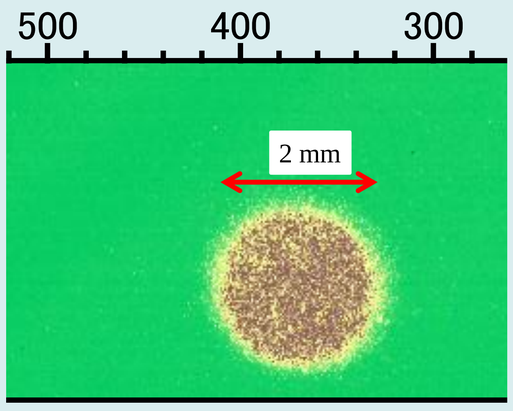


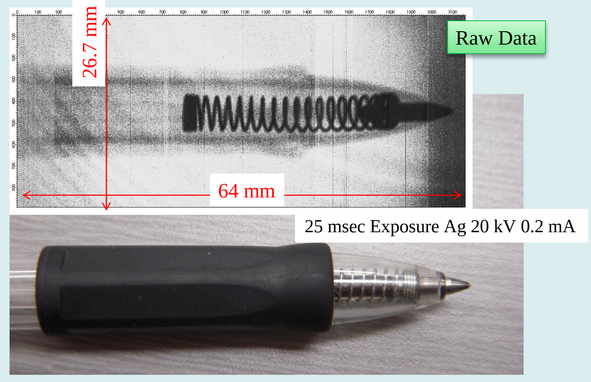
Dual-Sensor Detector
- Deployed to user operation in 2014
- 30 frame/sec
- 4 Mpixel

Multi-Sensor Detector
- Deployment target TBD
- 60 frame/sec
- max 80 Mpixel
- with E/O, calibration FPGA, and CLHS

X-ray Image

X-ray images have been taken using an evaluation data acquisition system controlled by NI-Labview.





Summary

SOI Pixel Technology
- **Ramping up to real scientific applications.**

SOPHIAS
- **Peak Signal 7 Me-, Noise 100 e-, Dual gain pixel, 30 um□ pixel, 1.9 M pixel/chip**

SOPHIAS status
- **Just after 1st run, Testing is underway**
- **Major tasks**
  - **Pixel-by-pixel Calibration**

Deployment to user experiment
- **2014 for Dual-Sensor Detector**
- **Multi-Sensor Detector is envisaged. Deployment date is under discussion.**

After SOPHIAS
- **Low input capacitance**
  - **Fast shutter in the nanosecond regime**