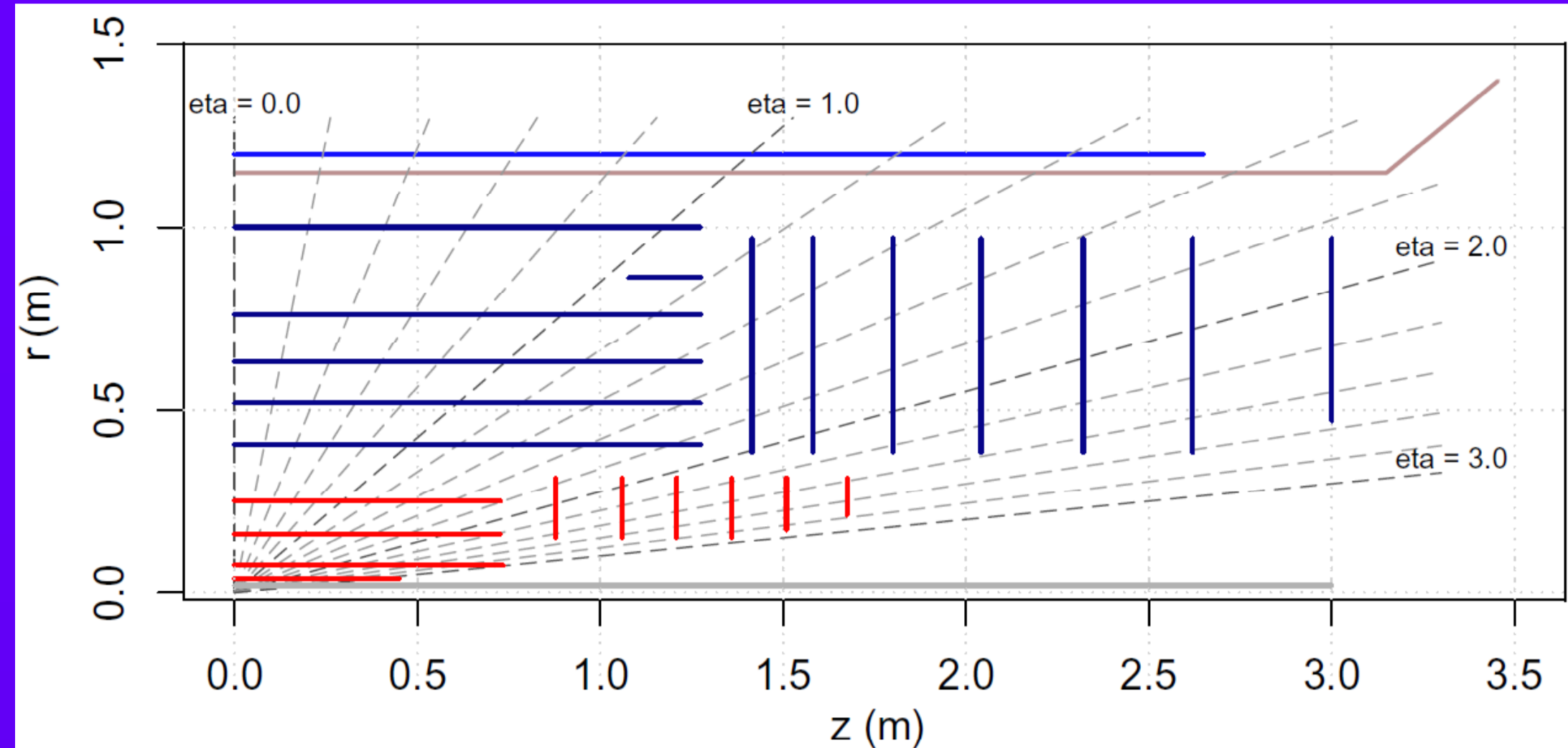


Silicon Strip Detectors for ATLAS at the HL-LHC Upgrade

K. Hara (U. of Tsukuba) and Y. Ikegami (KEK), for the ATLAS Upgrade Silicon Strip Community

The present ATLAS silicon strip (SCT) and transition radiation (TRT) trackers will be replaced with new silicon strip detectors, as part of the Inner Tracker System (ITK), for the Phase-II upgrade of the Large Hadron Collider, HL-LHC. We have carried out intensive R&D programs based on n⁺-on-p microstrip detectors to establish more radiation hard strip detectors that can survive the radiation levels corresponding to up to 3000 fb⁻¹ of integrated luminosity. We describe the main specifications for this year's sensor fabrication, followed by a description of possible module integration schema.



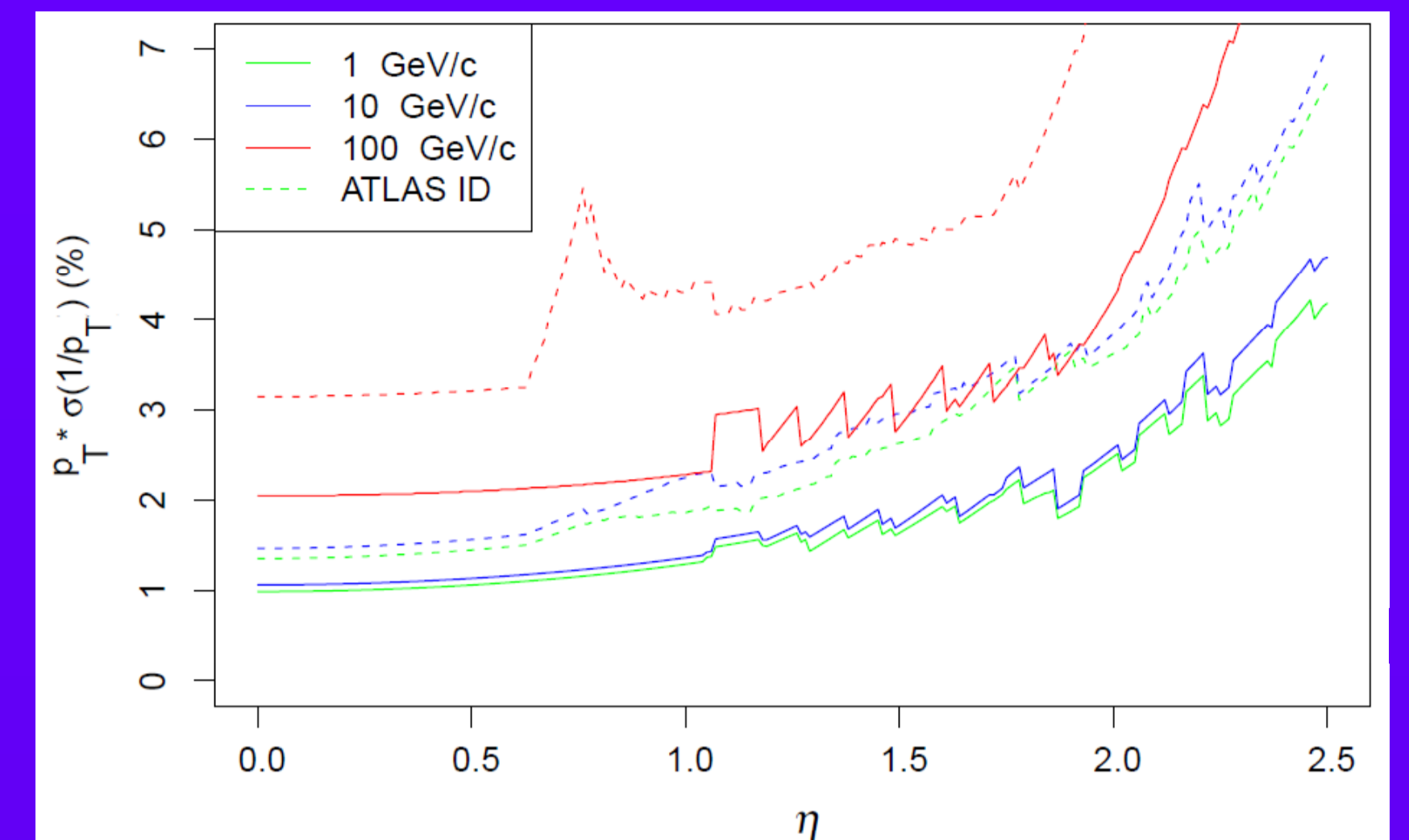
Baseline layout of the new ATLAS inner tracker for HL-LHC (pixels in red, strips in navy blue). The layout aims to have at least 14 silicon hits everywhere to perform robust tracking (Lol layout).

To cope with an increase of five times in luminosity to $5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, the barrel strips at three radii close to the interaction region are 2.4 cm long while the other layers are 4.8 cm (current SCT strips are 12 cm long), both at 74.5 μm pitch (ditto 80 μm). The expected fluence during their lifetime is

Short Strips: up to $1.2 \times 10^{15} \text{ 1-MeV } n_{\text{eq}}/\text{cm}^2$
 Long Strips: up to $0.56 \times 10^{15} \text{ 1-MeV } n_{\text{eq}}/\text{cm}^2$
 Ionizing dose: up to 35kGy

With the baseline layout, the barrel and end-cap strip detectors have respectively 122 and 70 m² area, and 47M and 27M readout channels.

By placing outer radii strips at large radius, the resolution is expected to improve over the current Inner Detector.

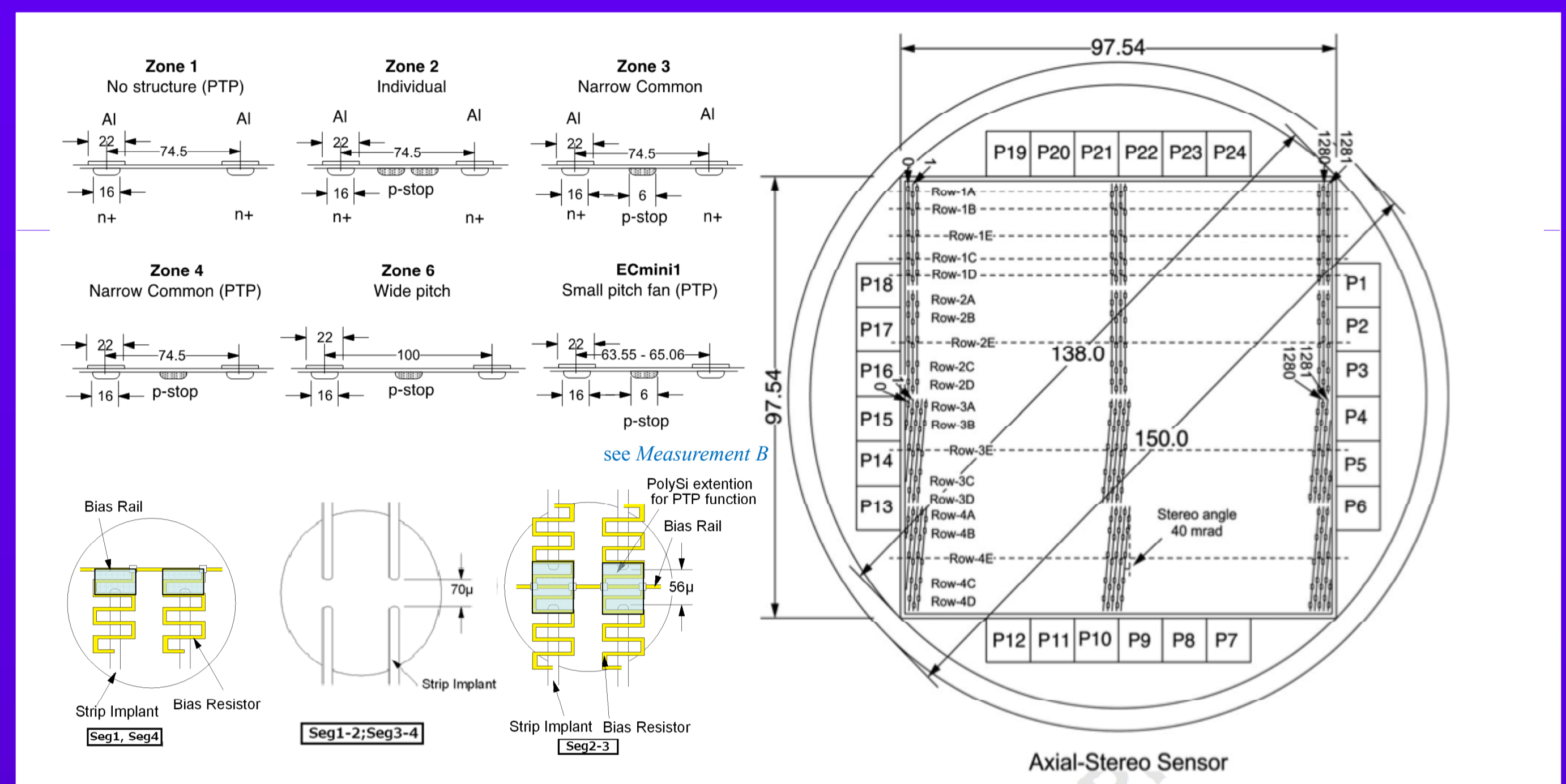


Estimated p_T resolution for different momenta. Dashed curves are for the present ATLAS. This is an analytical calculation.

The main specifications for this year's R&D sensor (ATLAS12) are summarized below:

- The baseline is p-type FZ wafers of >4k Ωcm resistivity to realize initial full depletion of <300V for 320 μm thickness.
- The strip isolation is achieved by common p-stop structure with doping concentration of approximately $4 \times 10^{12} \text{ ions/cm}^2$
- The maximum operation voltage is set at 600 V, suitable for 500V rating of the existing ATLAS cables. No micro-discharge should occur below 600V. However the sensors will be tested up to 1kV to investigate stable operation at higher biases.
- The interstrip capacitance to the nearest neighbor on both sides should be 0.8pF/cm at 300V bias and $f_{\text{TEST}}=100\text{kHz}$.
- >98% of good strips are required.

	ATLAS12
Wafer size	150 mm
thickness	$310 \pm 15 \mu\text{m}$
orientation	<100>
type	P
ingot	FZ
resistivity	>4 k Ωcm
Outer dimensions (after dicing)	97.54 x 97.54 mm ²
second scribe line (see Measurement A)	*96.60mm
Dimensions of Inner edge of bias ring	95.70 x 95.64 mm ²
Strip segments	4
Strip implant, resistivity	N, <20 k Ωcm
length (approximate)	23.86 mm
pitch (round of 0.5 μm)	74.5 μm
implant width	16 μm
Strip bias resistor	Polysilicon
bias resistance (R _{ib})	$1.5 \pm 0.5 \text{ M}\Omega$
Strip readout coupling	AC
Strip readout metal	Pure Aluminum
metal width	20 μm
Strip AC coupling capacitance	>20 pF/cm
Strip isolation	>10xR _b at 300 V
Strip isolation method	Narrow-common p-stop
Gap between strip segments	56 μm (rail region) 70 μm (no rail region)
Microdischarge onset voltage	>600 V
Maximum operation voltage (*)	600 V
Leakage current	<2 $\mu\text{A/cm}^2$ at 600 V
Radiation tolerance	$1.2 \times 10^{15} \text{ 1-MeV } n_{\text{eq}}/\text{cm}^2$

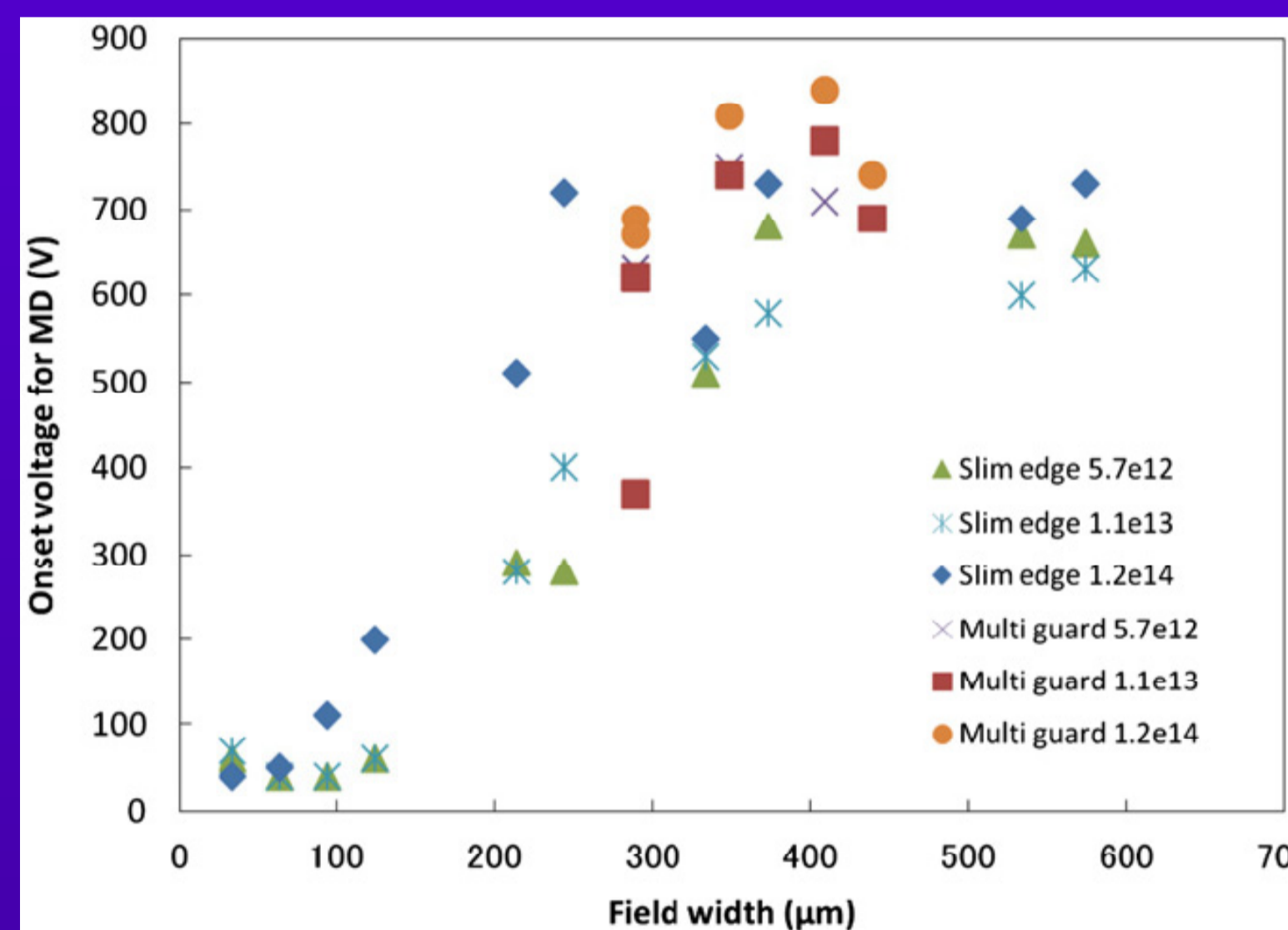


Wafer layout. The main sensor 97.54 mm square is segmented into four in strip length. The strips are biased from one ends through poly Si resistors; the Seg2 and Seg3 strips share a common bias rail. The strips in lower two segments are inclined by 40mrad. Miniature sensors 1 cm square surround the main, where different p-stop structures and strip pitches are examined. The main sensor is a la Z4 where PTP is realized by extending the implant ends closer (20 μm) to the bias rail.

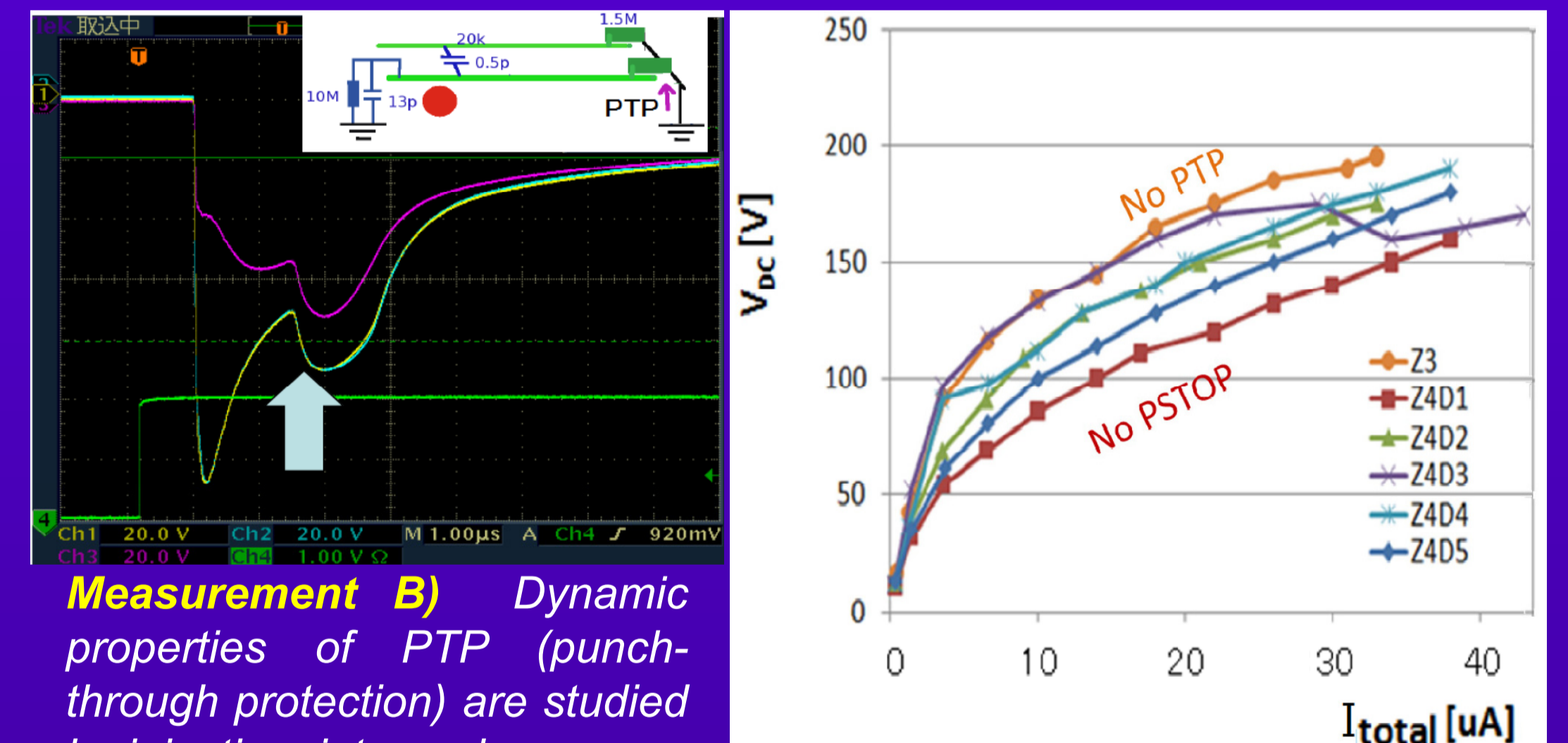
Most of the above requirements have been already met. The fully irradiated sensors provide a signal of 7.5ke⁻ to 12.5ke⁻ at 500 V for various irradiation sources. Since the electronics noise is found to be less than 700e⁻, the signal-to-noise ratio will remain above 10. We continue to monitor such performance in this new prototyping, while accumulating more experience on the sensor fabrication.

Apart from precise values are given in the specifications, two modifications should be noted here since the last prototyping ATLAS07.

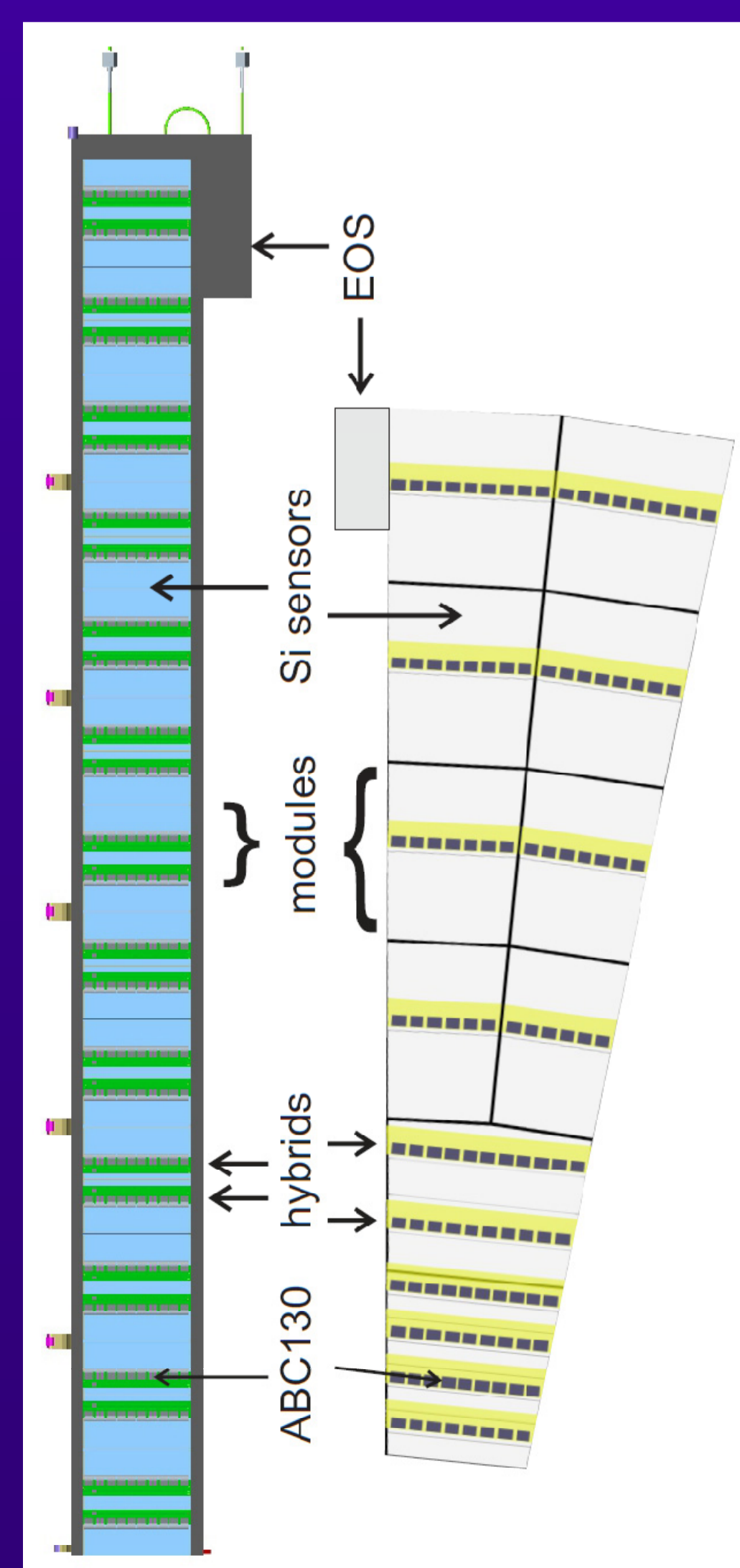
- 2nd scribe line: provides the possibility to narrow the sensor width. The corresponding measurement is given in Measurement A).
- PTP structure: The ends of the implants are covered fully by poly-Si tied to the bias rails. This helps stabilize the function of punch-through protection, as shown in Measurement B).



Measurement A) The micro-discharge onset voltage is plotted as a function of the distance between the bias-ring to the scribed edge, after irradiation. A distance of 400 μm seems possible. Samples: test structures of 1cm square. The 2nd scribe line at 450 μm in width is from this study.



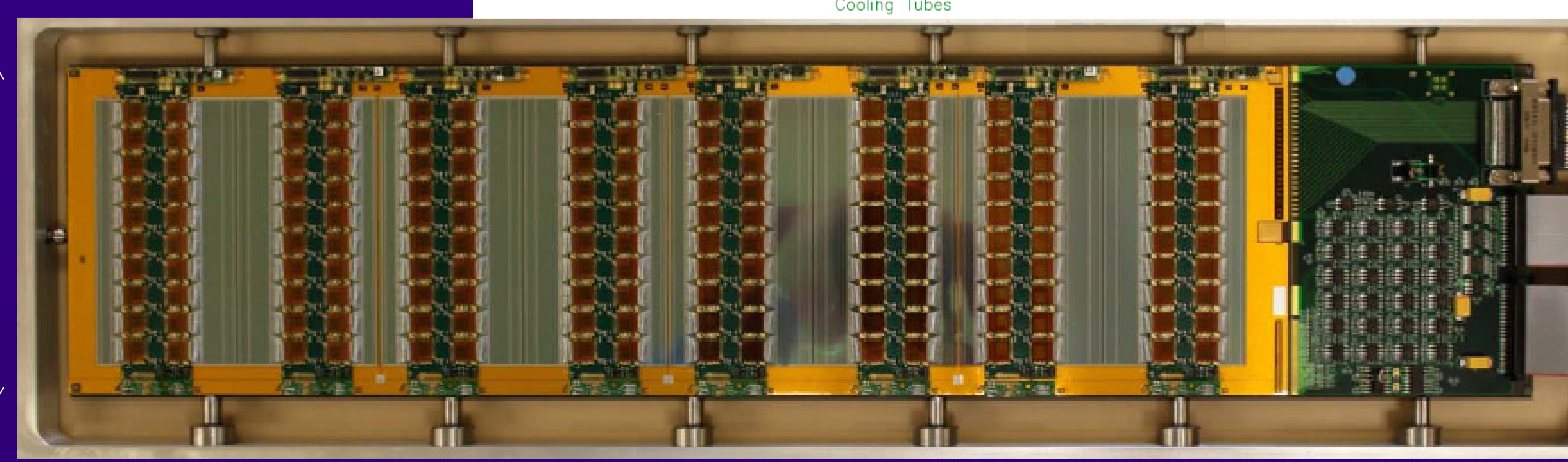
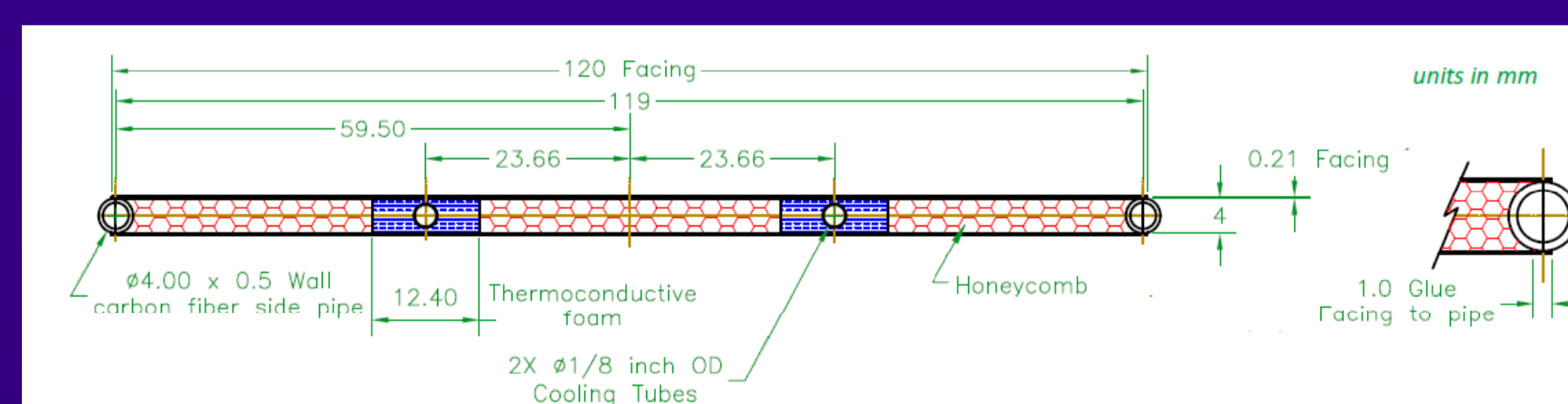
Measurement B) Dynamic properties of PTP (punch-through protection) are studied by injecting intense laser. The implant voltage while PTP is on (up to the arrow shown in the traces. After this point, the impedance changes to increase the implant voltage) is dependent on the laser injection position. For the worst case, i.e. laser injected at and signal read out from the other end of the PTP structure, the maximum voltages are plotted as function of generated current (40 μA ~10⁶mip/pulse). The curves are shown for different gate coverage over the PTP region; D1 is minimum and D5 is full coverage. Samples: test structures of 1 cm square.



Module Design: The barrel part consists of 512 objects (LS) as drawn. Each LS has 13 silicon sensors on each side providing stereo space point reconstruction, hybrids equipped with ABC130 ASICs, and a common interface (EOS) to the outside. For 256 channels per ABC130, 10 chips are lined on a hybrid, and two hybrids are required for each wafer of short strips. For long strip wafers, one hybrid is equipped per wafer. For the end-caps, the technologies are identical but the shapes are trapezoidal having shortest strips of 2.3 cm and longest of 6 cm with the strip pitch varying from 60 to 110 μm . As drawn there are six different silicon sensor types.

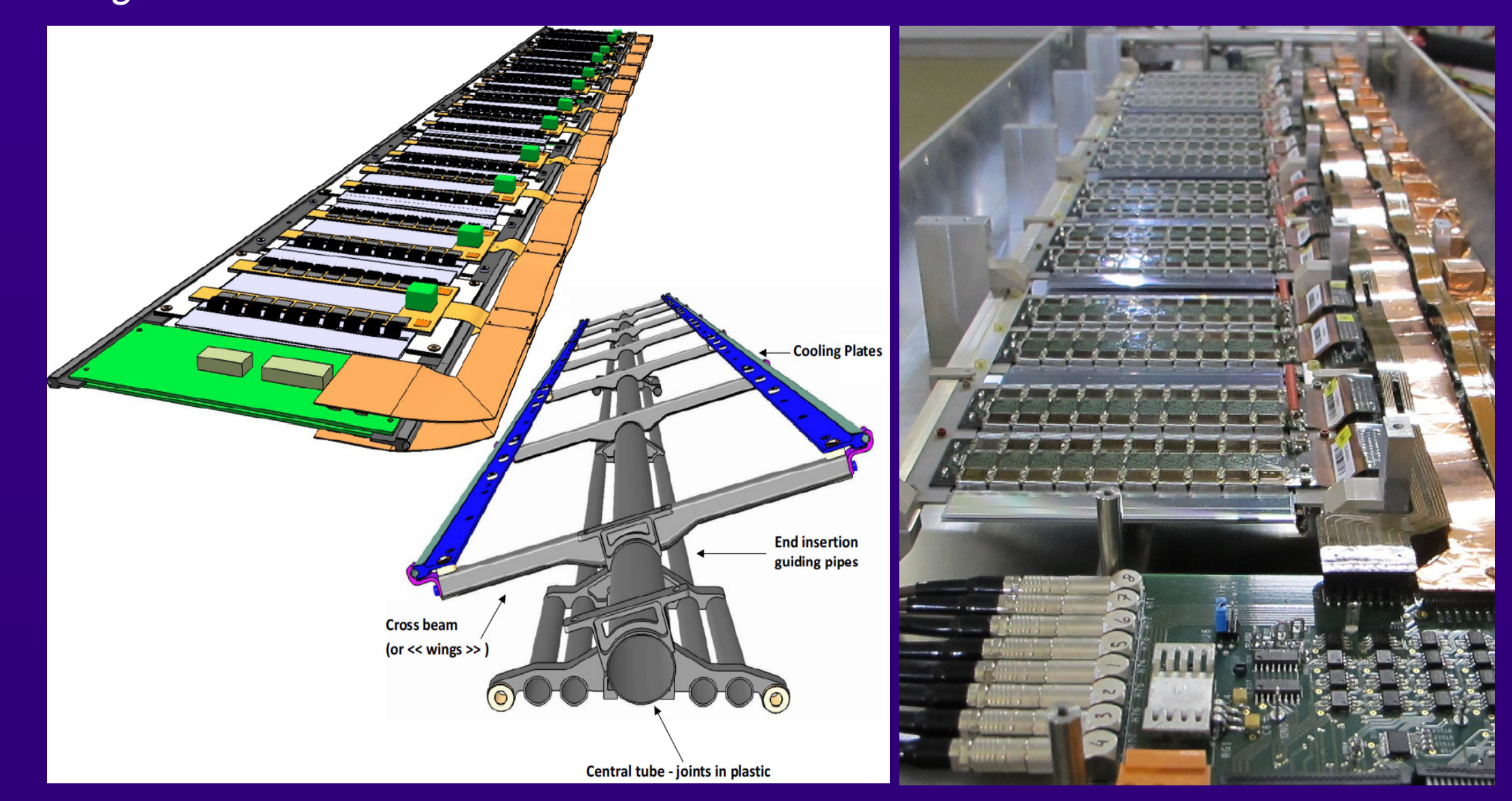
Two module designs (STAVE and SUPER MODULE) have demonstrated successfully their mechanical and electrical capabilities with prototype components (e.g. ABC250).

STAVE (baseline design) : Wafers and bus cables underneath are glued on a light structure with integrated cooling (see drawing below). The bus cables provide ASIC communication to the EOS (end-of-stave) module. The stave is supported sideway as shown in the prototype photo.



"Stavelet" shorter version of full Stave (ABC250 chips)

SUPER MODULE (optional design) : Two wafers are glued on a baseboard, to which the hybrids are glued bridging over the wafers. 13 such modules are integrated into a super-module using a light weight frame. The communication is provide through a bus cable running alongside the module.



Concept and a prototype (8 modules fill in a super module frame)