Thin n-in-p pixel sensors and the SLID-ICV vertical integration technology for the ATLAS upgrade at HL-LHC

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In collaboration with Fraunhofer EMFT

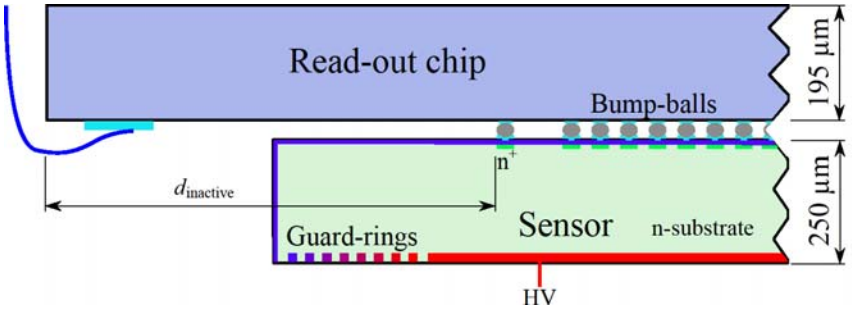
International Workshop on Semiconductor Pixel Detectors for Particles and Imaging, Inawashiro, Japan

PIXEL2012

R&D towards a 3D integrated demonstrator module

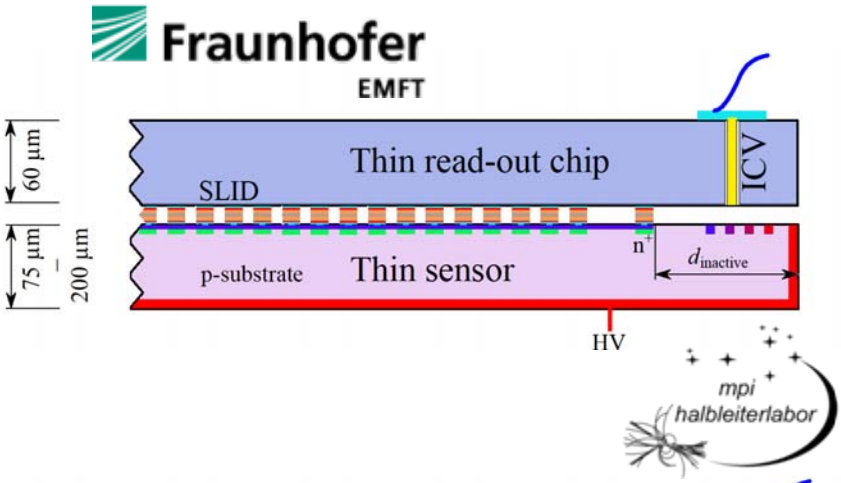
R&D towards a fully 3D integrated demonstrator pixel assembly allowing for a minimized inactive area:

- from the present ATLAS pixel module design ...

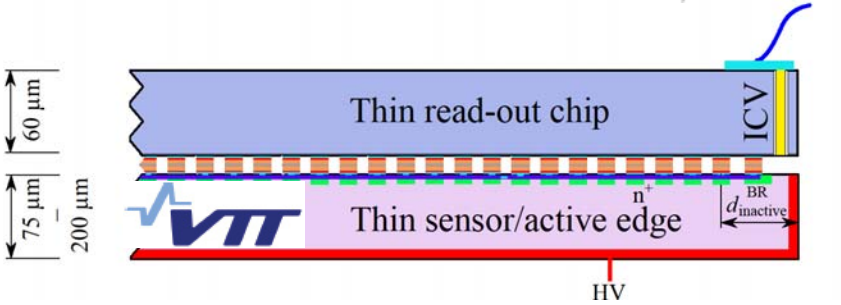


- ... to a 3D integrated assembly with thin sensors (75-150 µm range) interconnected with the Solid Liquid Interdiffusion technique, SLID, to thin chips (down to 60 µm thickness)

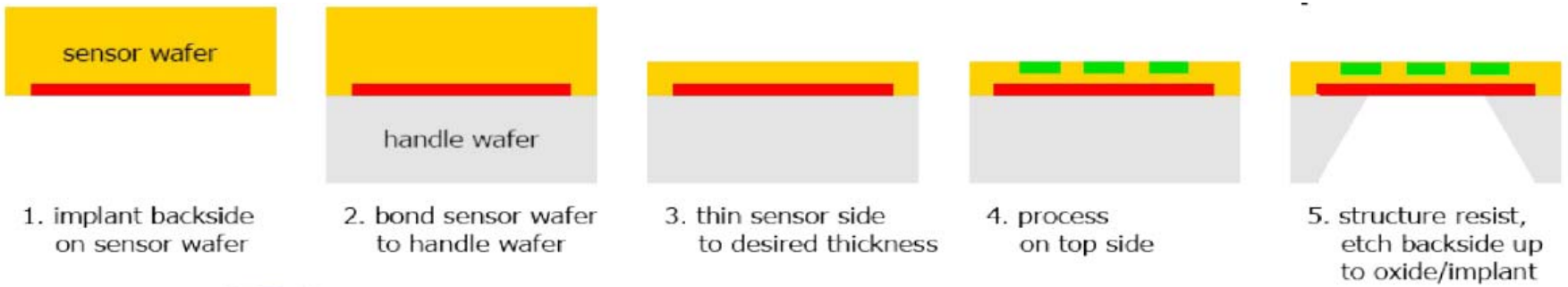
- Through Silicon Vias (TSV) etched in the read-out chip on the front-side on the positions of the original wire bonding pads to route signal and services to the ASIC backside

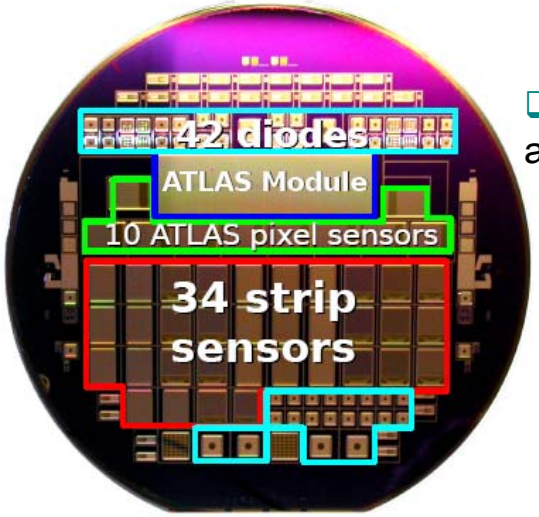


- Production of active edge sensors to achieve a fully four-side buttable module, in collaboration with VTT (Finland)

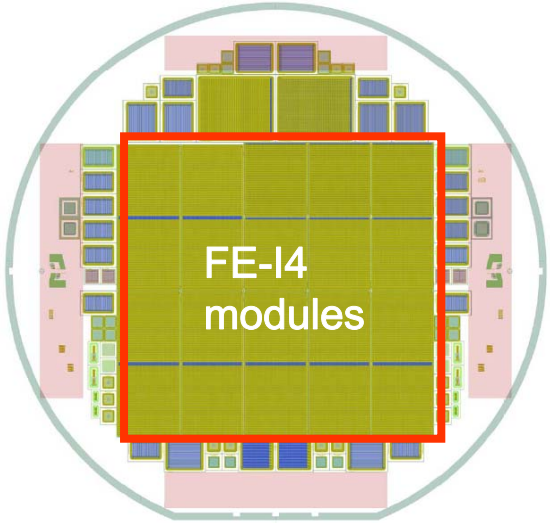


Thin pixel technology at MPP-HLL





- 75µm and 150µm active thickness



- 150µm active thickness

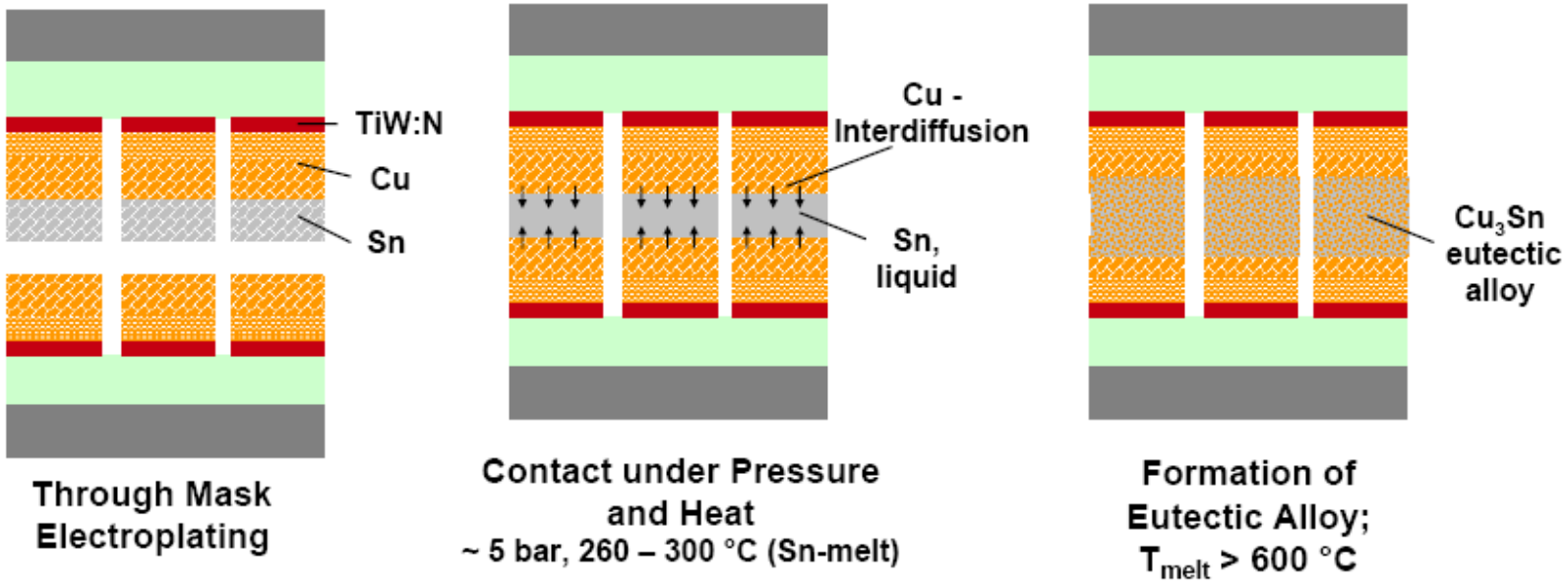
- n-in-p 6“ wafers with ATLAS FE-I3 compatible sensors
- 75 µm thick sensors interconnected with SLID to FE-I3 chips, thinned down to 200 µm, at EMFT

- n-in-p 6“ wafers with ATLAS FE-I4 sensors (pitch 50 µm x250 µm)
- IBL compatible GR → 450 µm dead edge
- Interconnected to FE-I4 chips with bump-bonding at IZM

EMFT SLID Process

Metallization SLID (Solid Liquid Interdiffusion)

Fraunhofer EMFT



Through Mask Electroplating

Contact under Pressure and Heat
~ 5 bar, 260 – 300 °C (Sn-melt)

Formation of Eutectic Alloy;
T_{melt} > 600 °C

- Alternative to bump bonding (less process steps “lower cost” (EMFT)).
- Small pitch possible (~ 20 μm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.
- For the analysis of the interconnection efficiency: arXiv:1202.6497

EMFT SLID Process

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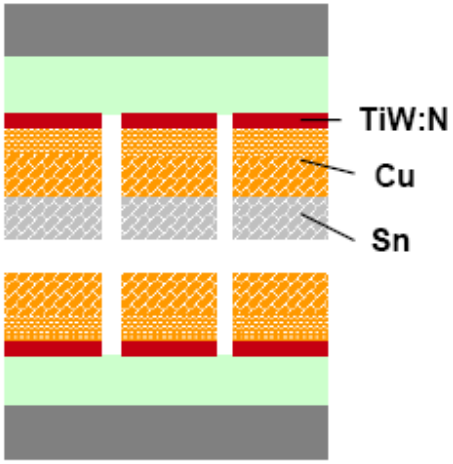
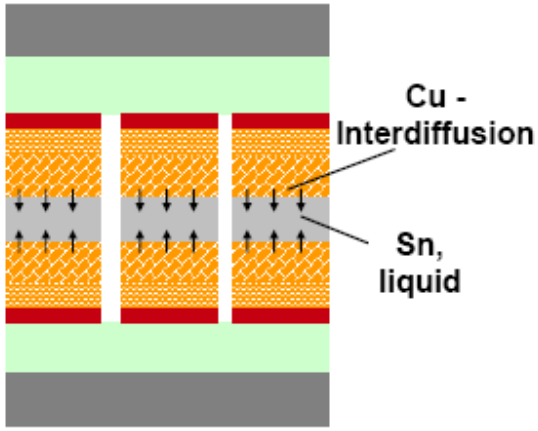


Through Mask Electroplating



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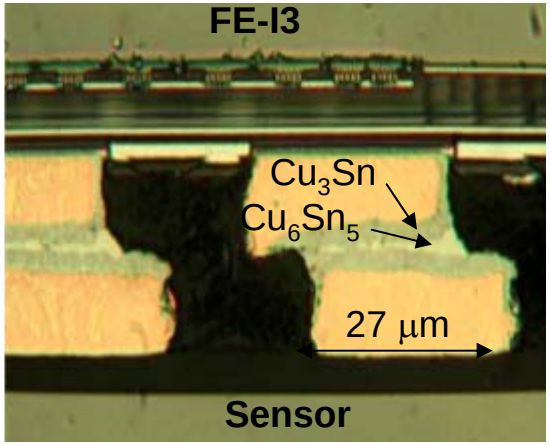

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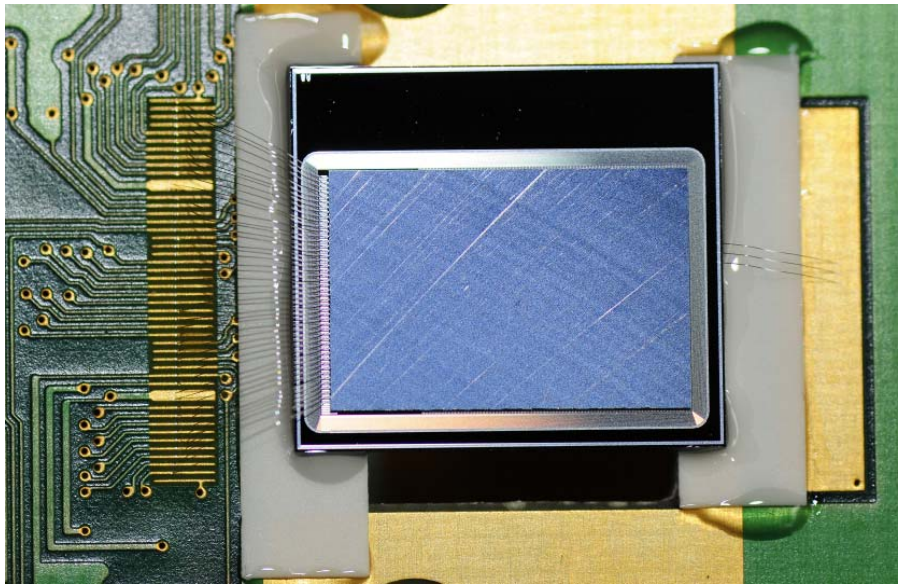
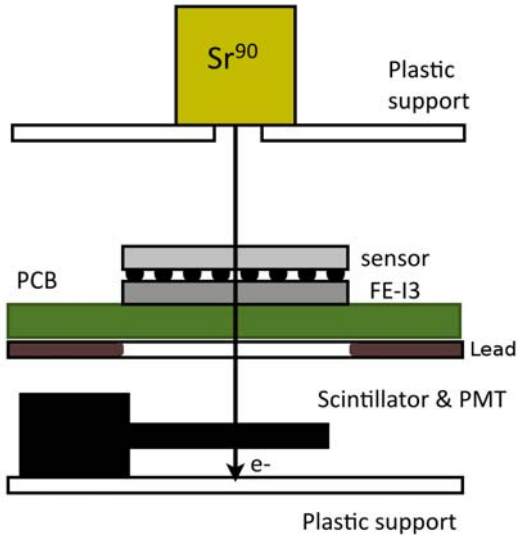
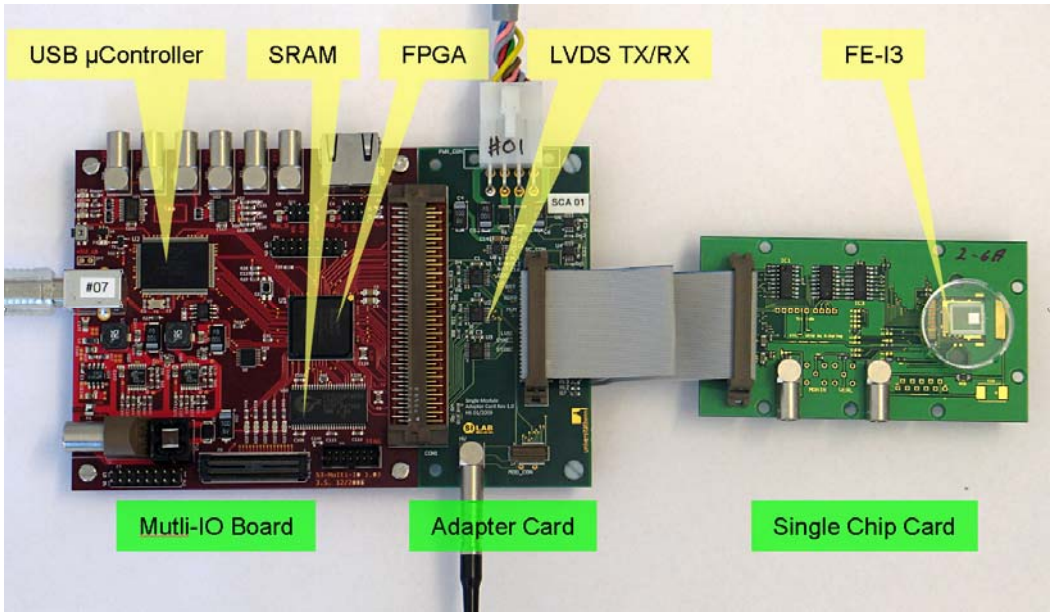
Set-up for the pixel module characterization



- Pixel modules glued and wire-bonded to a detector board designed by the University of Bonn in two versions for FE-I3 and FE-I4
- Measurements performed with the ATLAS USBPix read-out system

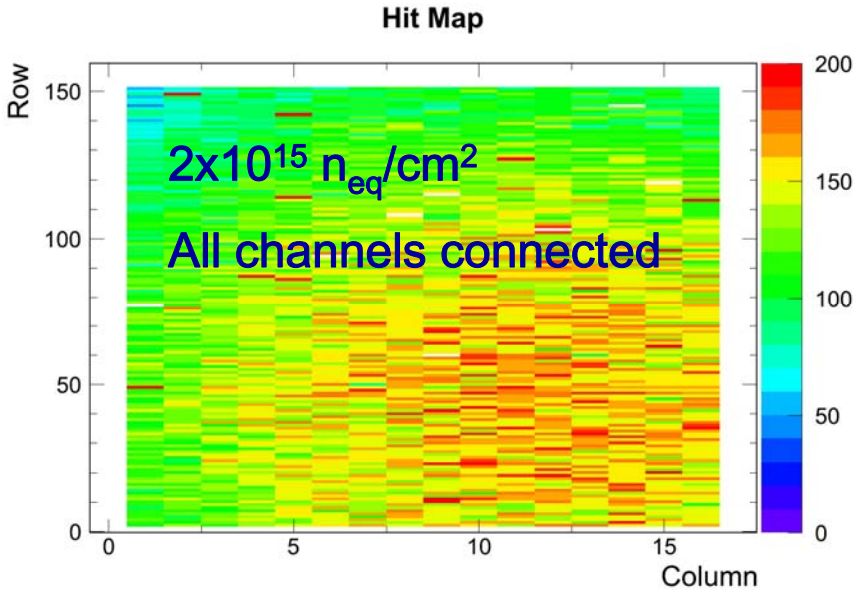


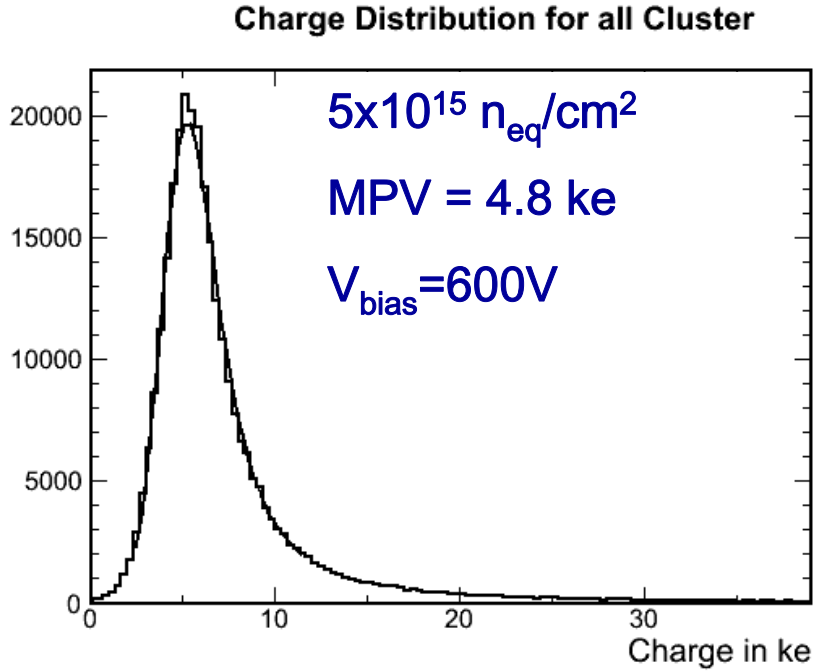


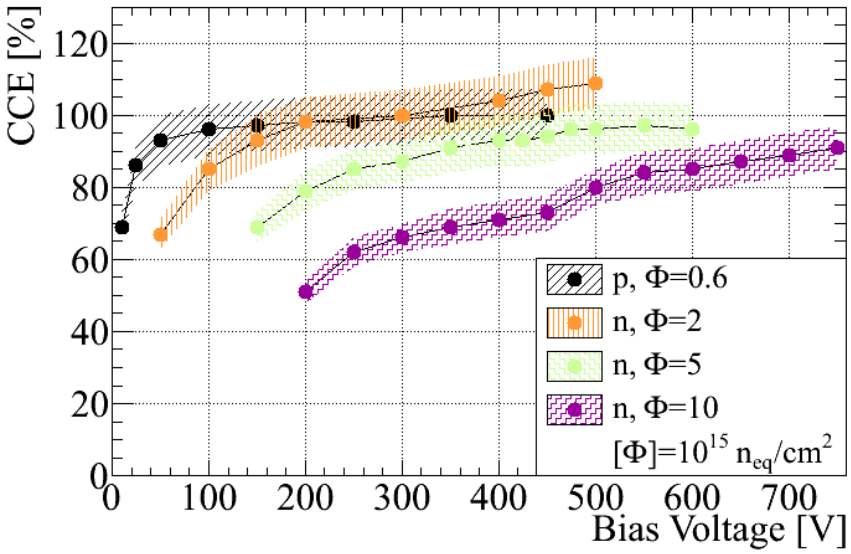
Post irradiation characterization of SLID modules

- Good Charge Collection efficiency after irradiation up to 10^{16} n_{eq}/cm^2
- Number of unconnected channels stable after irradiation and multiple thermal cycles (+20°C → -50°C)

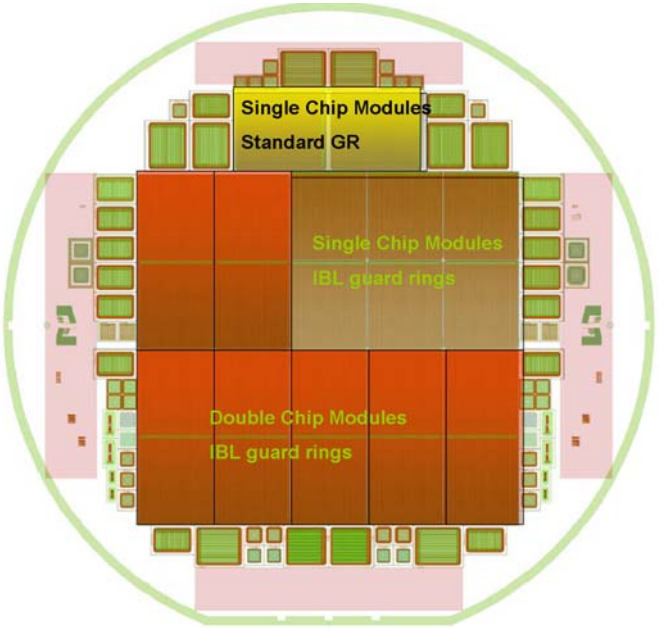
SLID interconnection is radiation hard and withstands thermal cycling





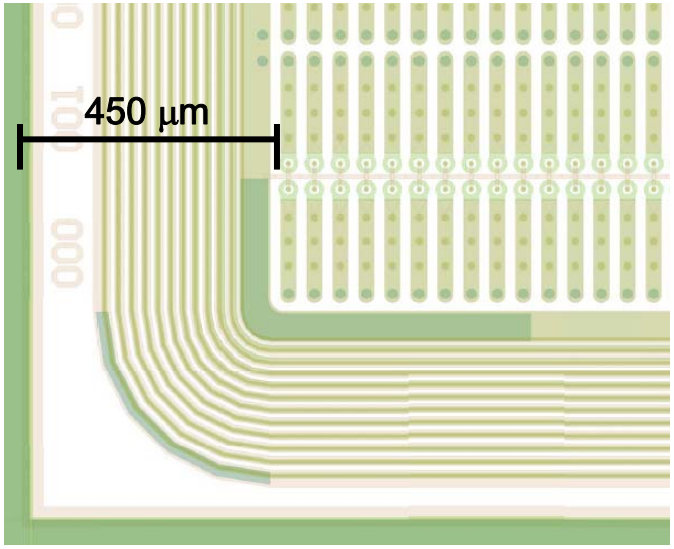


MPP-HLL SOI2 production: FE-I4 sensors, 150 μm thick



Pixel sensors with FE-I4 geometry

- Single and Double Chip Modules
- SCM 1.7x2.1 cm^2 dimensions
- Pitch 25x250 μm^2
- 450 μm inactive edge (IBL specifications)



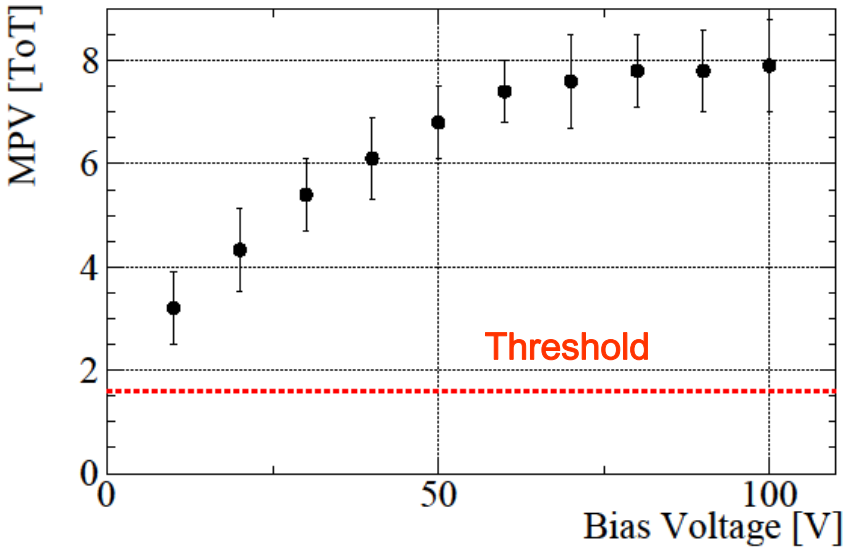
11 Single Chip Modules analyzed

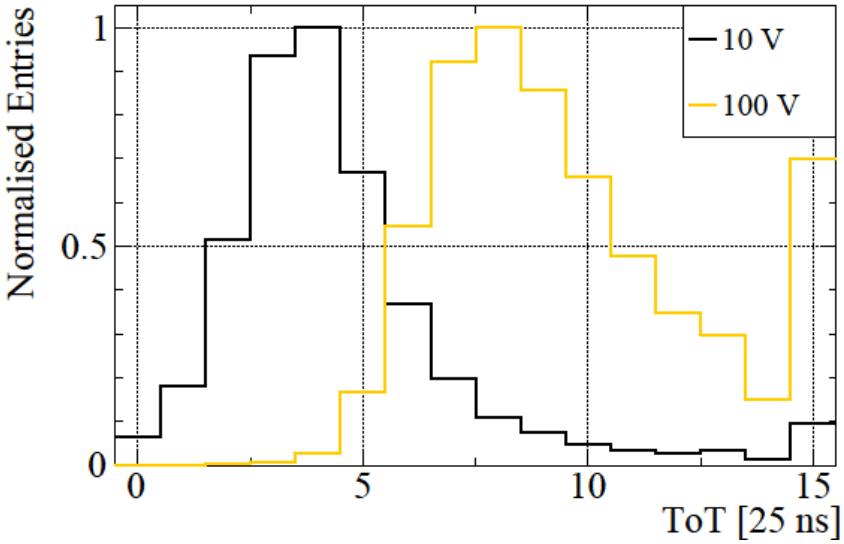
- Interconnection by bump-bonding at IZM
- 1 module irradiated at $2x10^{15}$ $n_{eq/}$ cm^2 at KIT with 25 MeV protons
- 3 modules irradiated at $4x10^{15}$ $n_{eq/}$ cm^2 in Los Alamos with 800 MeV protons

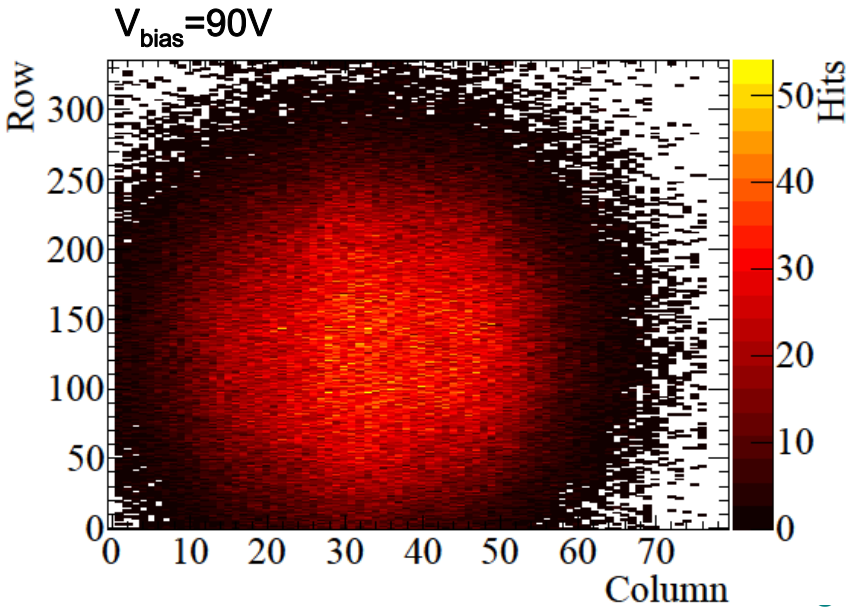
FE-I4 module characterization before irradiation

^{90}Sr Scan with Threshold=1600 e , Tuning of 10 ToT for 15 ke

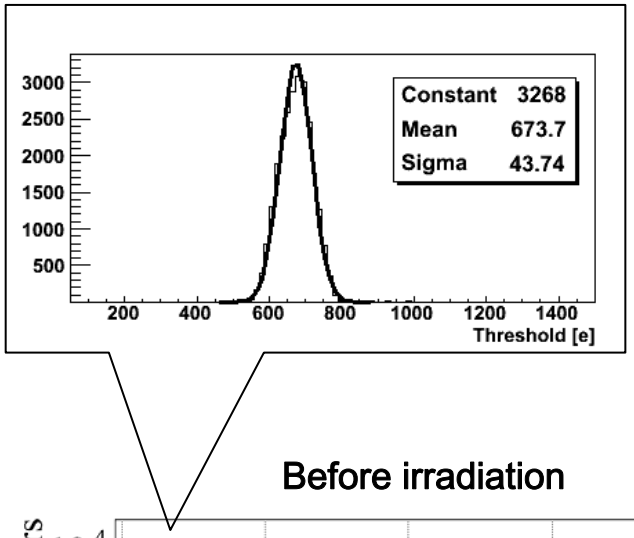
- FE-I4 chip with 4-bit resolution ToT
- No injection capacitance measurement circuitry was implemented in FE-I4A → difficoult determination of the absolute charge calibration
- MPV compatible with 12ke, value expected with a thickness of 150 μm





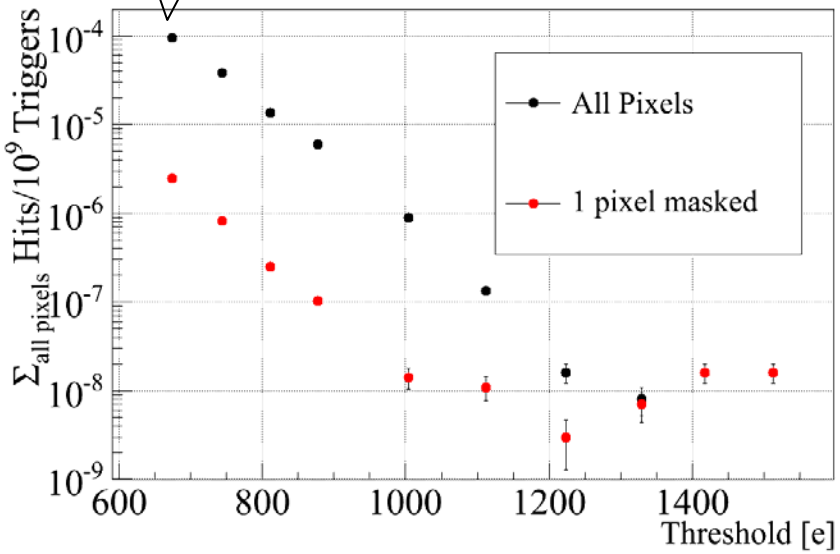


FE-I4 n-in-p modules: noise occupancy at low thresholds

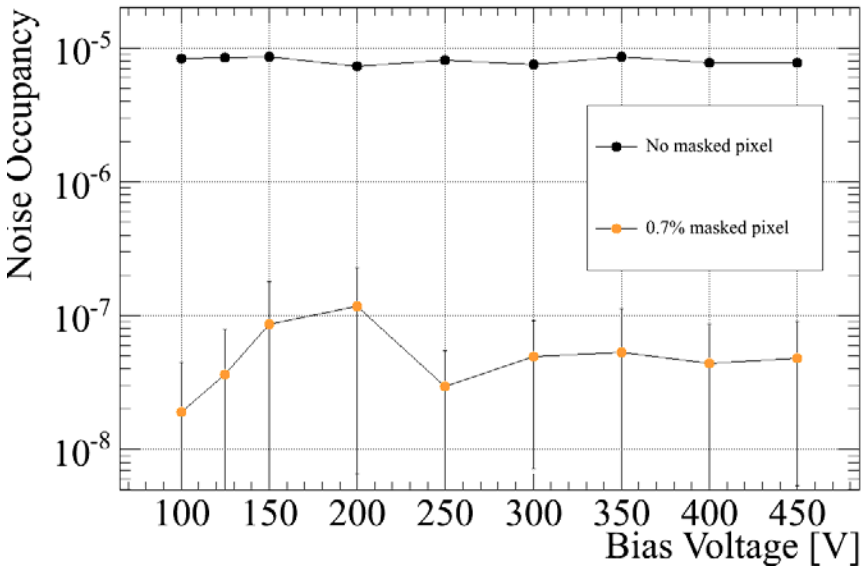


- FE-I4 chip: very low noise and occupancy also at reduced threshold values
- Low thresholds achievable with the FE-I4 chip help to deal with small charges after irradiation

Before irradiation



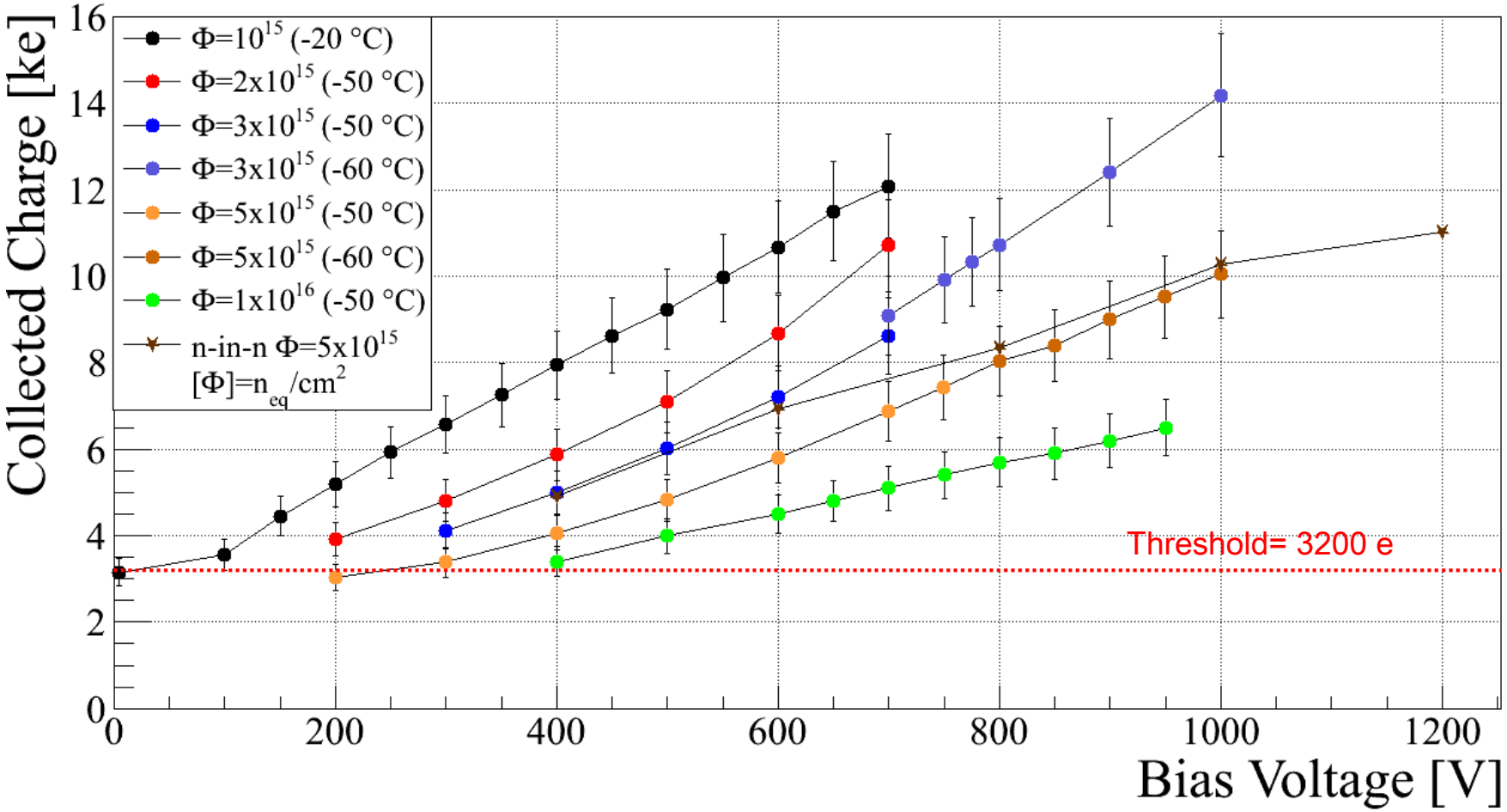
Φ=4x10^15 n_eq cm^-2 , Threshold = 1500 e



CC for FE-I3 n-in-p pixels, 285 μm thick

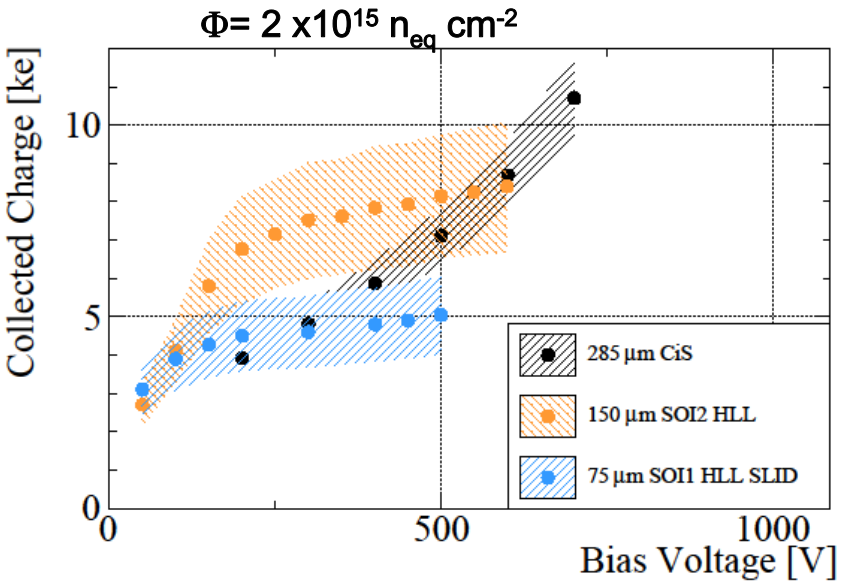
Charge collection summary of neutron irradiated CiS n-in-p modules, ^{90}Sr scan

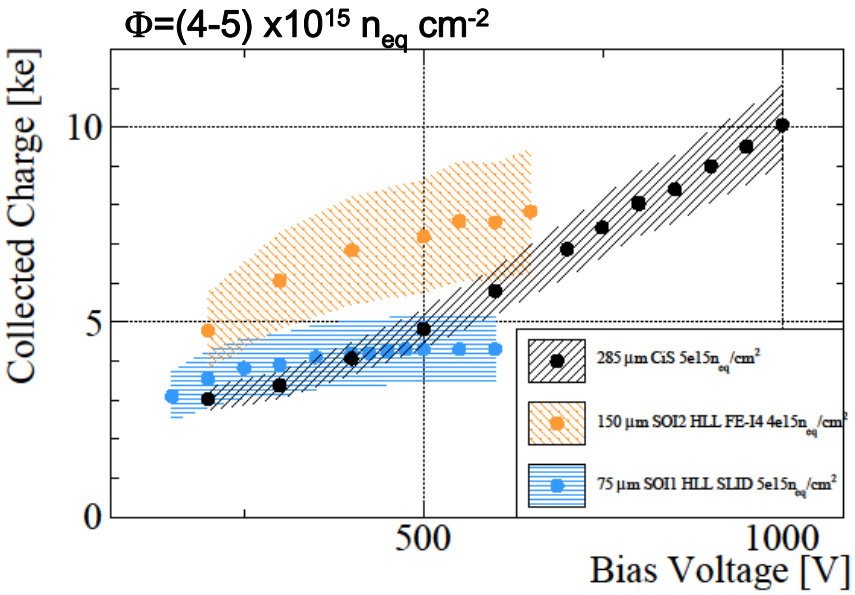
Ch. Gallrapp, A. La Rosa, A. Macchiolo, R. Nisius, H. Pernegger, R.H. Richter , P. Weigell

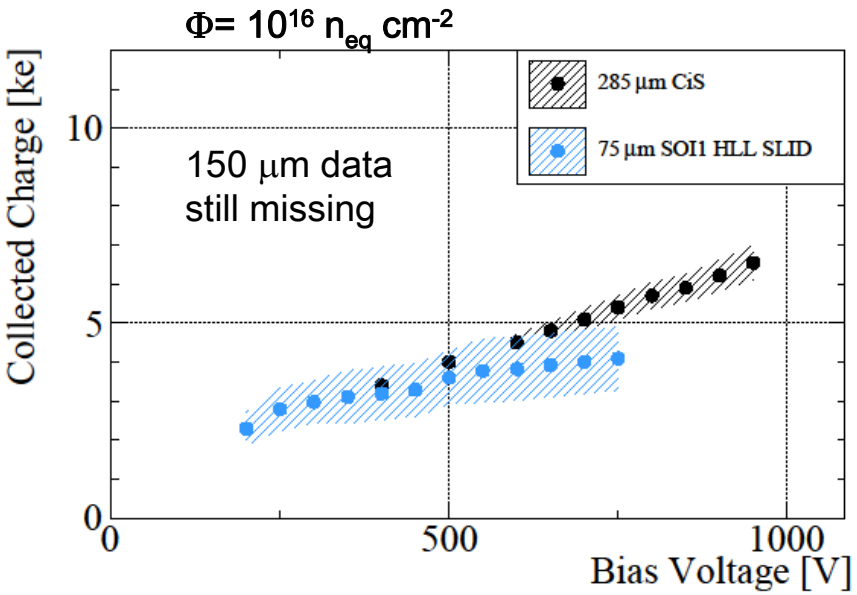


C. Gallrapp et al., "Performance of novel silicon n-in-p planar Pixel Sensors ", Nucl. Instrum. Meth. A679 (2012) 29

Comparison of CC for n-in-p pixels of different thickness



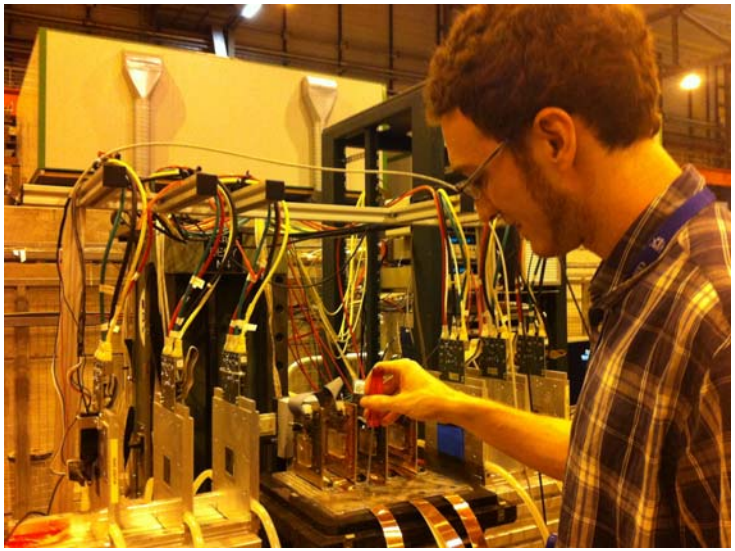




Higher charge with 150 µm thick sensors up to a fluence of Φ=(4-5)x10^{15} n_{eq} cm^{-2}

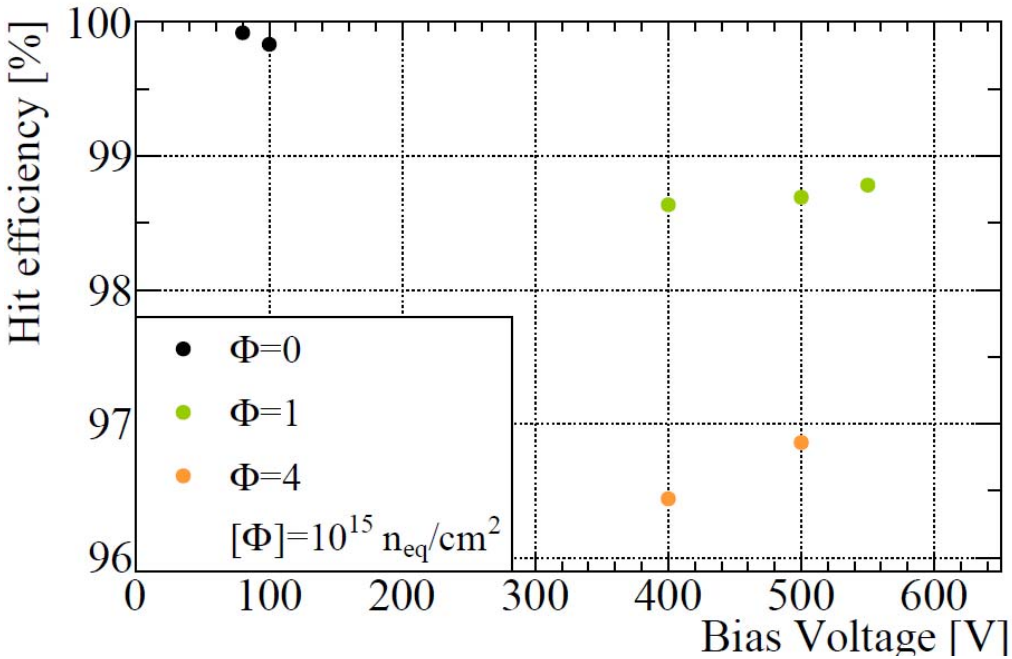
At higher fluences the charge of thin and thicker sensors tend to equalize

Test-beam results for FE-I4 modules



- Test-beams with EUDET telescope
- 120 GeV pions at CERN-SPS and 5-6 GeV/c electrons at DESY
- Many thanks to the PPS test-beam crew

S. Altenheiner, M. Backhaus, M. Bomben, K. Dette, M. Ellenburg, D. Forshaw, C. Gallrapp, M. George, I.~Gregor, J. Janssen, J. Jentzsch, R. Klingenberg, A. Kravchenko, T.Kubota, A.Macchiolo, T.Plümer, R.Nagai, B.Ristic, I. Rubinskiy, A. Rummler, Y.Takubo, S.Terzo, K. Toms, R. Wang, Y. Unno, P. Weigell, J. Weingarten



Good tracking performance of FE-I4 modules with 150 μm thick sensors up to a fluence of $\Phi=4\times10^{15}$ n_{eq} cm^{-2}

Moderate Vbias applied, up to 600V

FE-I4 module hit efficiencies

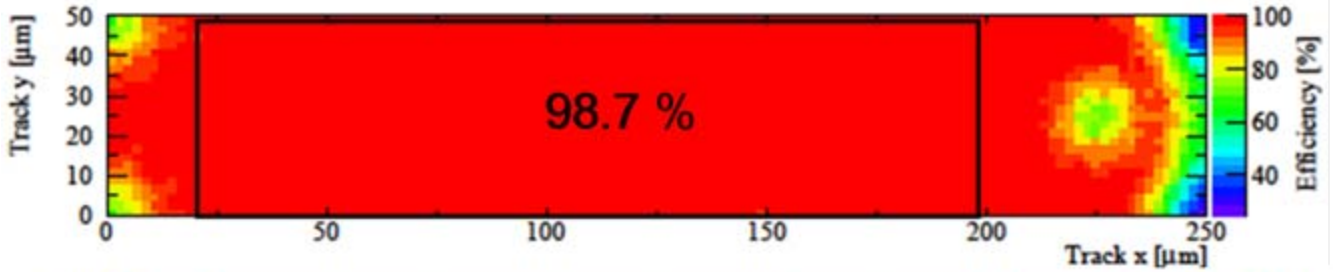
Hit efficiency of the module projected in one single pixel cell,
Eudet telescope, 120 GeV pions at CERN-SPS

Design of the
FE-I4 pixel

Φ=4x10^{15} n_{eq} cm^{-2}

400 V

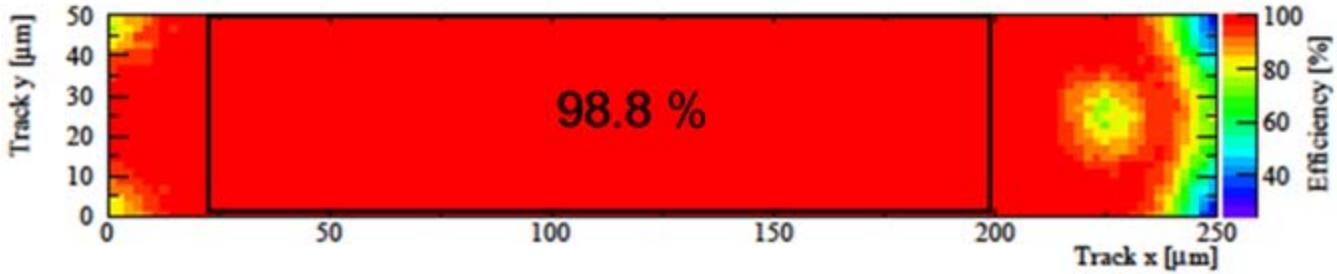
Global eff.= 96.5%



Φ=4x10^{15} n_{eq} cm^{-2}

500V

Global eff.= 96.9%



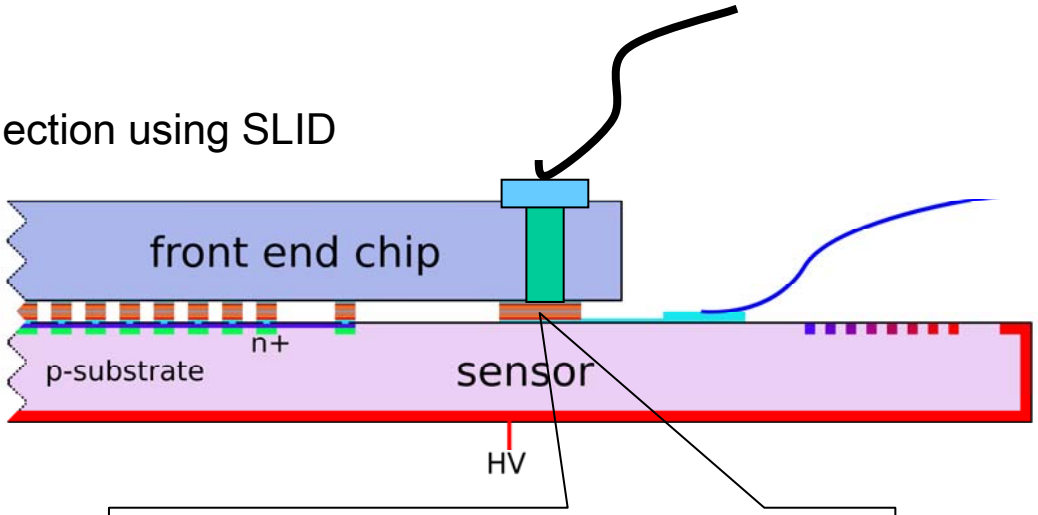
- Main loss of efficiency in the bias dot and in the bias rail → problem is relevant only for perpendicular tracks, as in this case

MPP 3D R&D Program: Through Silicon Vias

❑ TSV etched in the read-out chip on the front-side on every wire bonding pad of the FE-I3 chip to route signal and services to the ASIC backside

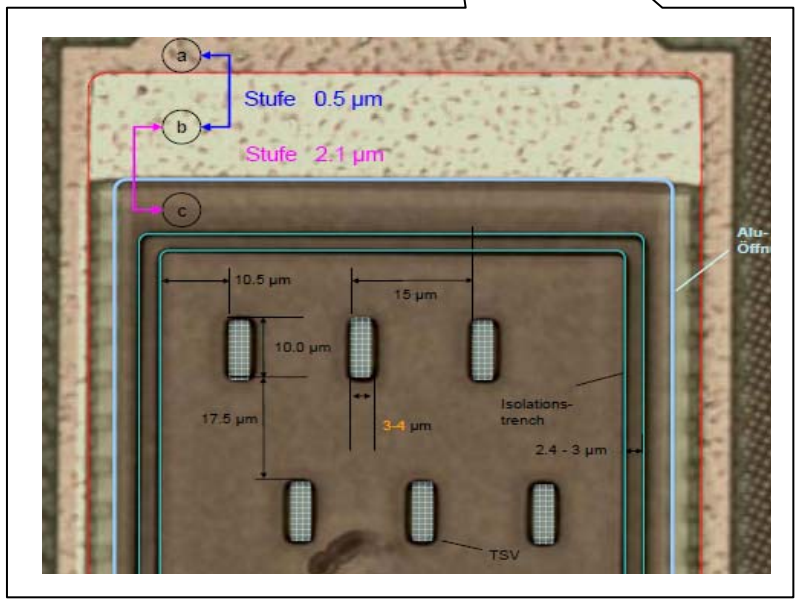
- ASIC thinned to 60 μm
- thin sensors /ASIC interconnection using SLID

Fraunhofer EMFT



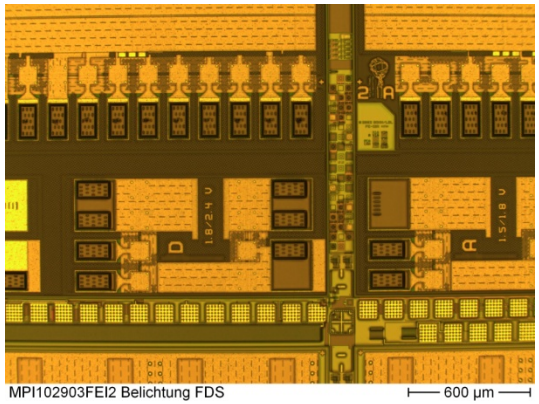
❑ Processing sequence:

- Via-etching in Bosch-process, TSV cross-section of 3x10 μm^2
- insulation with TEOS (low T)
- filling of vias with Tungsten
- attachment to handle-wafer on the top side and thinning to desired thickness of chip ~ 60 μm
- redistribution layer on the backside
- SLID-interconnection to sensor wafer.

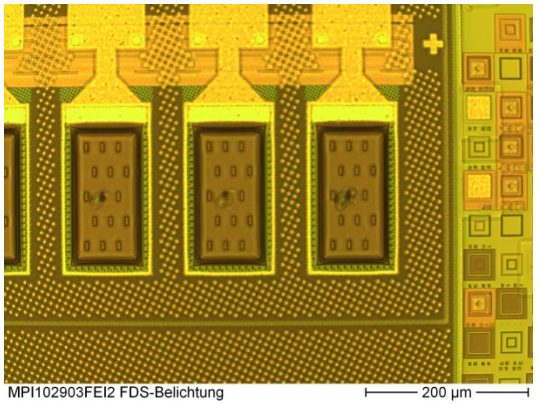


MPP 3D R&D Program: Through Silicon Vias

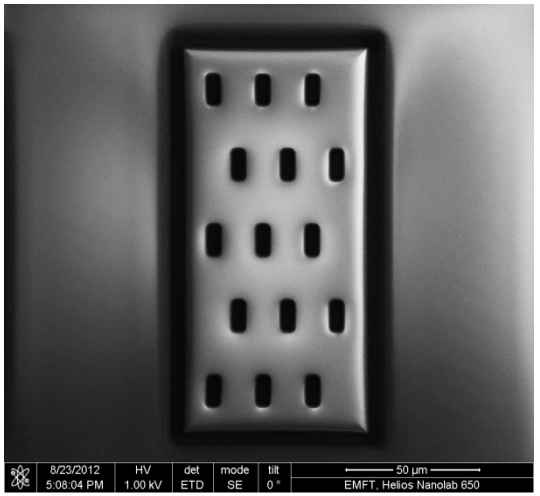
- Processing status on the first hot wafer: etching of the dielectric layers accomplished



total view pad array & test field



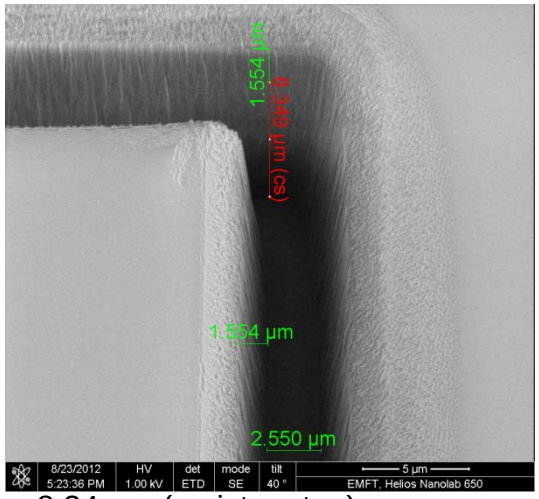
total view pad array



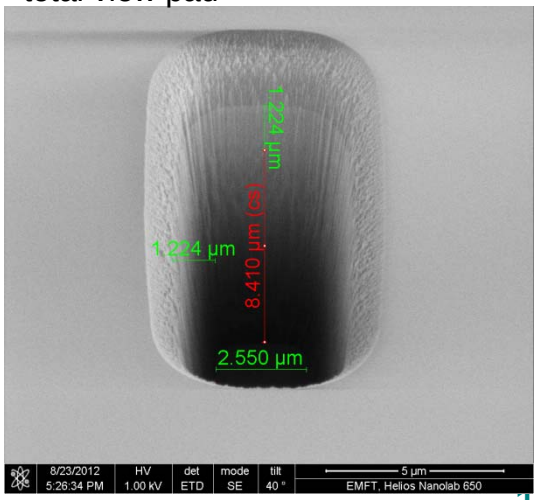
total view pad

Fraunhofer EMFT

- Very narrow TSV allows for their possible use to connect every single pixel

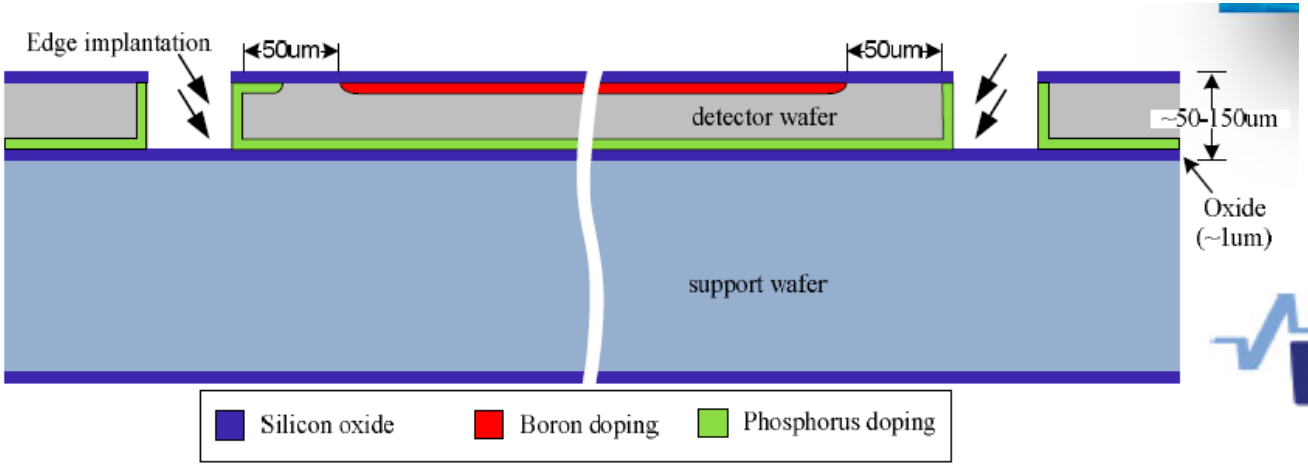


8.34 µm (resist on top)



8.4 µm (resist on top)

Active edges with planar n-in-p sensors



n-in-p pixels at VTT: active edge process with back-side implantation extended to the edges

See J. Kalliopuska talk "Results of a Multi Project Wafer Process of Edgeless Silicon Pixel Detectors"

- Multi-project run at VTT including ATLAS FE-I3 and FE-I4 n-in-p pixel sensors with different edge design
- 100 μm and 200 μm active thickness →together with the active edges makes these sensors very attractive candidates for the inner layers in Phase II
- p-spray isolation method transferred from HLL to VTT
- Flip-chipping performed at VTT after bump-deposition on the FE-I4 chip wafers

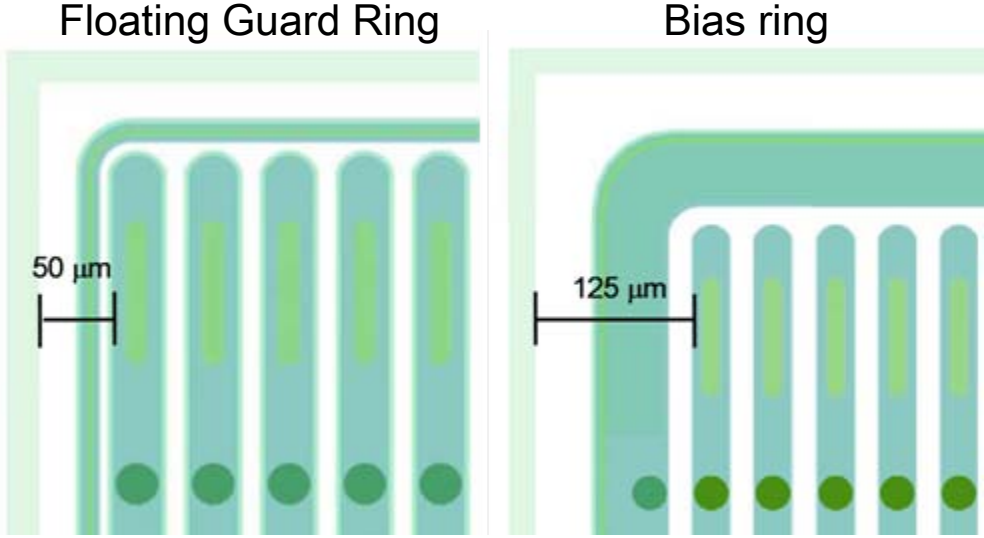
Active edges with planar n-in-p sensors

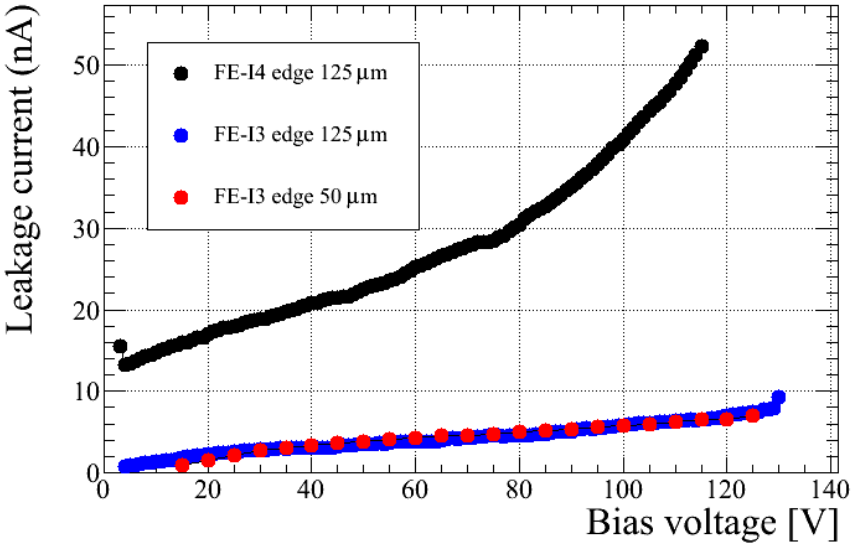
100 μm thickness

V_{break}~120V

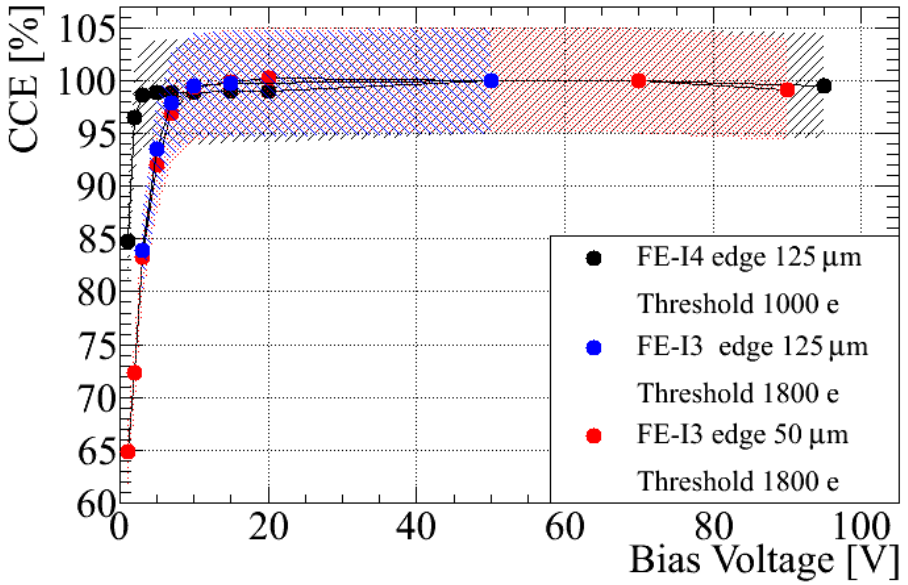
V_{depl} ~7-10 V

Charge ~ 6±1 ke

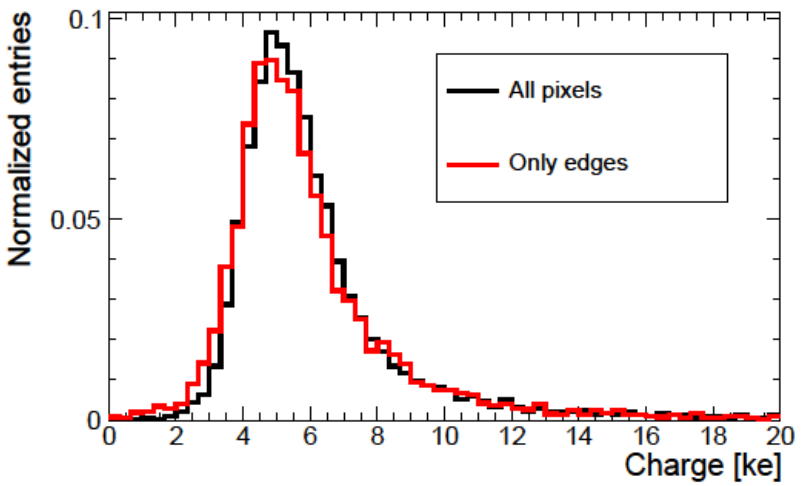


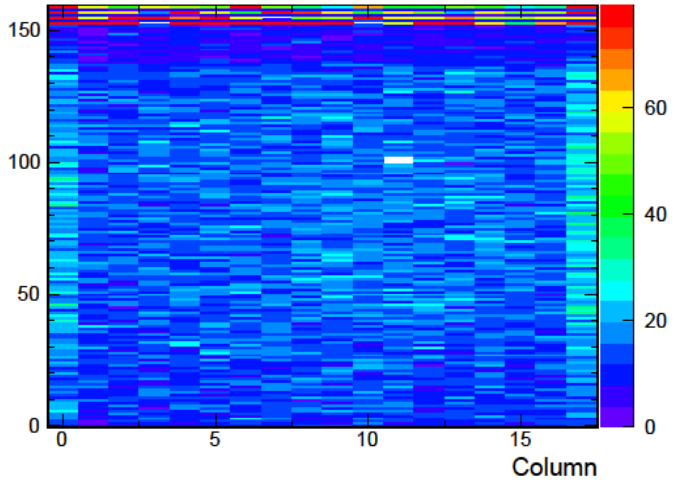


CCE with ^{90}Sr scans

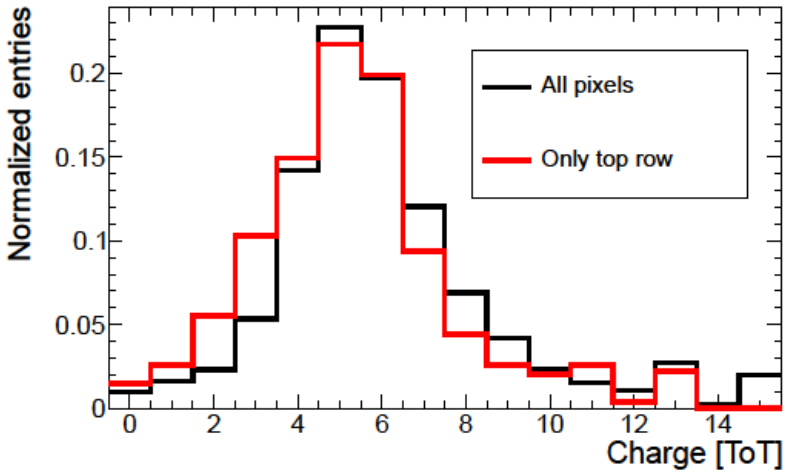


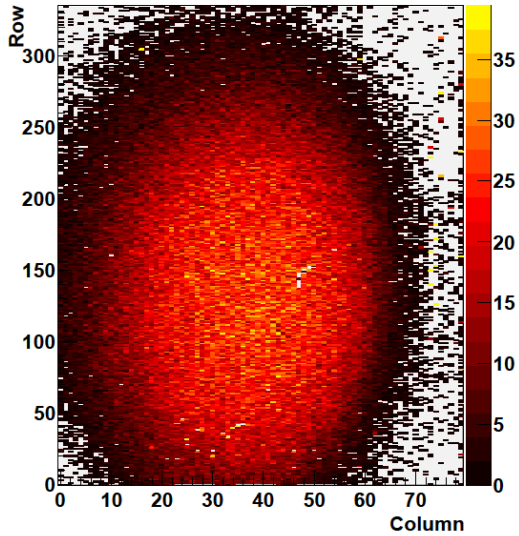
Active edges with planar n-in-p sensors





FE-I3
50 μm edge
V_{bias}=15 V





FE-I4
125 μm edge
V_{bias}=15 V

- Edge pixels show the same charge collection properties as the central ones
- Plan to study the hit reconstruction efficiency at the edges with test-beam before and after irradiation

Conclusions and Outlook

- Good performance of pixel detectors with thin n-in-p sensors irradiated up to a fluence of $\Phi=10^{16}$ n_{eq} cm^{-2} , demonstrated in measurements with radioactive sources and beam tests.

- Low thresholds achievable with FE-I4 chip and thin n-in-p pixels help to obtain good tracking performance also with small signals.

- SLID interconnection technology proved to be stable after irradiation, up to $\Phi=10^{16}$ n_{eq} cm^{-2} . Plans to extend the tests with further runs on FE-I3 and FE-I4 wafers.

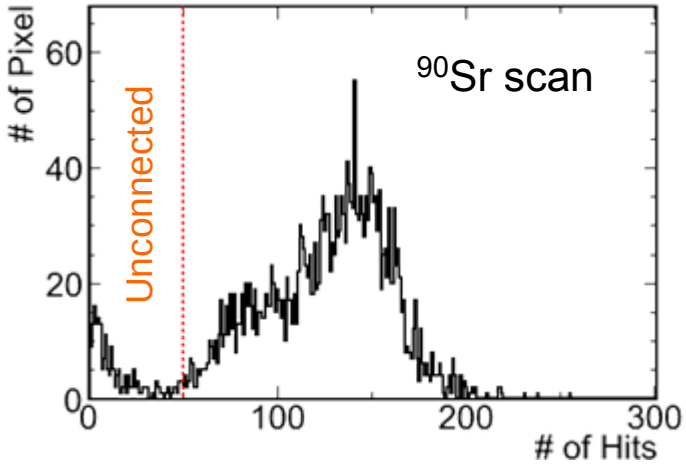
- TSV with narrow cross-sections are being etched on FE-I3 wafers. If applied to a TSV compatible chip, this technique will allow for four-side buttable modules.

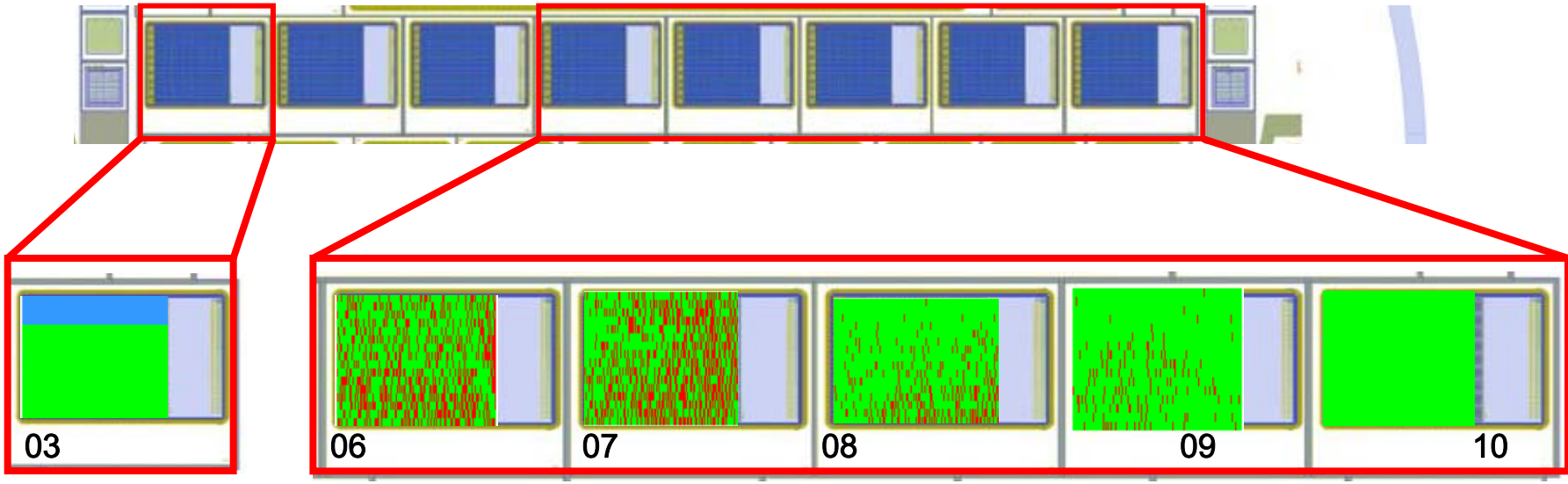
- First active edge pixels, 100 μm thick, interconnected to FE-I3 and FE-I4 chips. Preliminary tests show good behavior of the modules down to an inactive side of 50 μm → very thin pixels with active edges represent very good candidates for the inner layers of the pixel detectors at HL-LHC.

Back-up slides

Overview of SLID interconnection efficiency

Chip	Unconn. Pixels	Efficiency [%]
3	0	100
6	731	70
7	713	71
8	274	89
9	134	94
10	0	100





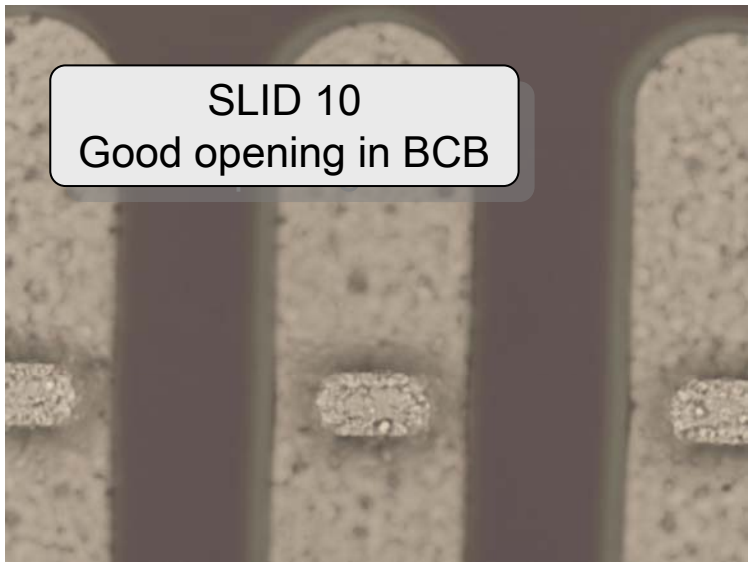
Connected channel

Dead columns

Unconnected channel

A. Macchiolo et al, "SLID-ICV Vertical Integration Technology for the ATLAS Pixel Upgrades", arXiv:1202.6497

Problem with contact opening in BCB passivation



- BCB (BenzoCycloButhene) passivation deposited to planarize the sensor surface before Cu and Sn electroplating

- Badly defined BCB contact openings observed in 2 sensor wafers not yet electroplated → pattern fully compatible with the distribution of unconnected channels in the modules

Unconnected channels are not an intrinsic SLID problem!

Problem cured for the remaining wafers with a descum process of BCB using a SF_6 plasma at IZM

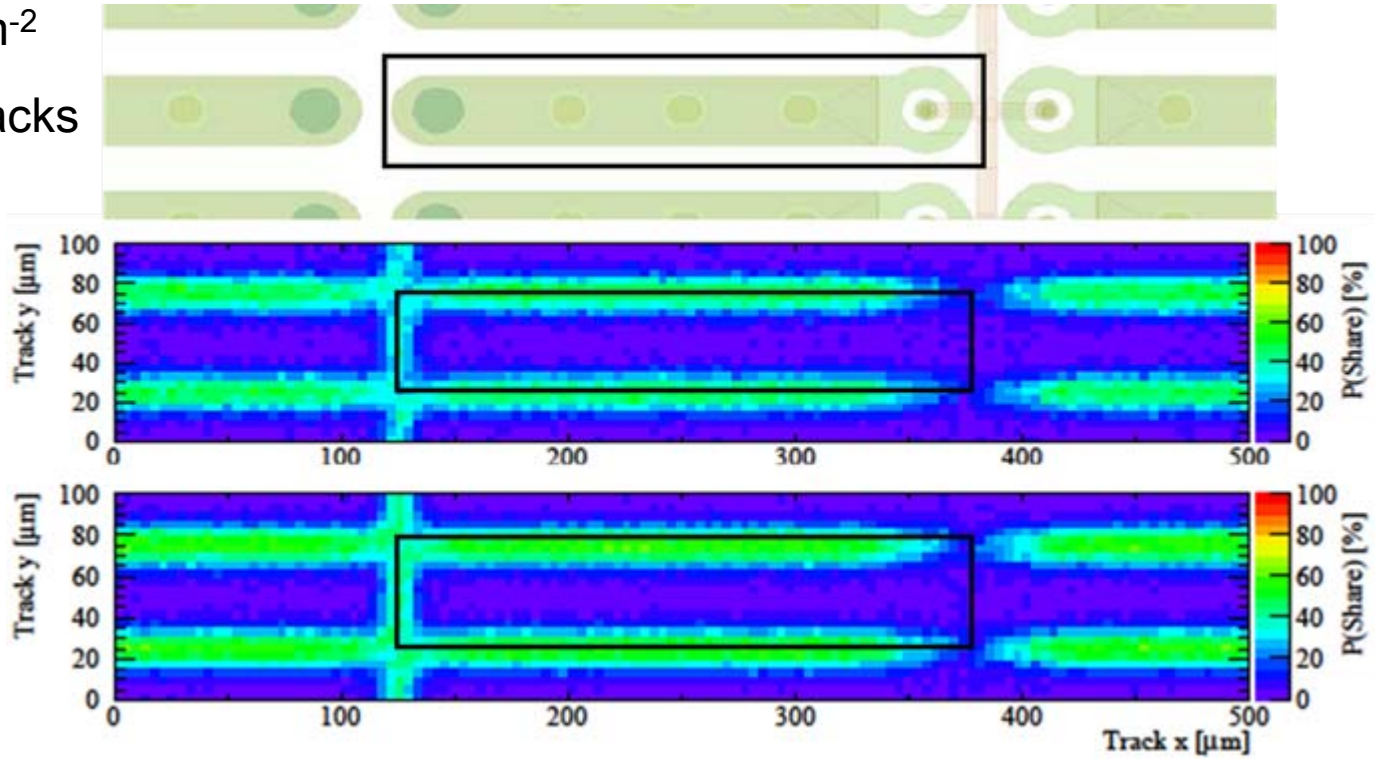
FE-I4 module charge-sharing

Φ=4x10^{15} n_{eq} cm^{-2}

perpendicular tracks

400V

500V



average cluster size

1.17 hits @ 400V

1.2 hits @ 500V

Cluster size	Fraction @ 400V [%]	Fraction @ 500V [%]
1-hit	81	78.6
2-hit	16	19.7
3-hit	1.1	1.1