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Thin n-in-p pixel sensors and the SLID-ICV vertical integration technology for the ATLAS upgrade at HL-LHC

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The R&D activity here presented is focused on the development of a new module concept for the upgrade of the ATLAS pixel system at the High Luminosity LHC (HL-LHC). It employs thin pixel sensors together with a novel vertical integration technology offered by the Fraunhofer Institute EMFT in Munich, consisting of the Solid-Liquid-InterDiffusion (SLID) interconnection, which is an alternative to the standard bump-bonding, and Inter Chip Vias (ICV) for routing signals vertically through the readout chips.
Two productions of thin pixel sensors, with an active thickness of 75 um and 150 um, were completed using a process developed at the Semiconductor Laboratory of the Max-Planck-Institute for Physics (HLL) and connected to the FE-I3 and FE-I4 ATLAS read-out chips, respectively.
Due to their cost effectiveness and radiation hardness n-in-p silicon devices are a promising candidate to replace the present n-in-n sensors in the radiation environment of HL-LHC and to instrument the large area of the new ATLAS pixel system. Furthermore thin pixel sensors offer a reduced contribution to the material budget and a higher charge collection efficiency (CCE) at the radiation levels expected in the inner pixel layers at HL-LHC.
The 75 um thick FE-I3 compatible sensors have been connected with SLID to read-out chips and were irradiated up to fluence of 5e15 n_eq/cm^2. A CCE close to 100% has been measured at bias voltages as low as 500 V and the SLID interconnection efficiency proved not to be affected by these radiation levels.
The 150 um thick sensors were interconnected by bump-bonding to the new ATLAS pixel read-out chip FE-I4. An excellent performance in terms of charge collection efficiency and noise occupancy were obtained before and after irradiation at 5e15 n_eq/cm^2.
The results, obtained with laboratory and beam tests, for these two thin pixel productions will be compared with those of n-in-p pixels of standard thickness.
On the thin FE-I3 modules ICVs, with a cross section of 3 um x10 um, are going to be etched at the positions of the original wire bonding pads of the FE-I3 chip. This step is meant to prove the feasibility of the signal transport to the newly created readout pads on the backside of the chips, allowing for four side buttable devices without the presently used cantilever for wire bonding. The status of the ICVs preparation on the FE-I3 wafer will be presented.

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