Scribe-Cleave-Passivate (SCP) Slim Edge Technology for Silicon Sensors

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Introduction

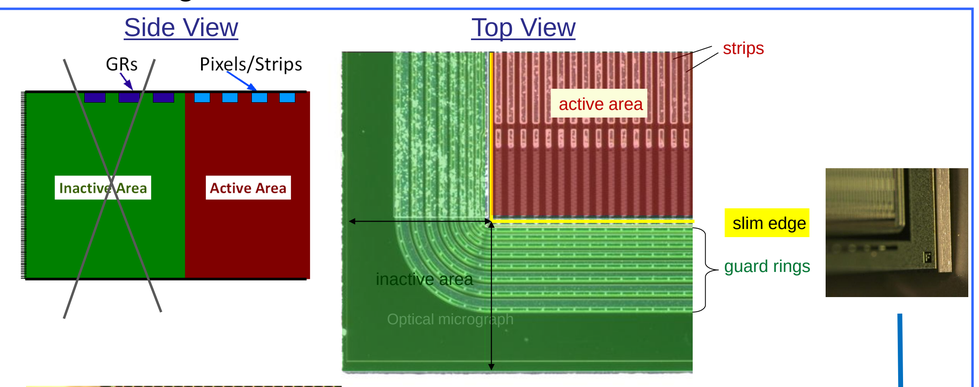
Modern large experiments, such as ATLAS and CMS, require large-area tracking systems with nearly hermetic coverage. The essential building blocks of such system are silicon sensors, which typically contain inactive regions at their periphery. This requires either tiling the sensors to achieve hermeticity , or introduction of additional layers to compensate for the acceptance gaps. There are similar requirements in other fields (e.g. medical imaging) .

We seek to dramatically increase the active area fraction of the sensors by minimizing the inactive area at the periphery of the sensors, from 500-1000 um typical distance to 100 um or less. This is sometimes called “slim edge” approach. The work was started in the context of ATLAS Planar Pixel Proposal [1]. Based on the initial results, a proposal to RD50 collaboration [2] was also approved in June 2011.

The technology we are developing can be used with any modern sensor. It is particularly useful for pixel systems that require large instrumented area composed of moderate size sensors, due to $\delta a / a$ area factor.

[1] M. Biemforde, “The ATLAS Planar Pixel Sensor R&D Project”, NIM A 636 (2011) S8
[2] http://rd50.web.cern.ch/rd50/

Goal:



Slim edge examples:

3D FE-I4 device with slim edge

Strip device with 4 slim edges

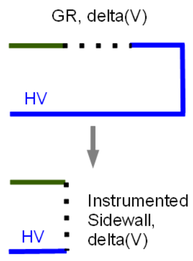
Method

Basic Idea

Conventional planar sensors have two relevant features that prevent establishing a slim edge:

- They are singulated by a saw which leaves large defect density on the sensor sidewall, making it conductive.
- There is a need for potential drop along either top or bottom surface of the sensor near the edge, which requires a finite inactive edge distance [1].

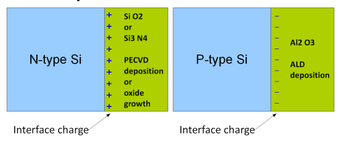
We seek to avoid these issues by making an instrumented sidewall which can tolerate the potential drop. The key aspects of the method are cleaving techniques that exploits silicon lattice orientation and proper sidewall passivation.



[1] N. Unno, presentation at 6th PPS meeting, DESY, April 2010.

Key Steps

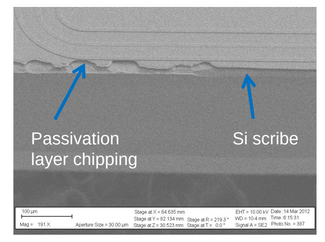
- Scribing along the lattice orientation of the Si wafer
  - Diamond
  - Laser
  - Etch-scribing with XeF2
  - DRIE scribing
- Cleaving
  - Manually with tweezers
  - With Industrial cleaving machines, e.g. by Dynatex or Loomis
- (optional) sidewall etch
- Passivation
  - N-type bulk requires positive interface charge with Si:
    - Native oxide formation with thermocycling, UV light
    - PECVD deposition of SiO2
    - PECVD deposition of Si3N4
    - ALD deposition of “nanostack” of SiO2 and Al2O3
  - P-type bulk requires negative interface charge with Si:
    - ALD deposition of Al2O3



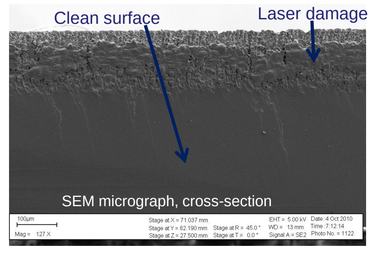
Scribing

There are many scribing options, with varying performance and reliability.

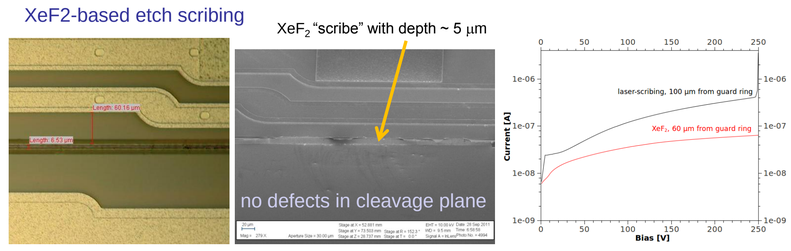
Diamond scribing



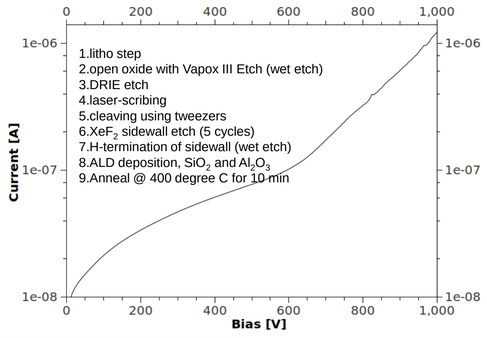
Laser scribing

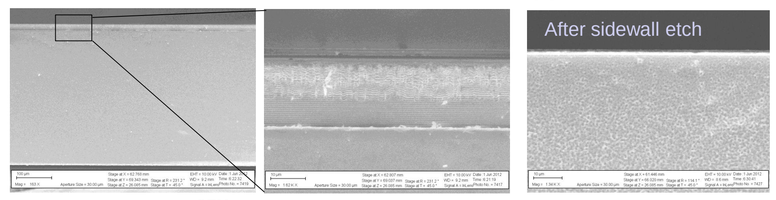


XeF2-based etch scribing



DRIE based etch scribing

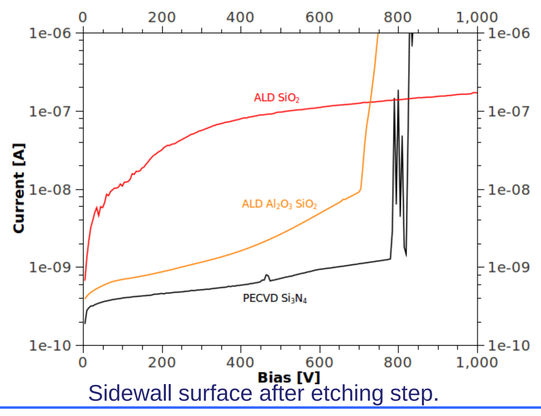




SEM micrographs, cross-sections

Passivation

For n-type devices PECVD-based passivations work well. But there is a problem with processing large devices in industrial machines due to lack of vertical clearance. We found that ALD-based deposition of “nanostack” works almost as well. Almost any device size can be processed.

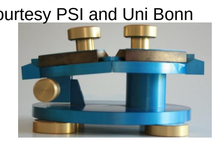


Sidewall surface after etching step.

Cleaving

We started with manual cleaving. But industrial machines are available, and found to work in many cases.

Wafer Brech Maschine
Courtesy PSI and Uni Bonn



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Patented Scribe and Break Dicing Technology
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Scriber-dicing machine

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Applications and Results

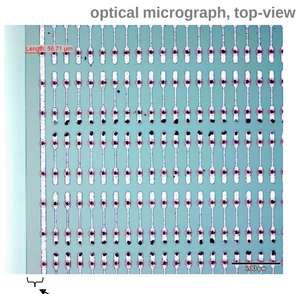
RD50 Project

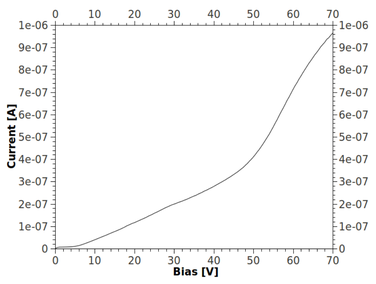
- The initial results were presented to RD50 collaboration. Based on the interest of participating institutions, this study became an RD50 project in June of 2011. There is a wide interest in this technology, reflecting its general nature. We have got multiple requests for post-processing existing devices, including planar devices with both n- and p- bulk type, as well as 3D sensors. The table below shows the current active projects and their status.
- Note that separate presentations feature some of these studies:
  - n-on-n pixel sensor studies is presented by T. Witting
  - n-on-p pixel sensor studies is shown by P. Weigell
  - 3D pixel sensors on modules is shown by G. Pellegrini

Institute	Contact Person	Sensors	Status
CNM Barcelona	G. Pellegrini	3D diodes, strips, pixels	2nd round of tests (FEI3 and FEI4 pixel)
FBK Trento	G.-F. Dalla Betta	3D diodes, strips	2nd round of tests ongoing
MPI Muenchen	A. Macchiolo	P-type planar pixels	In progress
UNFN Bari	D. Creanza	N-type “SMART” detectors	First processed devices sent for evaluation
Ljubljana U.	G. Kramberger	P- and N- type	Sent processed devices for laser TCT
Glasgow U.	R. Bates	P- and N- type	Sent processed devices for beam test
TU Dortmund	T. Wittig	IBL-style n-on-n sensors	Initial tests done, iterations with IBL sensors

CNM 3D pixel sensor:

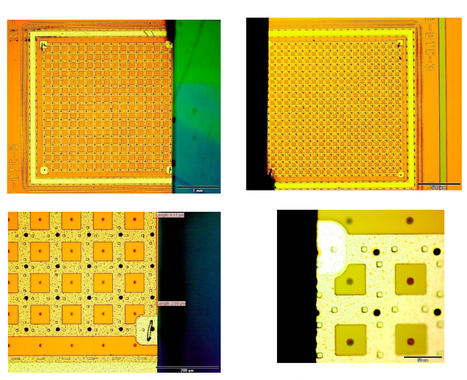
optical micrograph, top-view

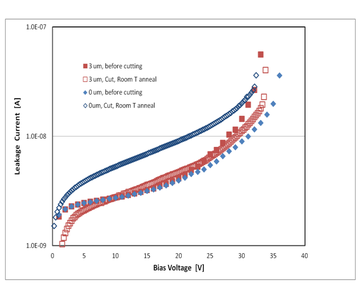




SCP edge distance to guard is ~ 58 μm.

FBK Trento 3D pixel diodes



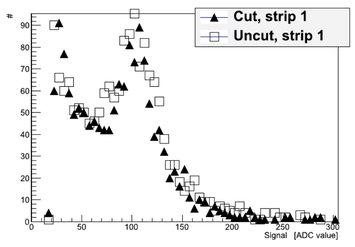


3 um distance

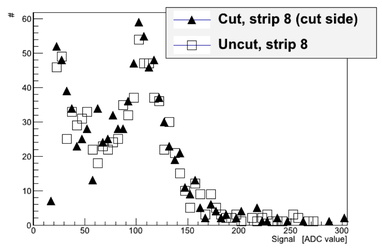
0 um distance

Charge Collection near the edge

- We have studies charge collection with strip sensors near the slim edge with binary readout system.
- A study by R. Mori et al (“Charge collection measurements on slim-edge microstrip detectors “, 2012 *JINST* **7** P05002) looked into more details of the signals collected by n-type strip sensors with Alibava system. No charge deficiency was found, within 5% of the total amplitude:



Edge strips at the normal (wide) edge



Edge strips at the slim (cut) edge

- There is an on-going study at CNM that looks into the effect on p-type 3D pixel detectors. See talk by G. Pellegrini for more details. ATLAS AFP detector could be possible application for such sensors.

Radiation Damage

We have irradiated both n- and p-type diodes at CERN SPS at the beginning of the summer. We will study the sensors as soon as we get them after cool down period.

Conclusions

- SCP method of making silicon devices with slim edges holds a lot of promise
- Work goes on in the framework of ATLAS PPS and RD50 Collaboration.
- The method development continues:
  - Basic technology development with a focus on industrialization:
    - new scribing options
    - new passivation for n-type devices (nanostack of SiO2 and Al2O3 suitable for wafer-scale processing)
  - Physics performance: Radiation tolerance, Charge collection
- We are thrilled to perform dedicated studies and service for the community!

Acknowledgments

- This work has been performed within the framework of CERN RD50 Collaboration and ATLAS Planar Pixel Proposal.
- We would like to thank the Institute for Nanoscience (NSI) at the U.S. Naval Research Laboratory (NRL) and the NSI staff. The work done at NRL was sponsored by the Office of Naval Research (ONR).
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- We thank Loomis Industries, Inc., PhotoMachining, Inc., as well as Kavli Nanoscience Institute at Caltech for scribing and cleaving test devices.