History and prospect of low-noise CMOS sensors

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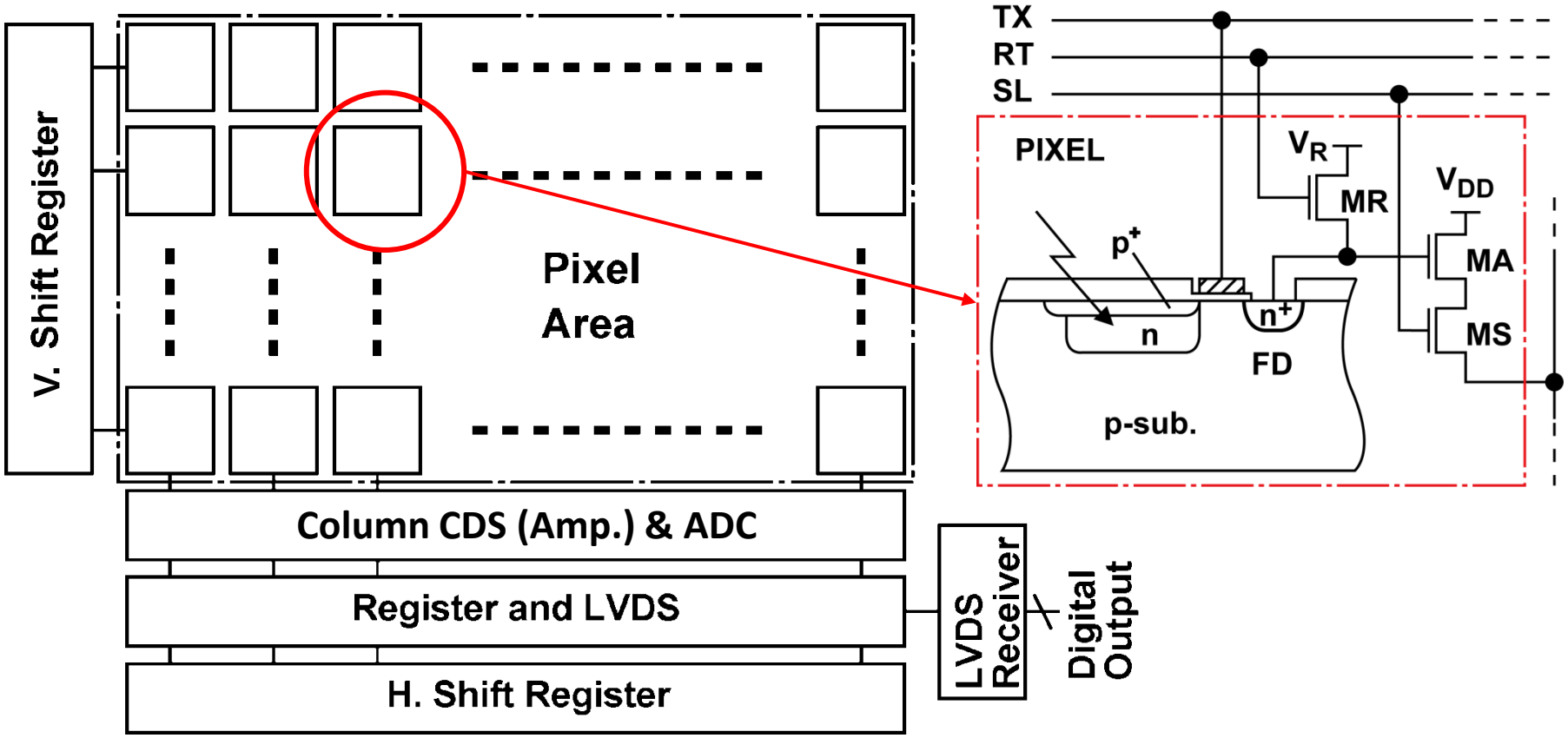
Typical CIS Architecture



- Charge-transfer-type active pixel with pinned photodiode
- Column CDS (Correlated double sampling) Amplifier (if necessary)
- High-speed A/D conversion Using 1-D parallel operation
- High-speed low-noise digital signaling like LVDS (low-voltage differential signaling)

Low Noise CMOS Image Sensors: Design Challenges

1. Low Noise (<2e-)
2. Low Noise at High Pixel Rate (= frame rate x # of pixels)
3. Low Noise and High Intrascene Dynamic Range
4. Sub-electron Noise

Low Noise CMOS Image Sensors

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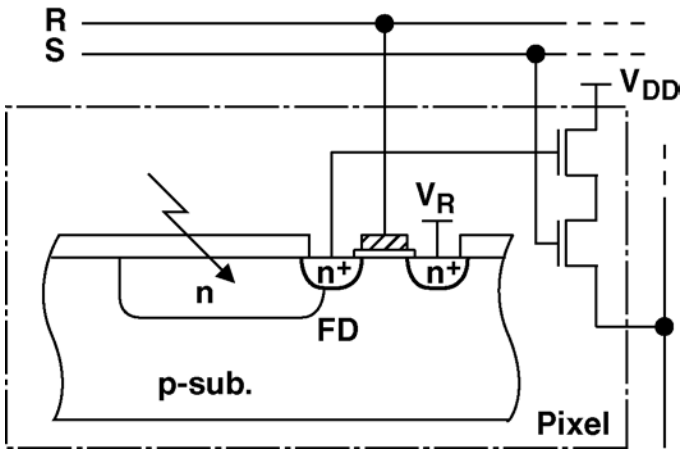
Dark Noise in CMOS Image Sensors

1. Temporal Random Noise
   - Dark Current (Shot Noise)
   - Reset or kTC Noise
   - Amplifier's noise (thermal and 1/f noise)
   - Row (Horizontal) Noise
2. Fixed-Pattern Noise
   - Pixel Source Follower's
   - Column Readout Circuit's (Vertical FPN)
   - Dark Current

Active Pixel Sensors

3Tr. APS

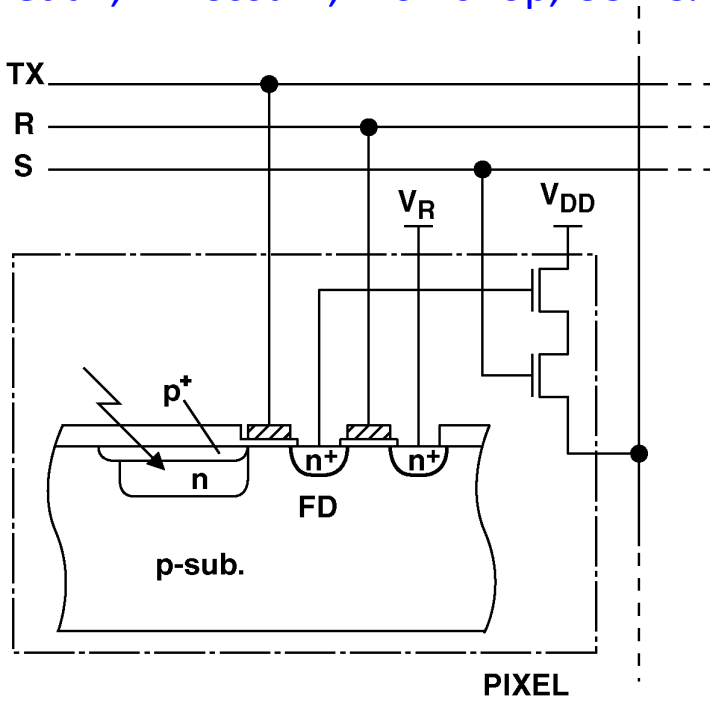
Chamberlain, IEEE-JSSC '69



- Used in end of 90's as a first cell-phone camera.
- kTC noise is NOT cancelled.
- Large dark current
- Conversion gain is determined by PD Cap.

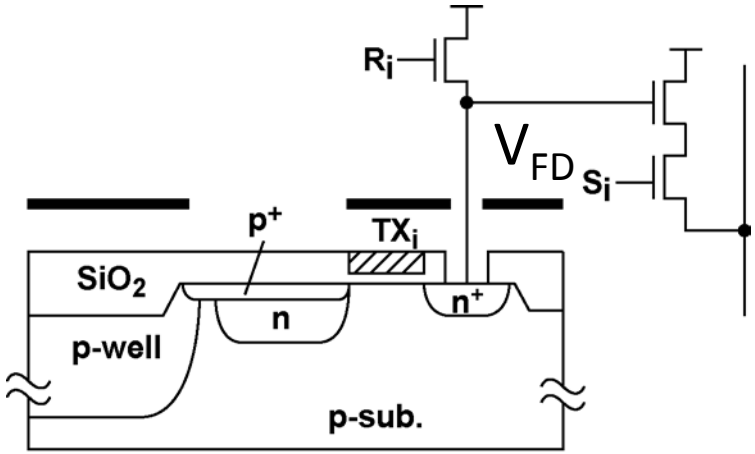
4Tr. APS (In-pixel charge transfer)

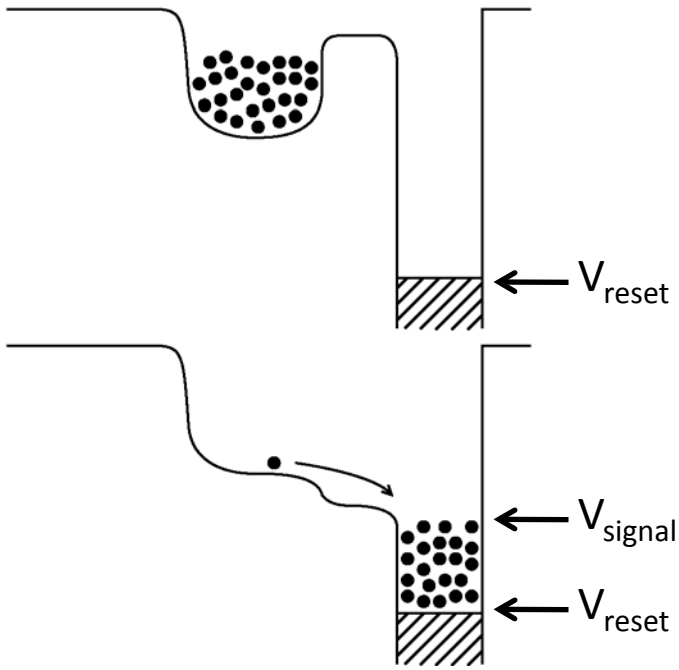
Lee et al., E. Fossum, Workshop, CCD &AIS, 1995.

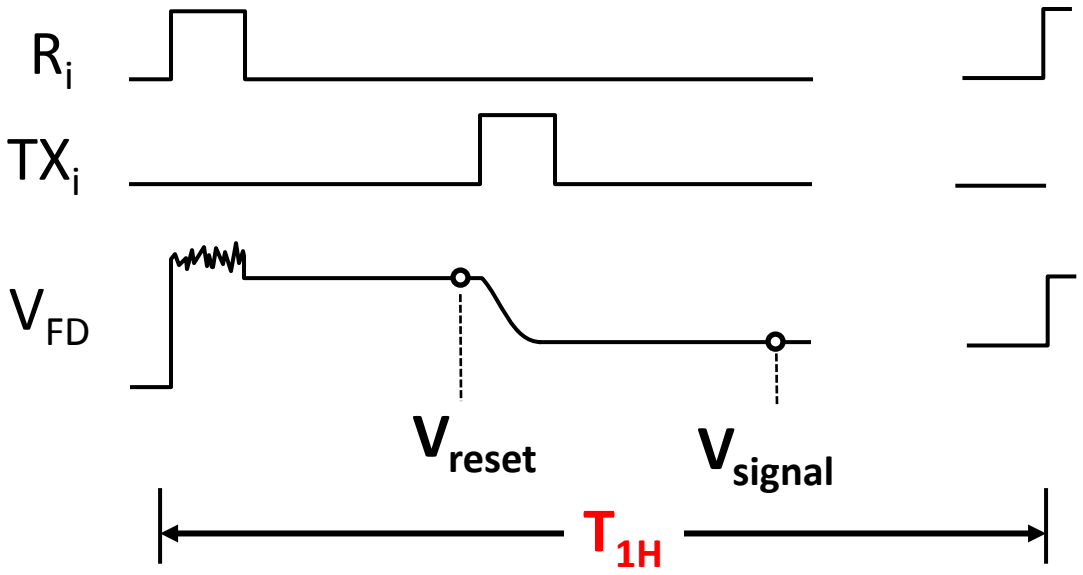


- kTC noise is cancelled.
- Low dark current due to pinned photodiode
- High conversion gain due to small floating diffusion capacitance.

Readout Operation in CIS





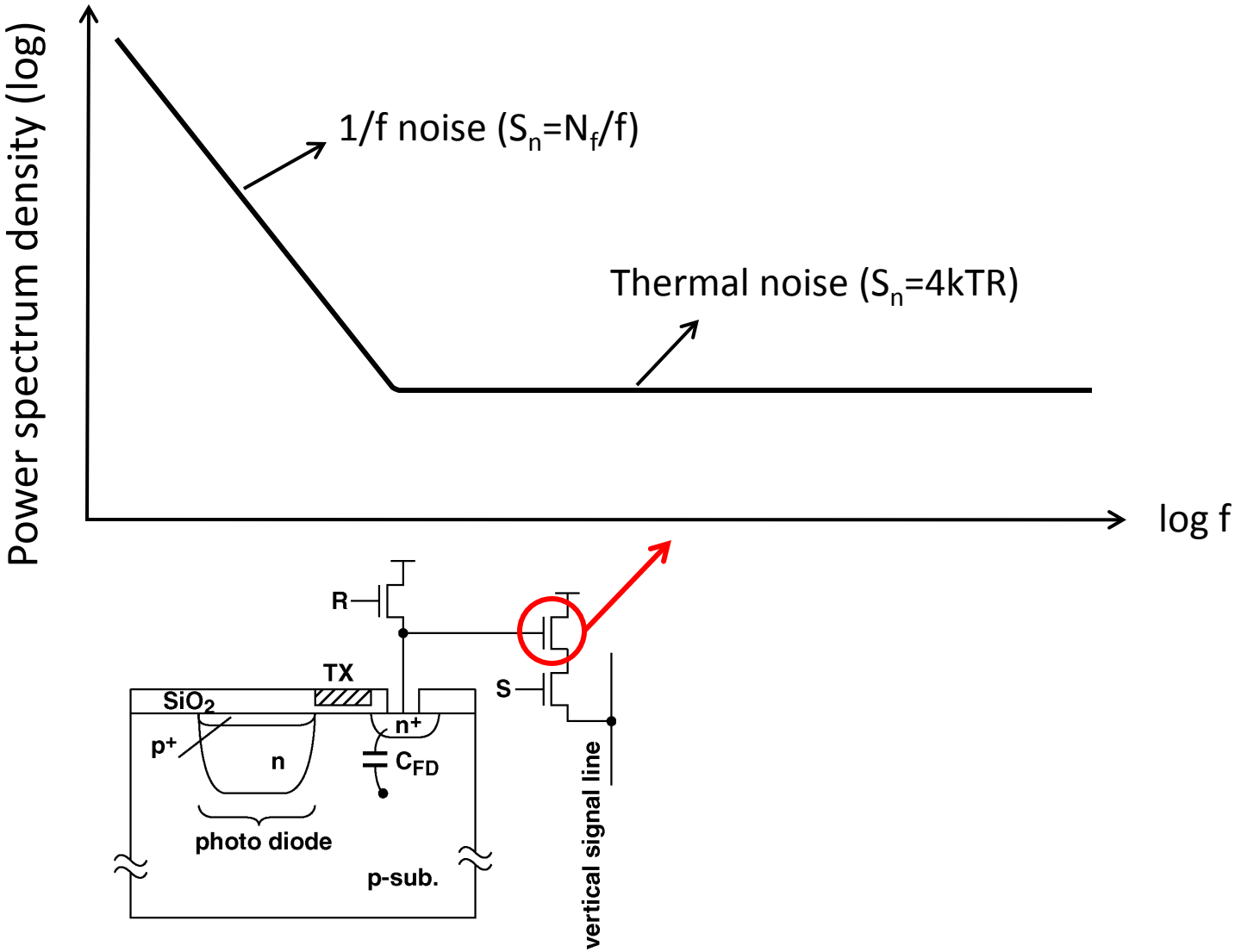


CDS (Correlated Double Sampling)

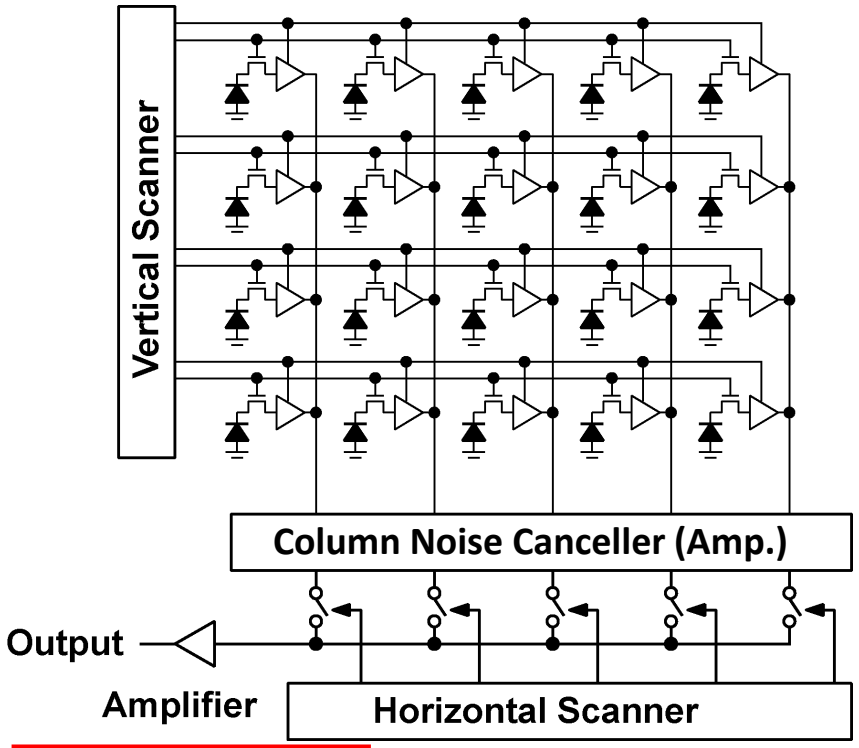
$$V_{out} = V_{signal} - V_{reset} \propto Q_s / C_{FD}$$

- Fixed Pattern Noise Cancelling
- kTC(Reset) Noise Cancelling

Thermal noise and 1/f noise in CMOS image sensors



Circuits' Noise in CMOS Image Sensors



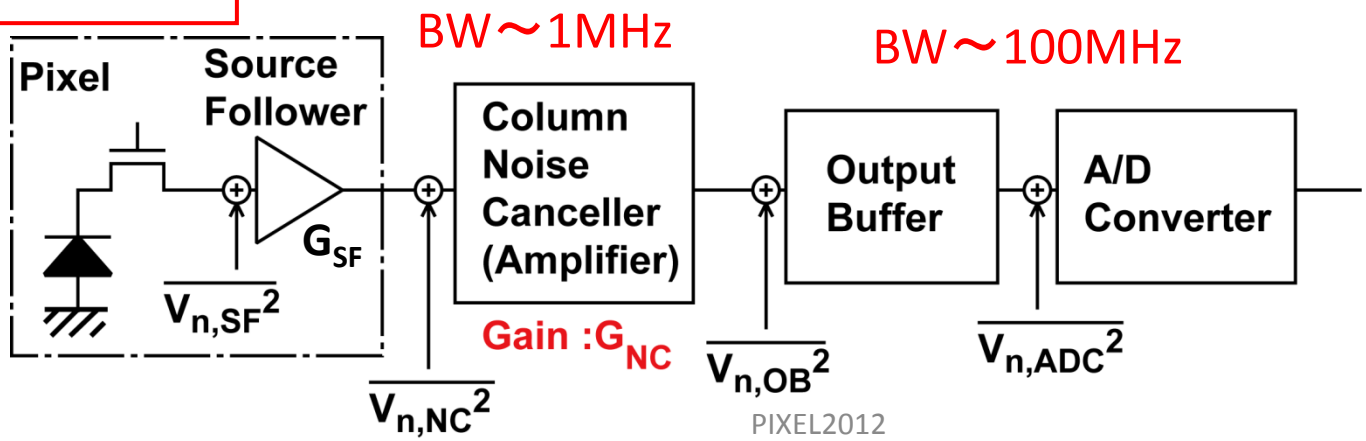
Input-Referred Noise (if G_{SF}=1)

$$\overline{V_{n,in}^{\,2}} = \overline{V_{n,SF}^{\,2}} + \overline{V_{n,NC}^{\,2}} + \frac{1}{G_{NC}^{\,2}}\left(\overline{V_{n,OB}^{\,2}} + \overline{V_{n,ADC}^{\,2}}\right)$$

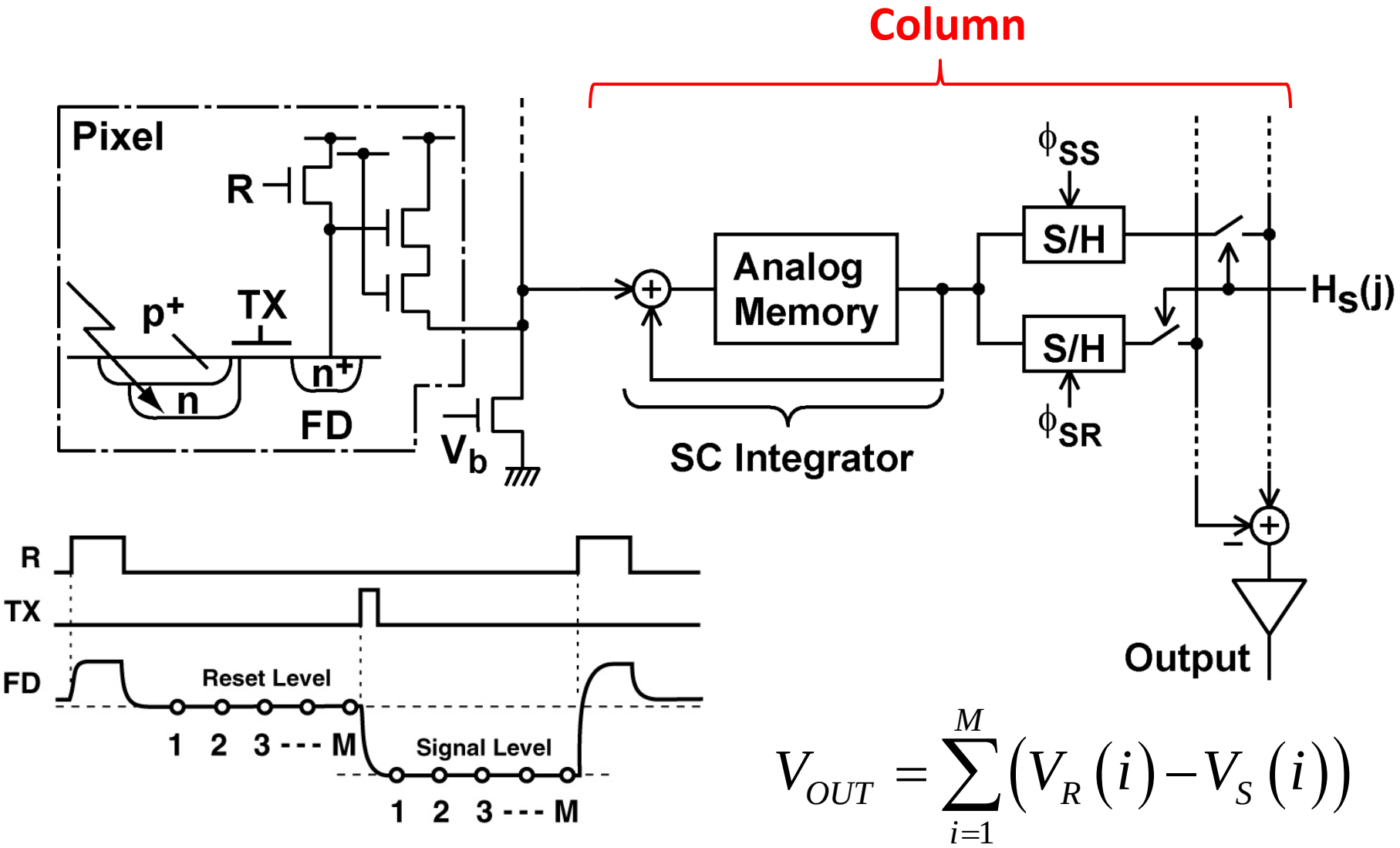
$$\cong \overline{V_{n,SF}^{\,2}} + \overline{V_{n,NC}^{\,2}} \quad (G_{NC} >> 1)$$

→Gain of column amplifier greatly reduces wideband circuit noise.

Signal Chain



Column-Parallel Correlated Multiple Sampling



$$V_{OUT} = \sum_{i=1}^{M} \left(V_R(i) - V_S(i) \right)$$

M-time Sampling has a gain of M→ Noise Reduction

Noise Reduction Effect of Correlated Multiple Sampling

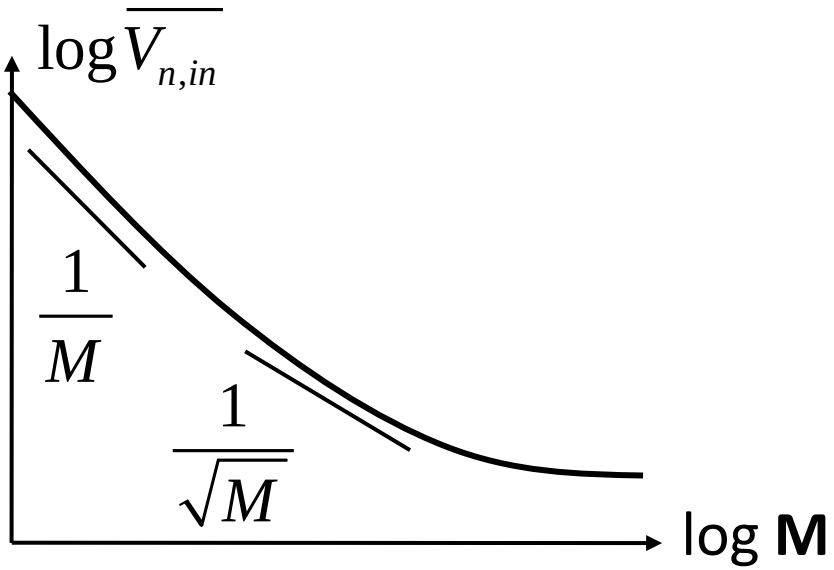
Input Referred Noise

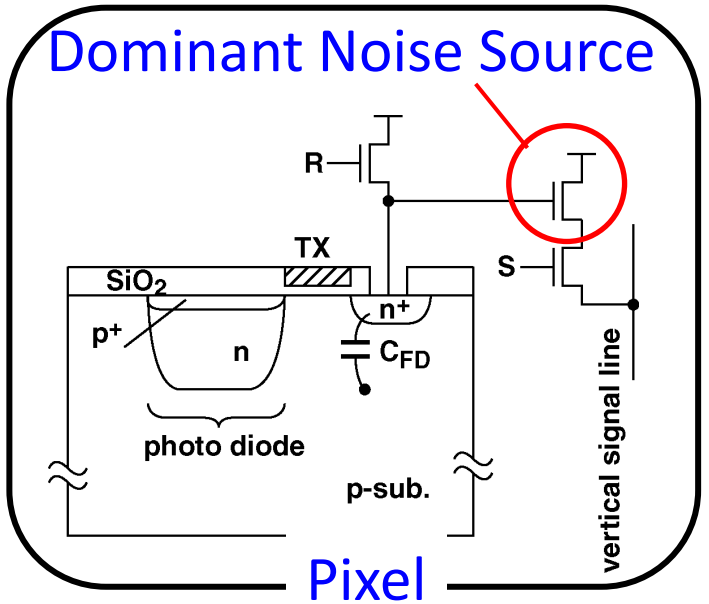
$$\overline{V_{n,in}} \cong \sqrt{\overline{V_{n,1/f}}^{2} + \frac{\overline{V_{n,th}}^{2}}{M} + \frac{\overline{V_{n,OB}}^{2}}{M^{2}}}$$

$\overline{V_{n,1/f}}^{2}$: 1/f Noise of S.F. for M=1.

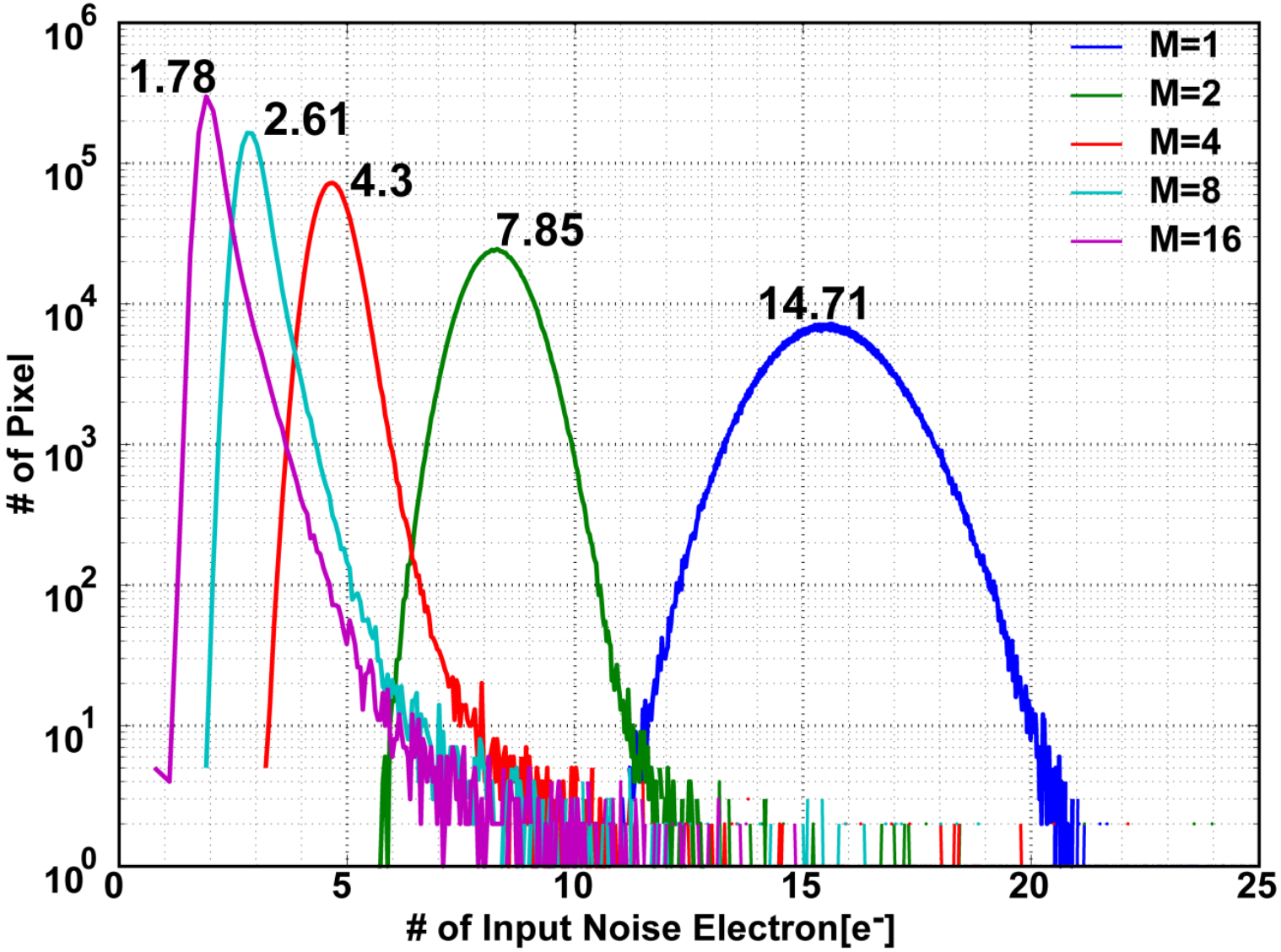
$\overline{V_{n,th}}^{2}$: Thermal Noise of S.F. for M=1.

$\overline{V_{n,OB}}^{2}$: Noise of wideband output buffer





Noise Histogram of 1Mpixel CMOS Imager



S. Kawahito et al., IISW 2009

Low Noise CMOS Image Sensors

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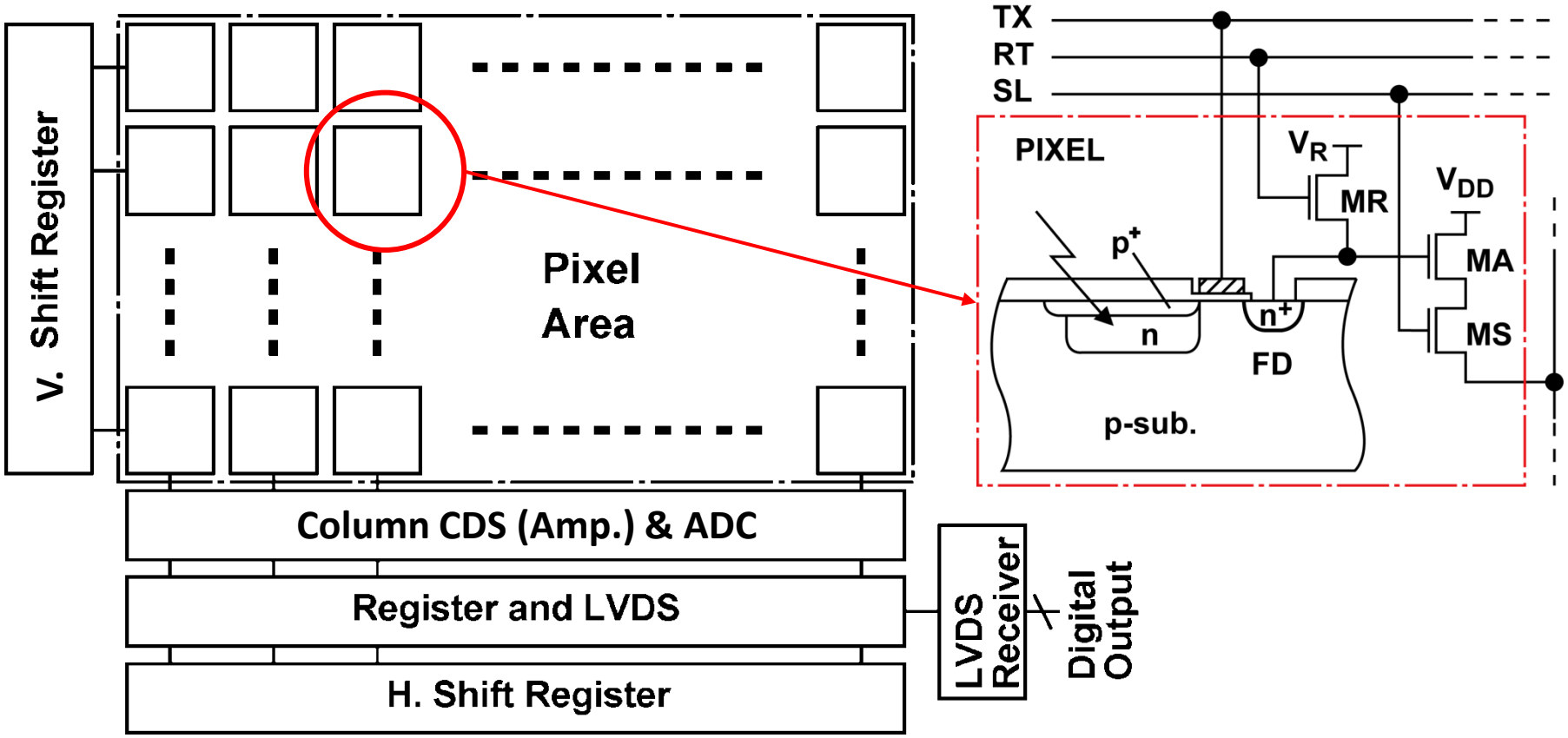
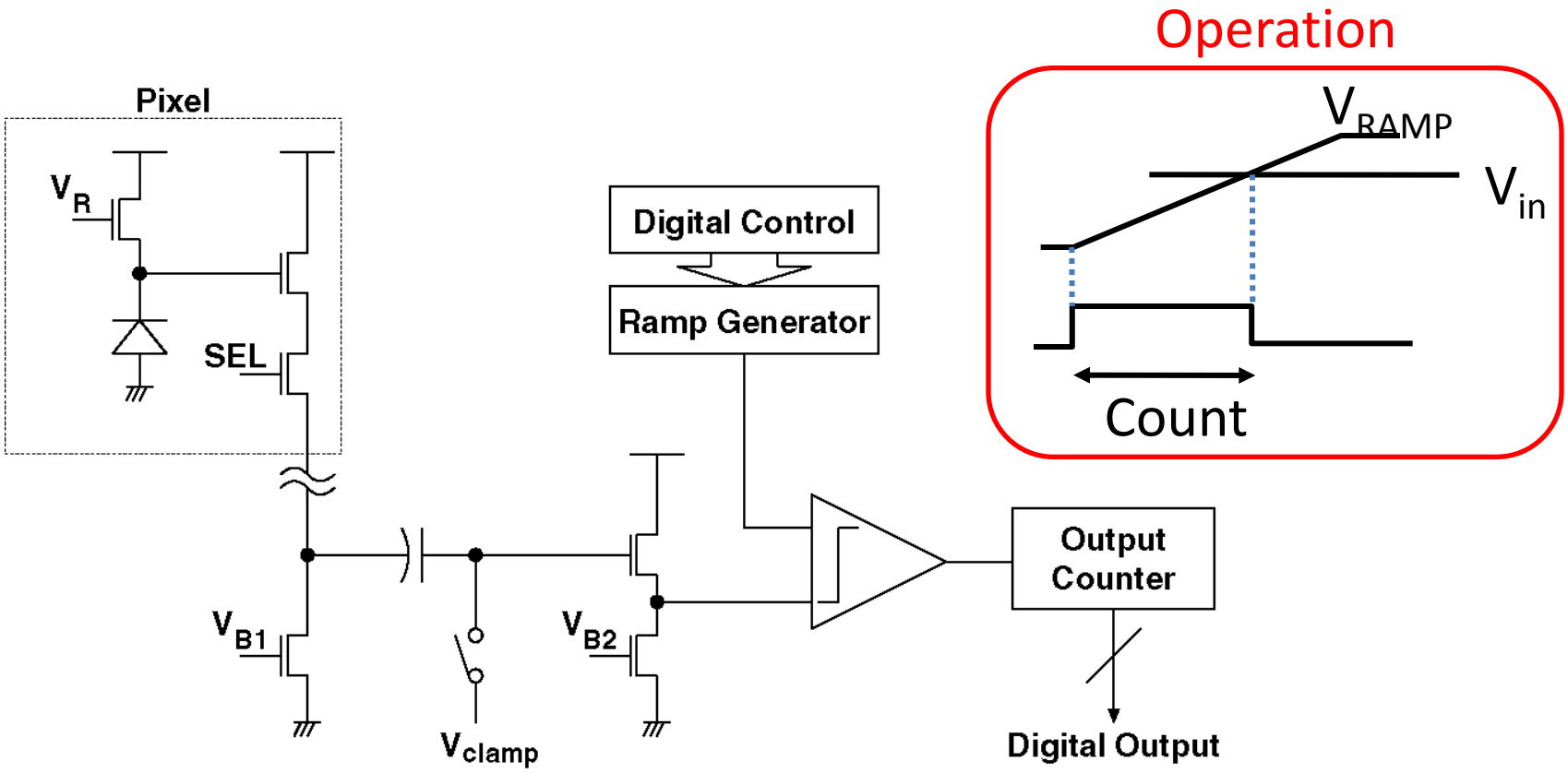
CIS Using Column ADC



- High-speed A/D conversion Using 1-D Parallel Processing
- High-speed low-noise digital signaling like LVDS (low-voltage differential signaling) is used.
-Digital H. Read is 10times faster than Analog. (Analog : several 10MHz, Digital: several 100MHz)

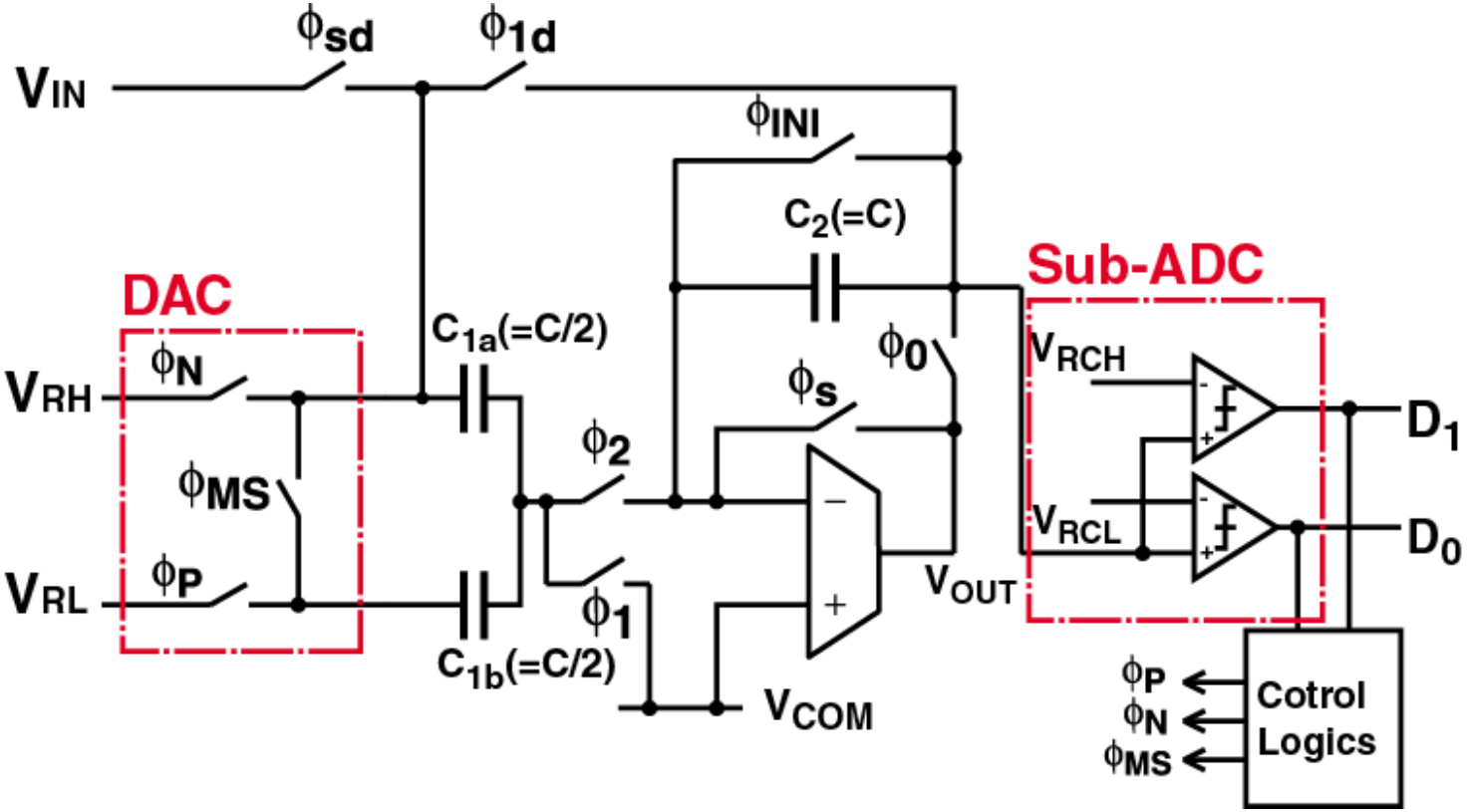
Single-Slope ADC



- Measure the time when V_{RAMP} equals to V_{in} using a counter.
- Basic Elements: Comparator and counter (or register)
- N-bit conversion requires 2^N clocks.

10b single-slope: Toshiba (ISSCC '00)

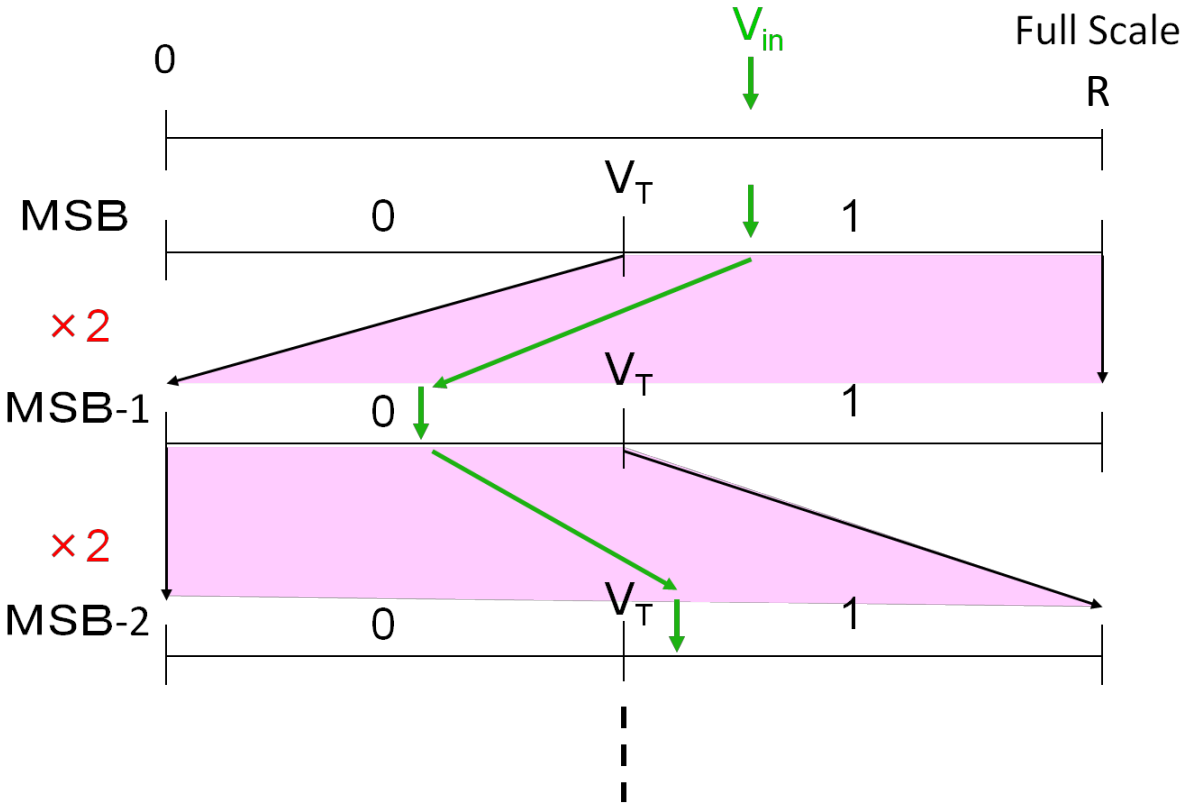
13b Column-Parallel Cyclic ADC



- Symplest Cyclic ADC (One Amp., Two Comparators, 3 Caps)
- M-1 Cycles for M bits
- Low Noise (4.9e-, gain=unity, 61uV/e-)

J. H. Park, S. Kawahito et al., ISSCC '09

Operation of Cyclic ADC

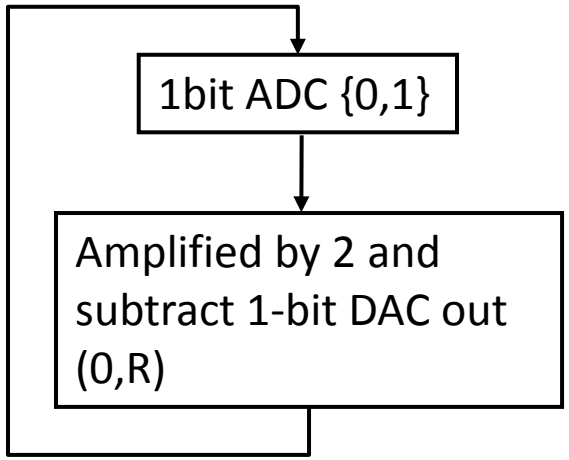


D_i

(1)

(0)

(1)



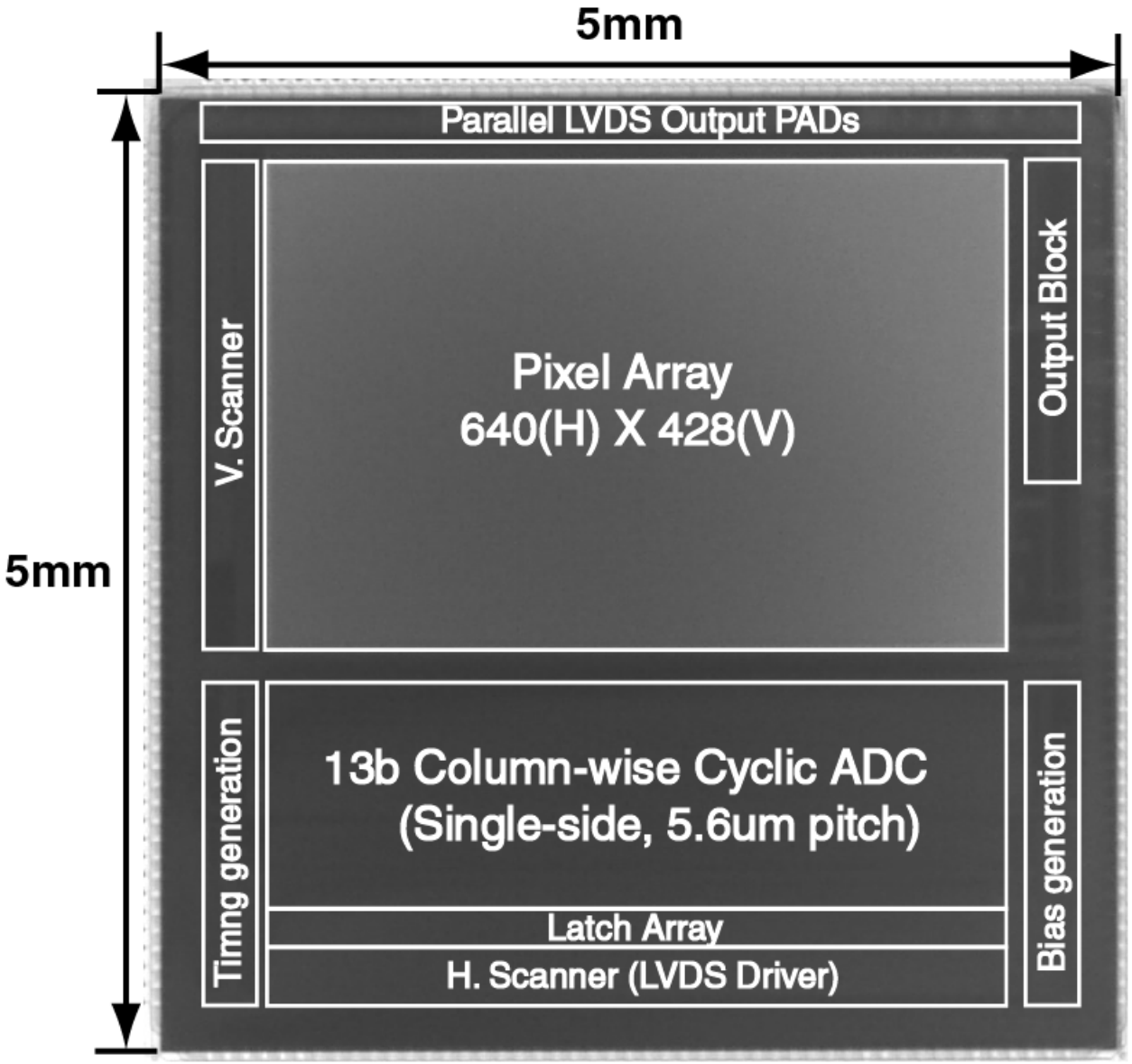
N cycles for N bits

Basic Operation:

$$X_i = 2X_{i-1} - D_{i-1} \times R$$

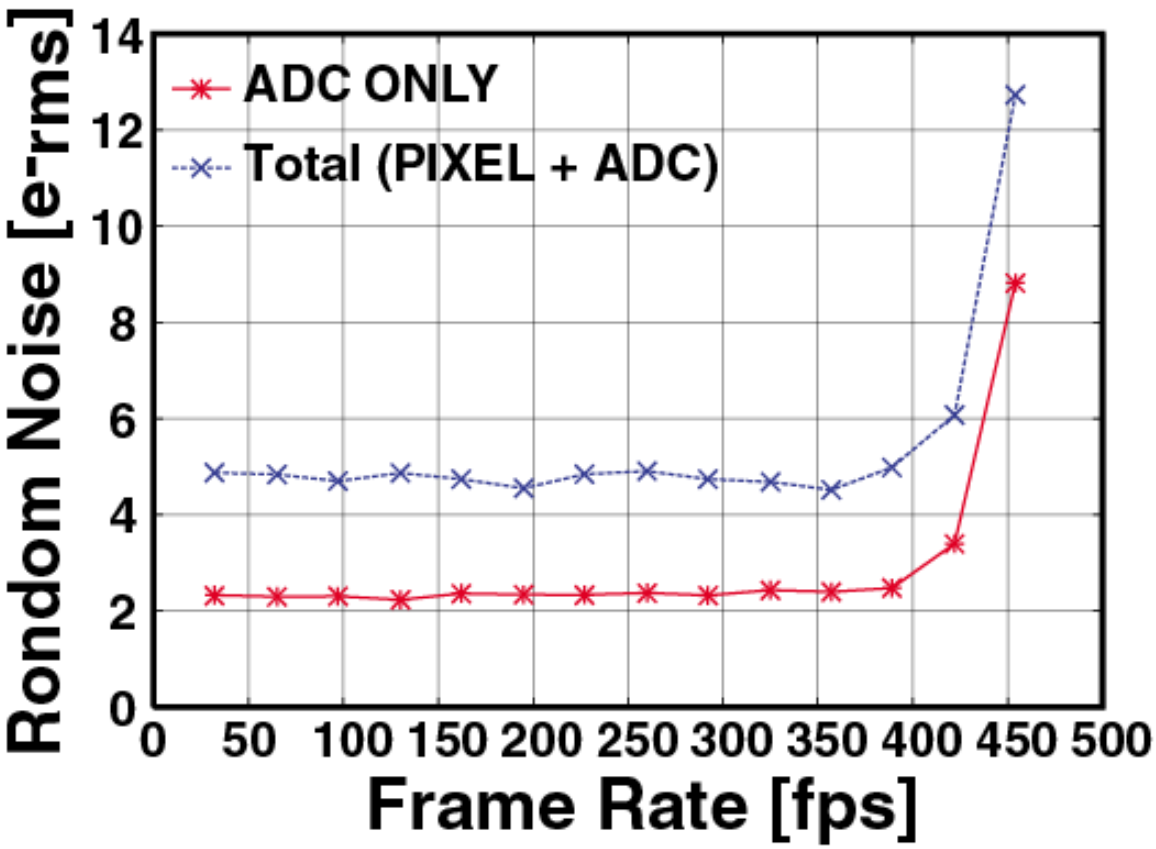
Actual Implementation : 3-state {-1,0,1} sub-ADC is used for relaxing comparator precision (N-1 cycles for N bits)

Implemented CMOS Imager



- 0.18μm CIS Process
- 4-Tr. Pinned photodiode
- Pixel Size : 5.6μm X 5.6μm
- ADC Resolution : 13b
- Frame rate : 340 fps

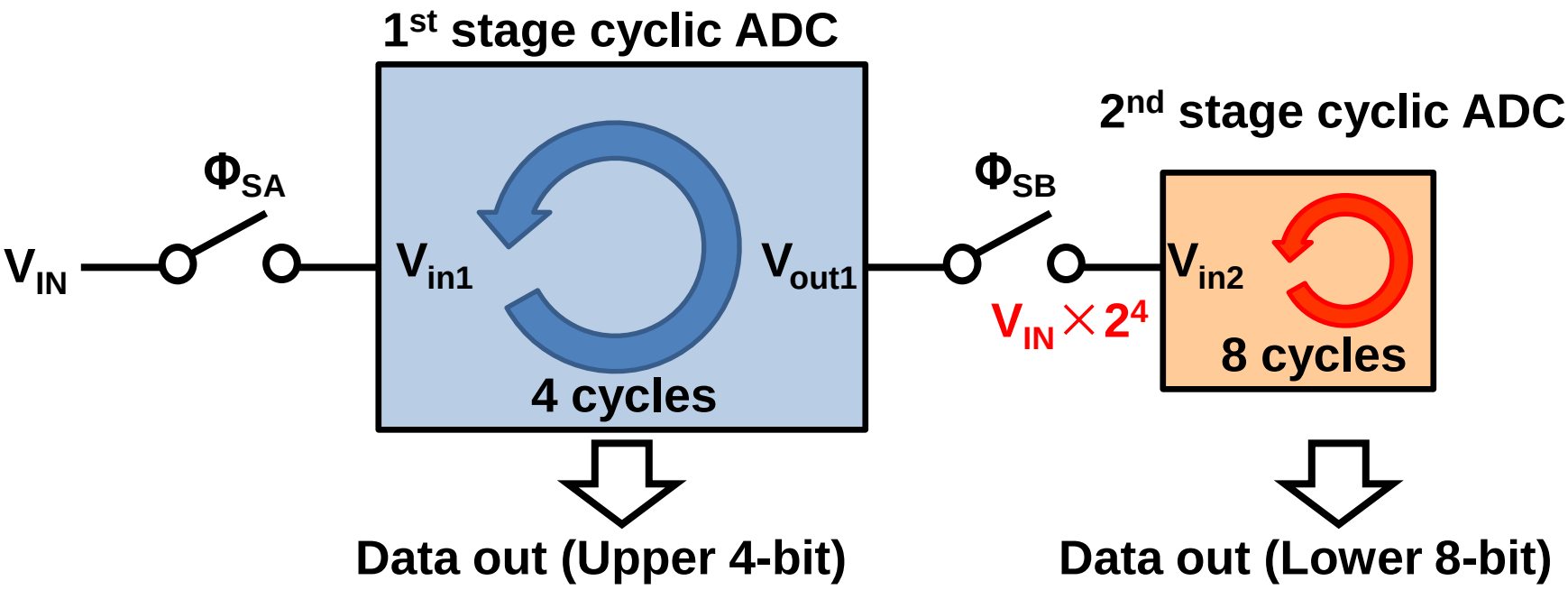
Noise Versus Frame Rage



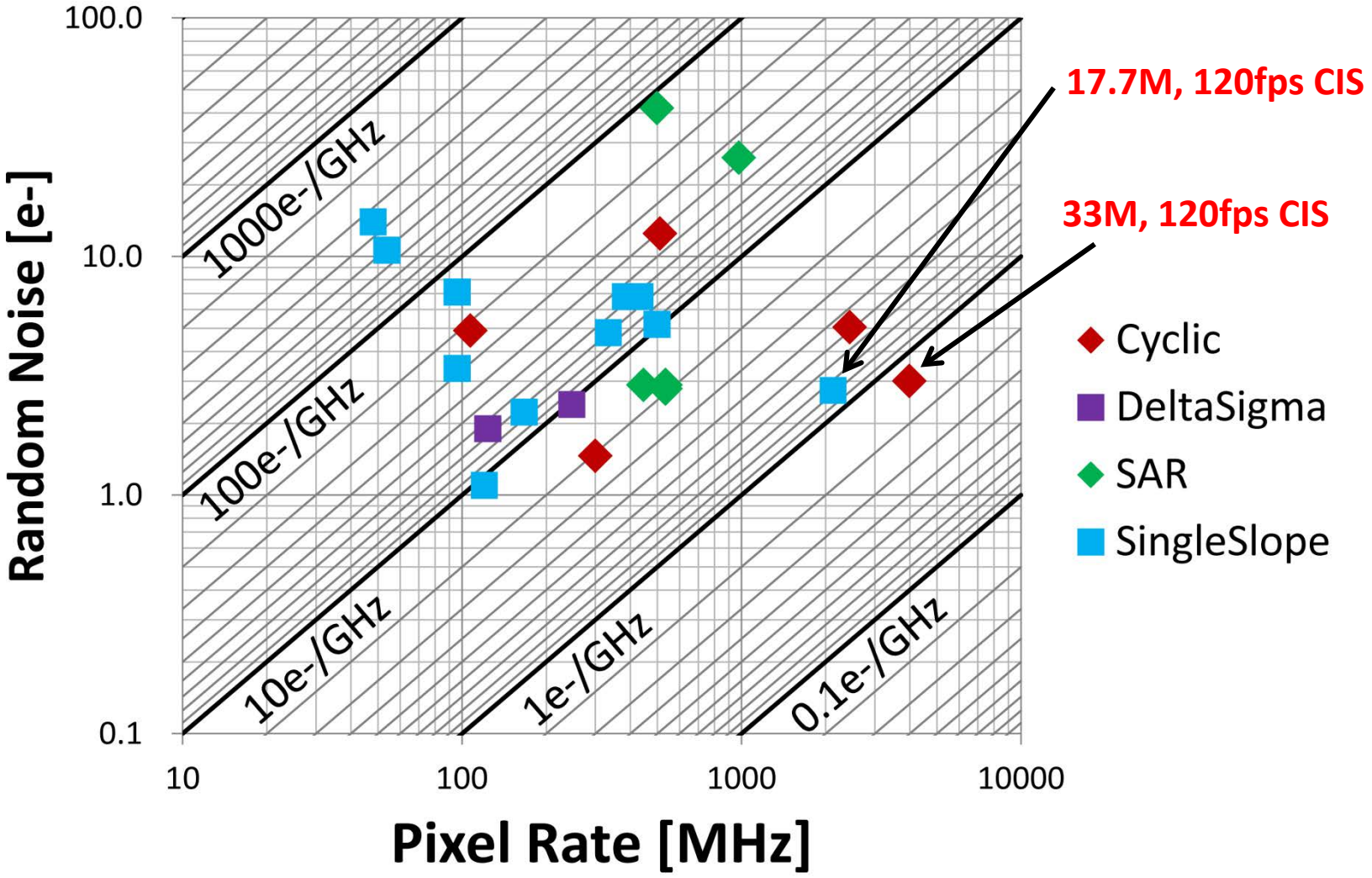
- Low ADC Noise (2.5e-): Constant up to 390fps
- Low total noise without gaing ($4.9e^-_{rms}$)

Two-stage Column-parallel Cyclic ADC

- High-speed with pipeline and parallel operation
- Low-power and small area design for 2nd stage cyclic ADC exploiting amplifier function of cyclic ADC



Noise – Pixel Rate of Digital CISs



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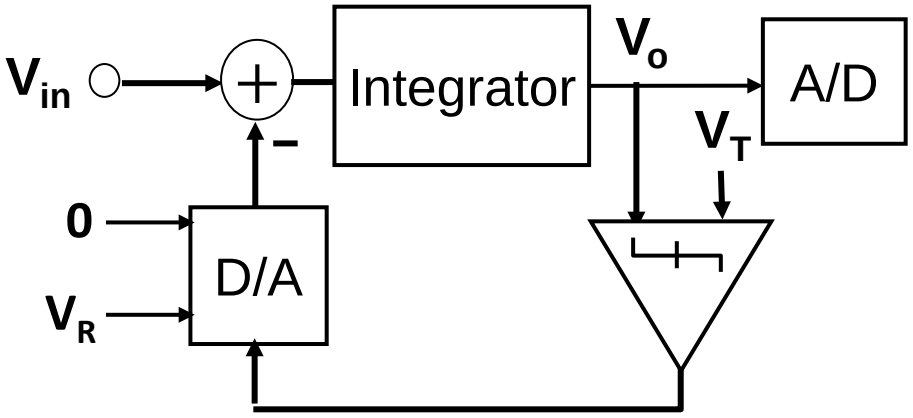
Folding Integration Algorithm (Extended Counting)



$$D_i = \begin{cases} 1 \ (\text{if} \ \ V_i \geq V_T) \\ 0 \ (\text{if} \ \ V_i < V_T) \end{cases}$$

$$V_o(i) = V_o(i-1) + V_{in}(i) - \begin{cases} V_R & (\text{if } D_{i-1} = 1) \\ 0 & (\text{if } D_{i-1} = 0) \end{cases}$$

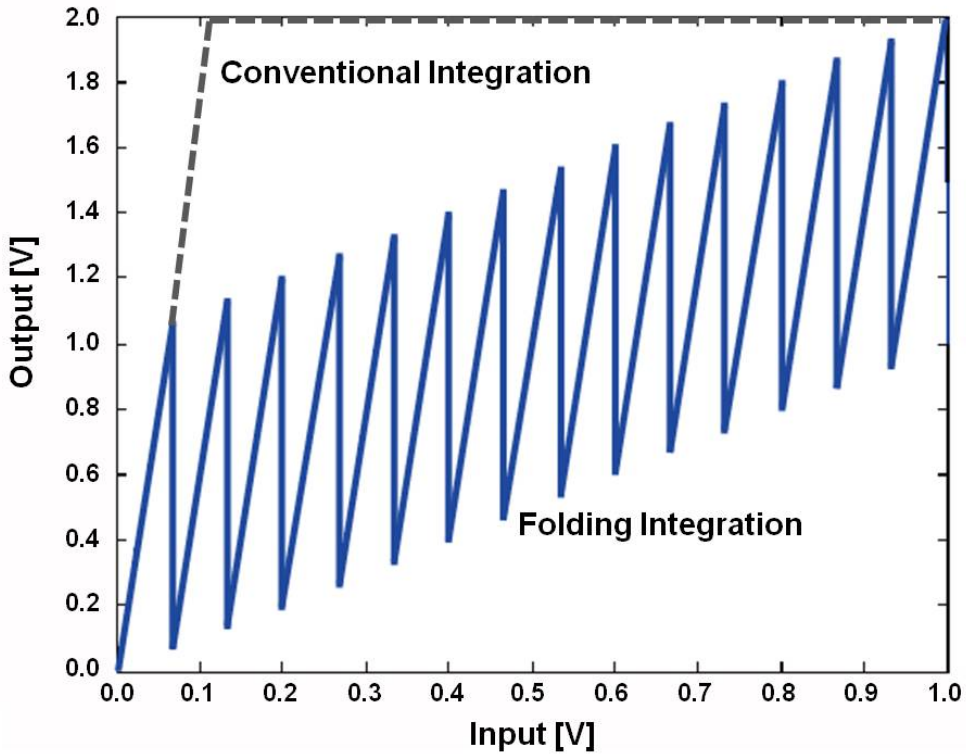
M-time Sampling : Gain of M

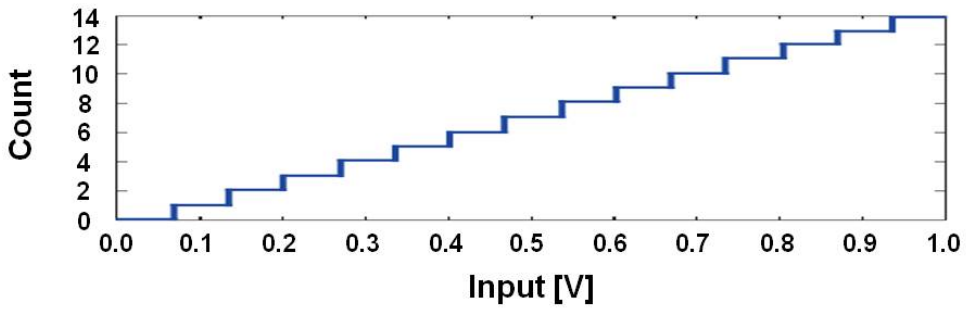
$$V_o(M) = M \times \overline{V_{in}} - N \times V_R$$

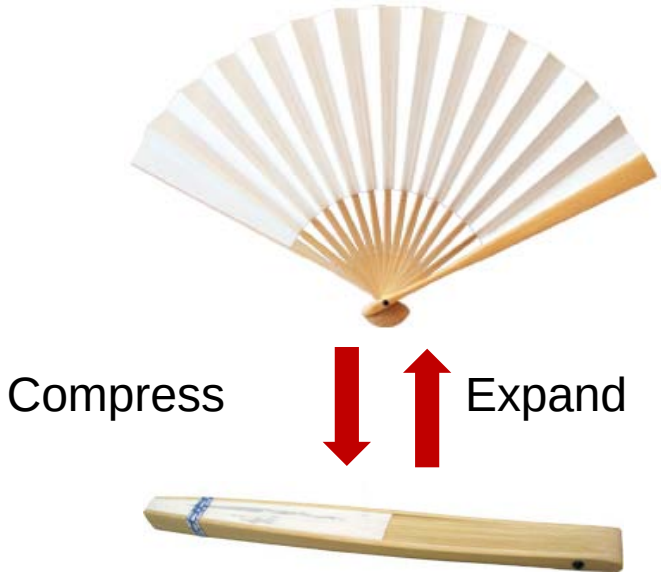
N : Number of 1's

~ Amplified by a gain of M, while compressing V_o in the same range of V_{in} (or 2 x Vin).

Transfer Curve of the Folding-Integration ADC (M=16)



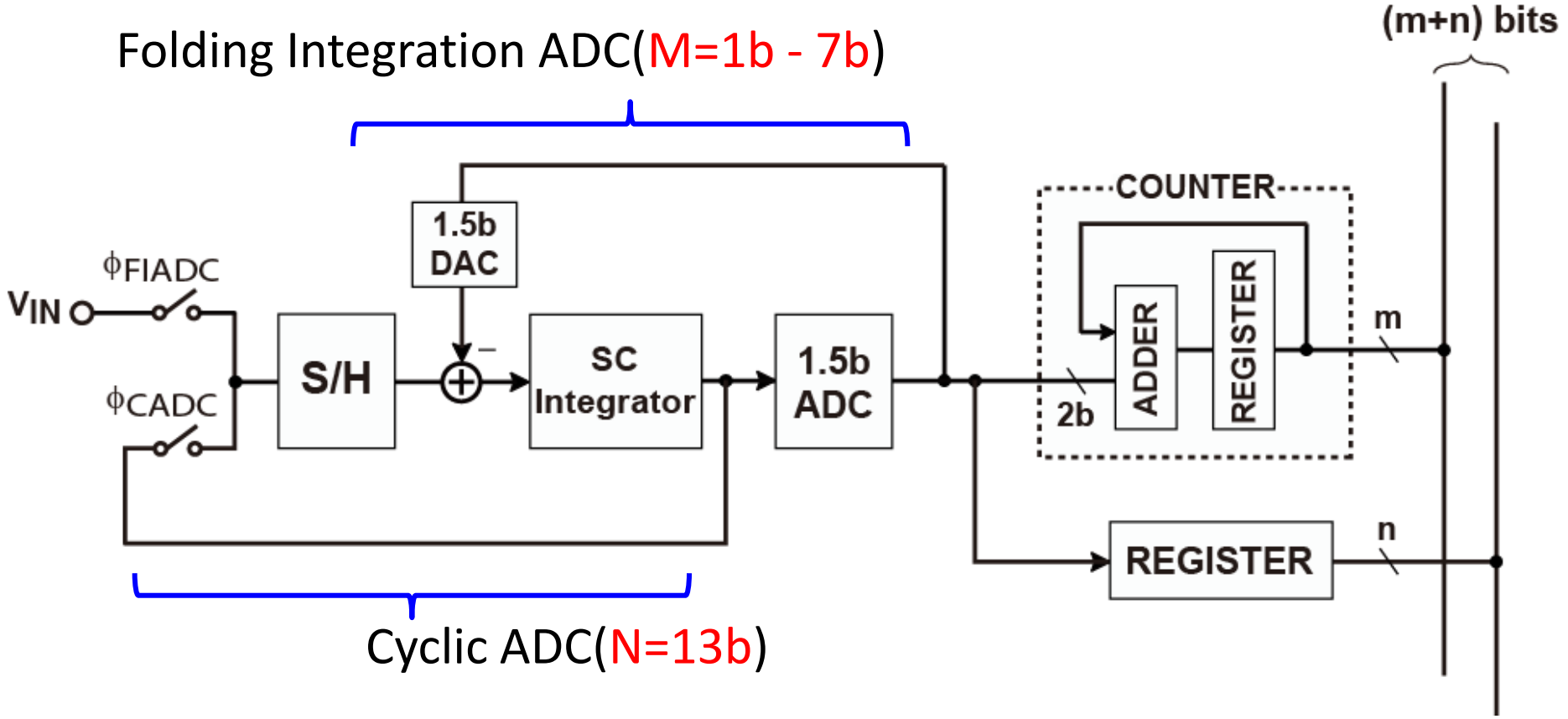




- Output signal is compressed into 1 to 2V by folding operation.
- # of counts is used for coarse ADC. Cyclic ADC is used for the analog output.
- Folding integration is also known as extended counting*.

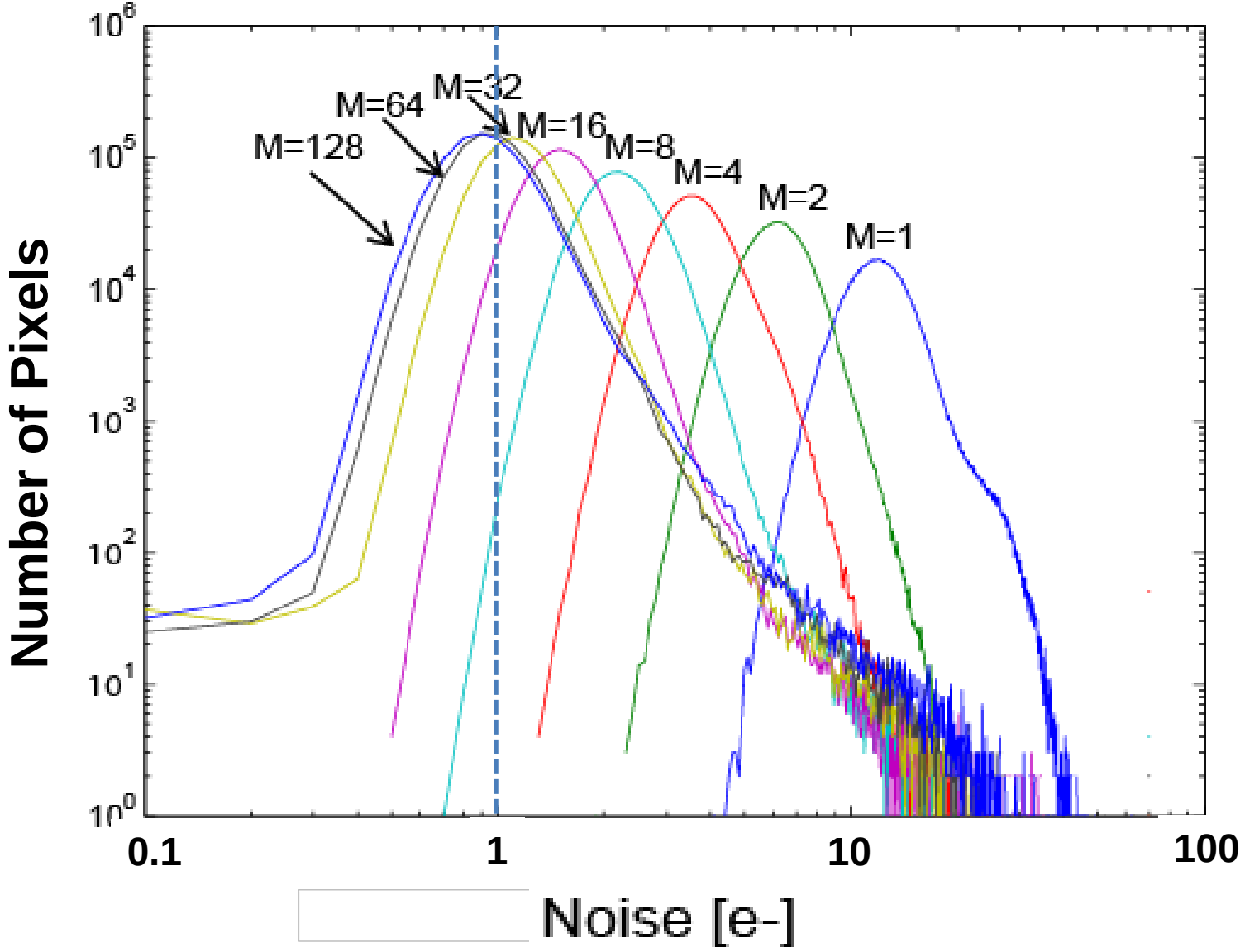
[*Jansson, IEEE Transactions on circuits and systems, 1995]

Block Diagram of the Folding Integration/Cyclic ADC

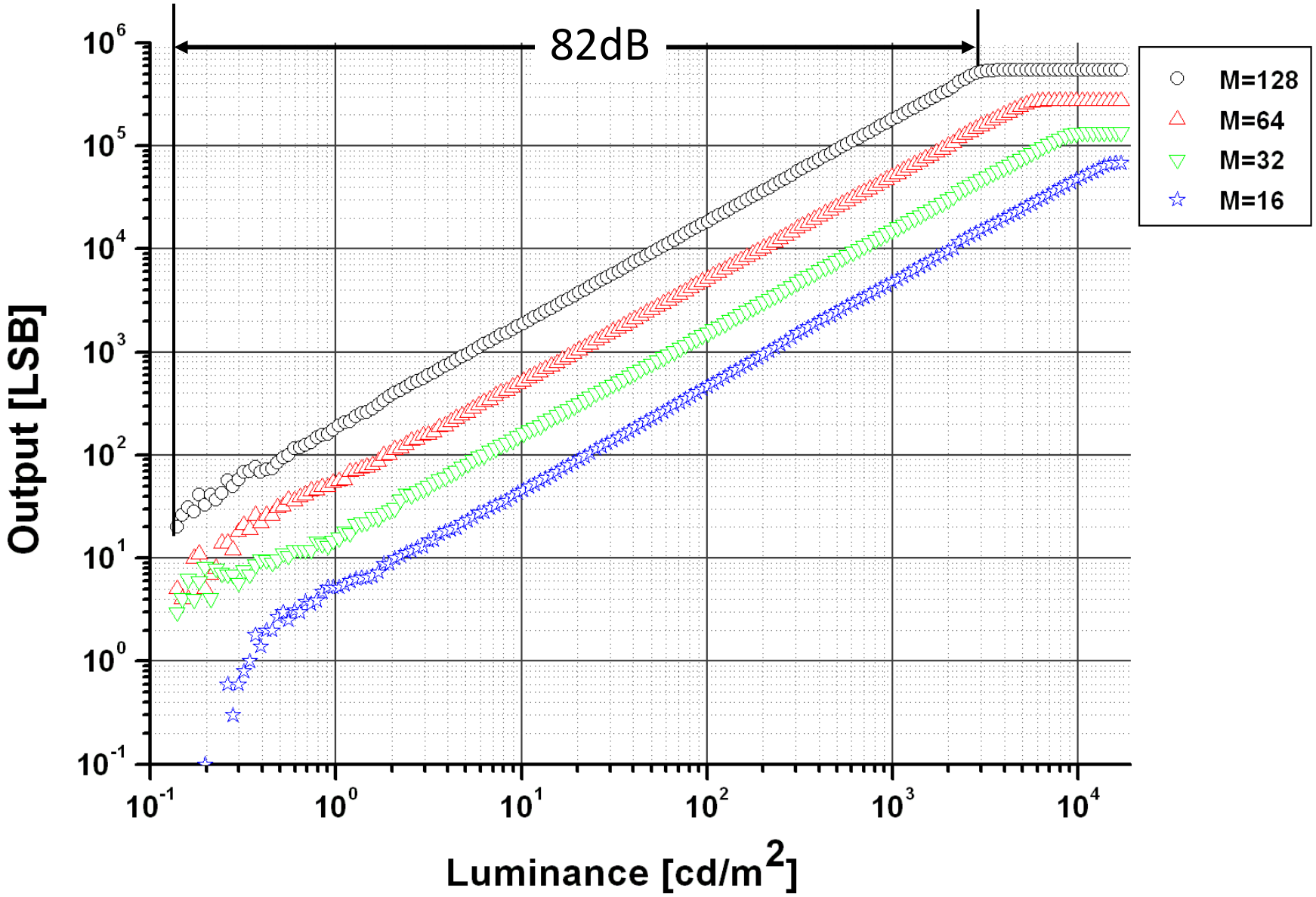


- The total resolution is M+N-1 [bits], very high gray-scale resolution (18b).
- The analog core is used for both the folding-integration and cyclic ADCs. (No additional analog circuits than that for cyclic ADC)

Noise Histogram of 1Mpixel CIS

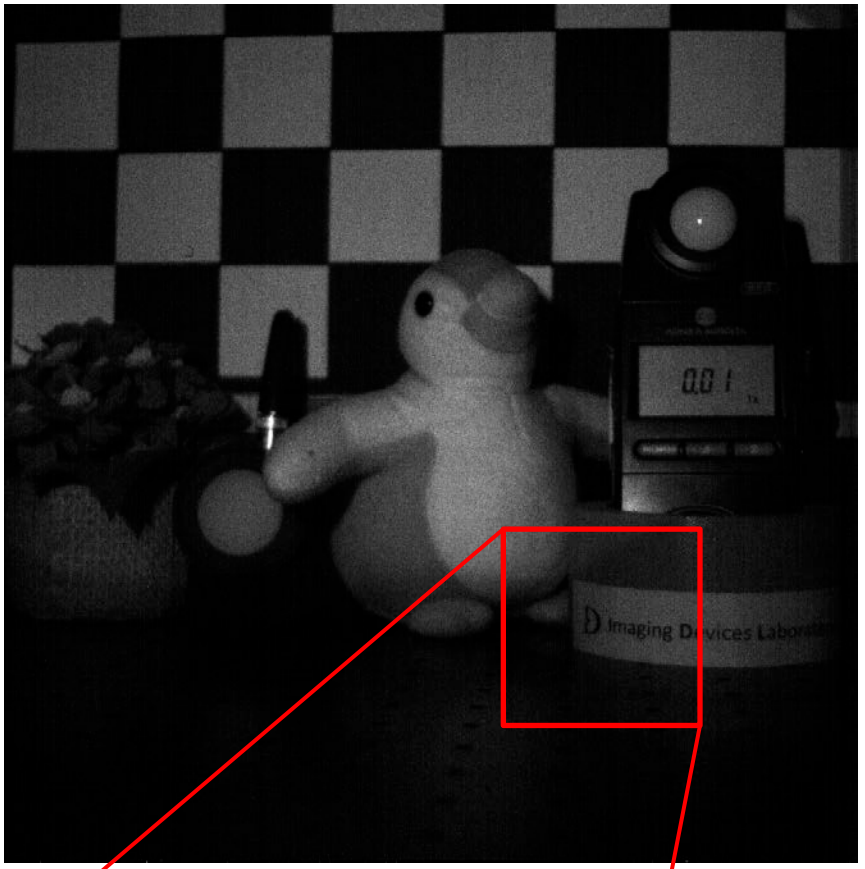


Linearity of Photo Response

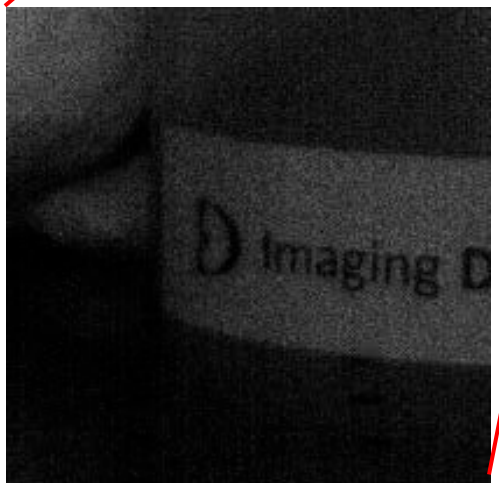


EM-CCD (Gain : x800, Cooling:-10℃, 4fps)

HS-CMOS (Gain : x768, Cooling:10℃, 4fps)

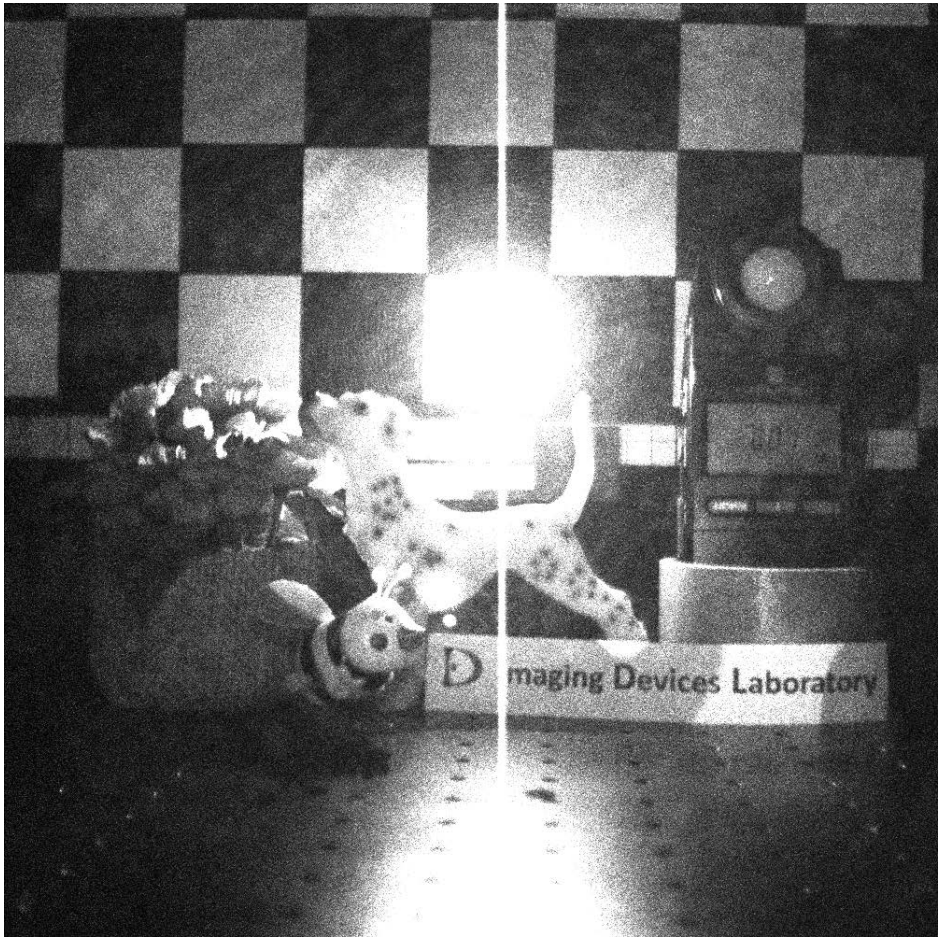


Illumination
: 0.005lx



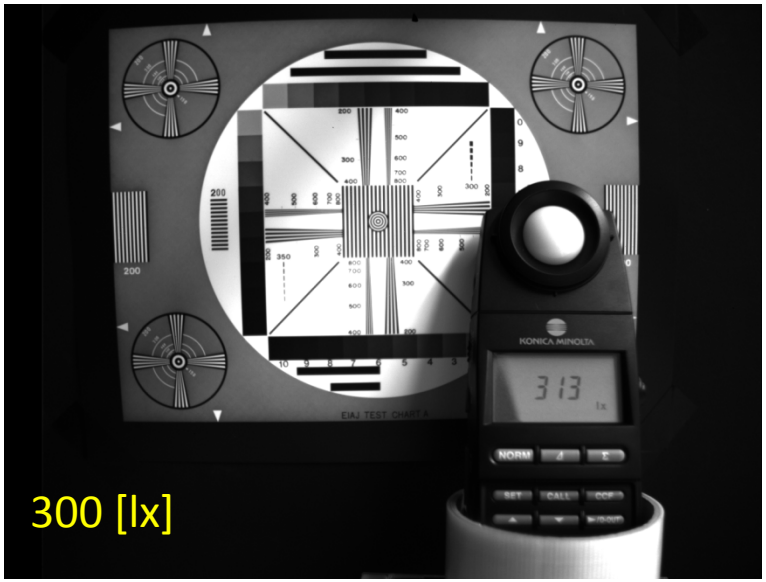
Dynamic Range Comparison

(EM-CCD)

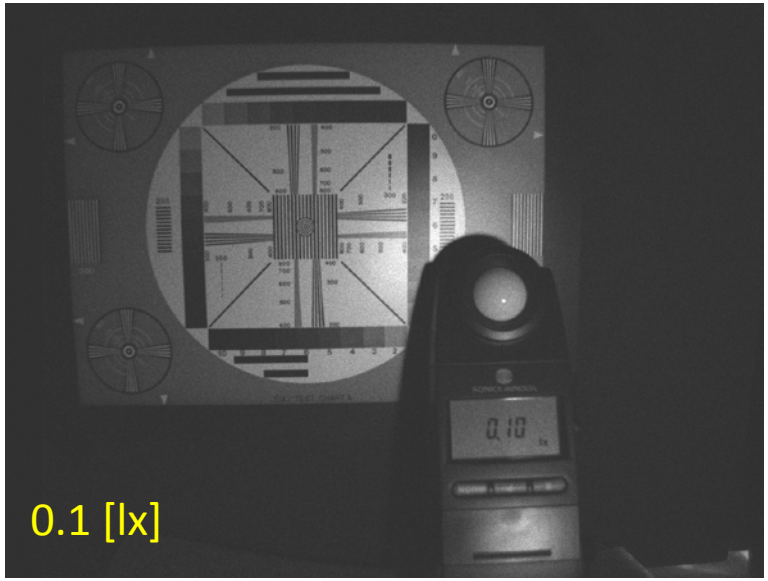


(HS-CMOS, γ=1.65, DR=82dB)

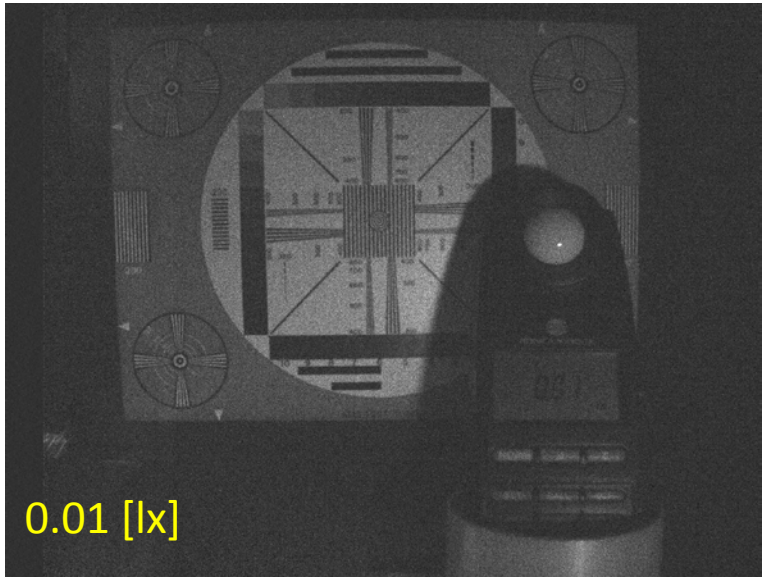
Low Light Level Image (1.3M, 7.1um, @30fps, 1.2e-)

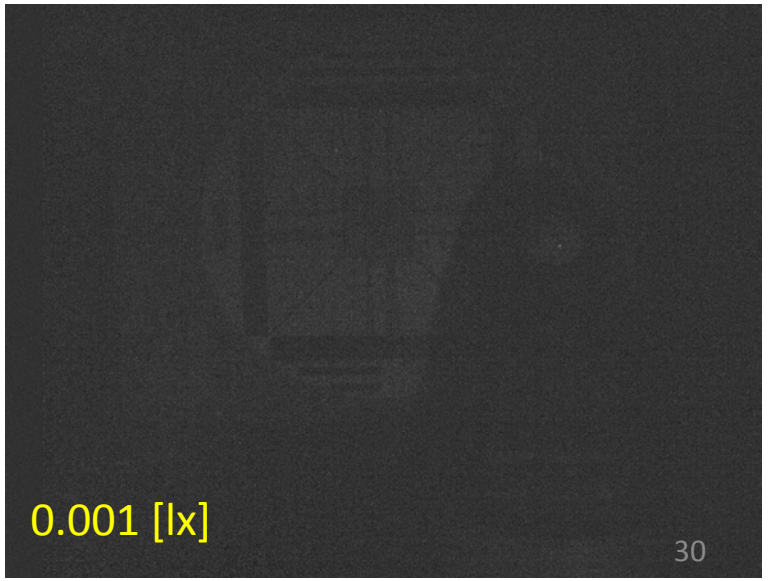


300 [lx]



0.1 [lx]


0.01 [lx]


0.001 [lx]

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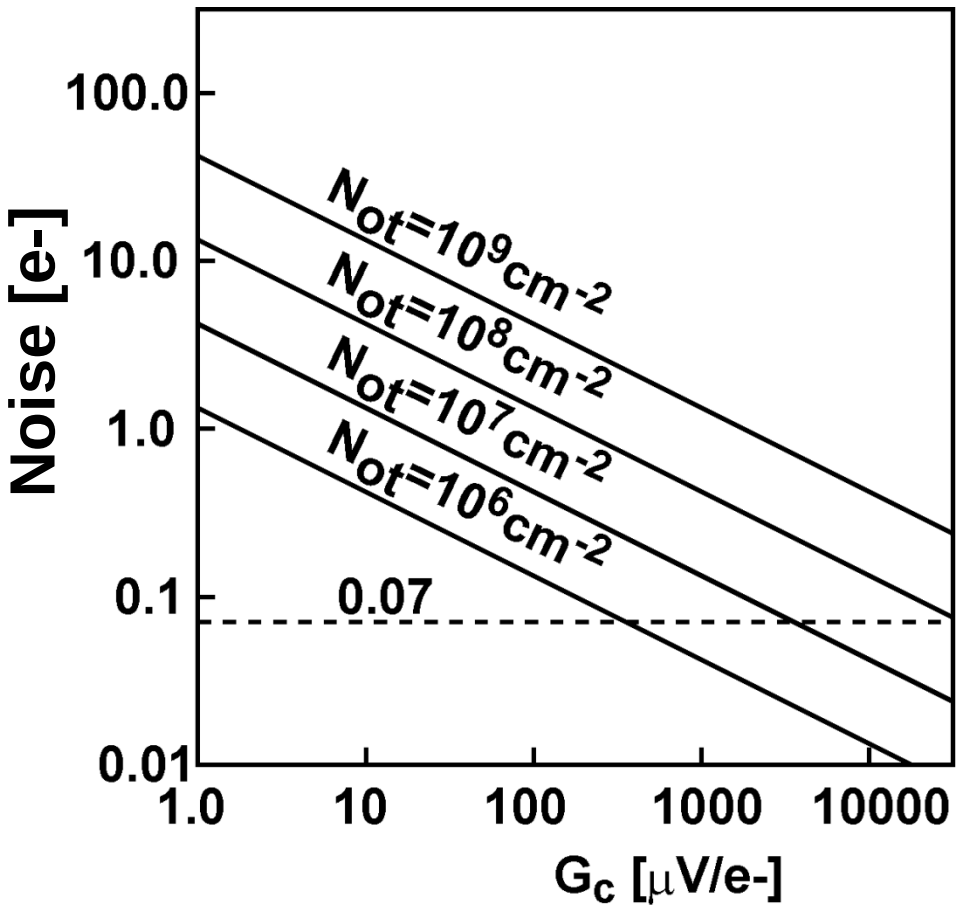
Reports on Low-Noise CISs (<1.1e-)

Technique Used	Noise		Conversion Gain [μV/e-]	Reference
	[μV]	[e-]		
Column Amplifier (G=32), Single-Slope ADC (SSADC)	n. a.	0.8	n.a. (2.1DN/e-)	IISW 2007
Multiple Sampling, Folding Integration/ Cyclic ADC	65μV	0.95	67μV/e-	ISSCC 2011, JSSC (Jan.,2012)
Pseudo Multiple Sampling with SSADC	121μV	1.1	110μV/e-	ISSCC 2010
PMOS Common-Source Pixel Amp.	260μV	0.86	300μV/e-	ISSCC 2010
Buried Channel nMOS S. F. Multiple Sampling with SSADC	32μV	0.7	45μV/e-	ISSCC 2012
nMOS S. F. with Switched Biasing	n. a.	0.5	n. a.	www.caeleste.com, 2011

Low 1/f Noise Pixel + Multiple Sampling Column ADC

How to realize 0.1e- Noise



1/f Noise Spectrum

$$S_{nf} = \frac{q^2 N_{ot}}{C_{ox}^{\ 2} A_G} \frac{1}{f} = \frac{N_f}{f}$$

N_{ot}: Effective Trap Density[cm^{-2}]

Presently, $10^7 \sim 10^8 cm^{-2}$

$$G_c = G_{SF} \frac{q}{C_{FD}}$$

Highest Conversion gain reported ～300e-

- Low 1/f Noise Transistor :Small N_{ot}
- High Conversion Gain Charge Detector (>1000μV/e-) (extremely small capacitance of <0.1fF)

Summary

- Pixel : Charge transfer active pixel with pinned photodiode (Low dark current, kTC noise canceling and high conversion gain)
- Low circuit noise : High gain column readout circuits (using multiple sampling and ADC)
- Low noise at high pixel rate : column ADC is the key
- Low noise and wide dynamic range : enabled by column readout circuits (Advantage of CMOS)
- Sub-electron noise imager: low 1/f noise pixel amplifier (further reduction: high conversion gain)