PHENIX Silicon Pixel Detector Construction, Operation, and the first Results

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Outline
1. Detector Hardware
2. Installation and Peripheral
3. Operation and Physics result
4. Issue and repair work
5. Summary

History
2004.8 First proposal
2007.6 Start Construction
2008.8 Beam test at FERMILAB
2010.10 Barrel assembly start
2010.12 Installed and operation start
Detector and Hardware
Requirements for Vertex Tracker

Heavy Ion collision and polarized proton-proton
up to CMS 200 / 500GeV

Physics side

• High precision tracking for displaced vertex measurement.
  – \( c\tau \sim 100\mu m(D), \sim 400\mu m(B) \)

• Large coverage tracking capability with momentum resolution
  (\(|\eta|<1.2\), and full azimuthally with \(\sigma/P \sim 5\%P\))

Environment side

• High charged particle density ‘\(dN/d\eta\)’ \(~ 700 \ @ \eta=0 \sim 2000\) Tracks
• High Radiation Dose \(~100\)KRad@10Years
• High Luminosity \(2*10^{32}\) cm\(^{-2}\) s\(^{-1}\)@PP -> High rate readout
• Low Material Budget <- avoid multiple scattering and photon conversion for electron measurement by outer detectors.
VTX: Silicon Barrels ~ $2\pi$

Beryllium beam pipe

Layer 0
Layer 1
Layer 2
Layer 3

Pixel: inner 2 layers and Stripixel: outer 2 layers

Life time ($\tau$)

$D^0: 123 \, \mu m$
$B^0: 464 \, \mu m$

DCA

Beam View

West
East
Pixel detector = inner 2 layers of VTX
1\textsuperscript{st} layer: 10 full pixel ladders = 20 half ladders = 40 sensor modules
2\textsuperscript{nd} layer: 20 full pixel ladders = 40 half ladders = 80 sensor modules
Pixel size (Φ x z) 50 µm x 425 µm
Sensor Thickness 200 µm
ΔrΦ = 1.28 cm, Δz = 1.36 cm (Active area)
256 x 32 = 8192 channel / sensor
4 chip / sensor
4 sensor / stave

Total 4M Pixel

Readout by ALICE_LHCB1 chip
- Amp + Discriminator / channel
- Bump bonded to each pixel
- Running 10MHz clock (RHIC 106nsec)
- Digital buffer for each channel > 4 µsec depth
- Trigger capability > FAST OR logic for each crossing
- 4 event buffer after L1 trigger
Reaout overview

In order to meet the PHENIX readout speed requirement, parallel readout (4 x 32 bit) was made.

- Number of data lines is 128 (4 x 32 bit)
- Readout time is 256 (f) x 2 chips x 10 MHz = 51.2 μs

Readout scheme

- Digital Pilot Chip
  - Receiving 4 x 32 bit data from R/O chips
  - Sending data to FPGA
  - Controlling R/O chips

- Analog Pilot Chip
  - Supplying reference voltage for R/O chips.
  - Monitoring supply, bias voltage and temperature on the detector.
  - GOL : Transmit data with 1.6 Gbps
Bus structure

- 6 layers structure
- GND, Power and 4 signal lines

Signal 1; (for Surface Mount Device)

Signal 1 to Signal 4 are connected with through hole

Signal lines; 60 μm pitch

Material Budget; Total ~ 0.26 %
Procedure 3

3. Align each sensor module
Encapsulation of wire

Side view of bonding wire

• Wire has intermittent current due to readout synchronized the level 1 trigger.
• Wire vibrates in magnetic field and may break

Resonance

<table>
<thead>
<tr>
<th>Ratio of widths of wire at GTL ON and OFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.8</td>
</tr>
<tr>
<td>1.0</td>
</tr>
</tbody>
</table>

GTL signal frequency [KHz]

No encap
~ 5.9 KHz
Installation and Peripheral
Layer 0 (PIXEL)  
5 ladders

Layer 1 (PIXEL)  
10 ladders

Completed and installed on 2011.12

Beryllium beam pipe
To remove power dissipation 1560W/VTX, need to cool down pixel/strip detectors.

To avoid detector destruction by heating, need safety interlock system

- Interlock trips off power supply by temperature and flow of coolant.
Operation and Physics result
### Pixel ladder as of 2011 January 15

**Compiled by H. Asano**

<table>
<thead>
<tr>
<th></th>
<th>R</th>
<th>L</th>
</tr>
</thead>
<tbody>
<tr>
<td>West L0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>West L1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>East L0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>East L1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Central Arm
- Acceptance
- West top
- West bottom
- East top
- East bottom

Q/A test by Asano and Akimoto

Date: Jan, 15th, 2011
VTX in Run 2012: p+p at 200 GeV

VTX in Run 2011: Au+Au at 200 GeV

Primary Vertex: BBC vs VTX

Data: AuAu at 200 GeV

Beam size σ (beam) ~ 90 μm
Electron Distance of Closest Approach (DCA)

- Data
- Hadron cont.
- Dalitz
- Conversion $e^\pm$
- Random BG
- Ke3 Decay

200 GeV Au+Au MB
2 GeV/c < $p_T$ < 2.5 GeV/c

PHENIX preliminary
Pixel at PHENIX VTX completed

• Since 2011.12, Operation started.
• We archived
  ✓ Large acceptance ⇒ |η| < 1.2, Δφ ~ 2π
  ✓ Primary vertex resolution (DCA) ⇒ σ ~ 77μm
  ✓ b->e and c->e separation

• Issues: Damage to wires of pixel detectors during 1st run
Issue and repair work
Large temperature excursion due to the cooling interlock broke wires.
- Wire breaks at neck. -> not problem on wire bonding, problems on extra tensions
- 5-10deg -> -5deg for a few minibus, by turning off power ~ 1W/cm², but running cooling system
- Expansion coefficient Encapsulant ~ 300ppm/deg (Sylgard 184 and 186)
  Other material (Myler, Si, Al, Cu Carbon) 20~30ppm/deg
1. Removing encapulant
2. Clean up pad
   • But fear to damage pad
   • Decide wire on bond mark.

• After re-wire bonding, pull tests were performed.
• Always neck breaks with 6-8g tension.
Actions and Repairing work

• Fix interlock system, minimize unnecessary LV off.
• Operate 15-20deg, to decrease thermal shock.
  – No additional broken wire.
• Repair work
  1. Remove encapsulant
  2. Clean up bonding pad
  3. Re-wire bonding
  4. encapsulation

• Encapsulant
  – Available encapsulation material 300ppm/deg
  – Use soft material to minimize extra tension.
    • Penetration 65 (JIS K2207)
• Survive Heat shock test ( 0<->40deg 1min  50 times)
Summary

• We constructed Si Pixel detector for heavy ion collision experiments.
• It works and performs well for physics
  – Vertex resolution 77\(\mu\)m.
• Some of pixel ladders were damaged in the first run. Repair work is underway
Backup
# VTX parameters (in proposal)

## Geometrical dimensions

<table>
<thead>
<tr>
<th>Layer</th>
<th>R (cm)</th>
<th>( \Delta z ) (cm)</th>
<th>Area (cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>2.5</td>
<td>21.8</td>
<td>280</td>
</tr>
<tr>
<td>R2</td>
<td>5</td>
<td>21.8</td>
<td>560</td>
</tr>
<tr>
<td>R3</td>
<td>10</td>
<td>31.8</td>
<td>1960</td>
</tr>
<tr>
<td>R4</td>
<td>14</td>
<td>38.2</td>
<td>3400</td>
</tr>
</tbody>
</table>

## Channel count

<table>
<thead>
<tr>
<th>Sensor size</th>
<th>Channel size</th>
<th>Sensors/ladder</th>
</tr>
</thead>
<tbody>
<tr>
<td>R \times \zeta (cm²)</td>
<td>R \times z (cm²) (256 \times 32 pixels)</td>
<td>R \times z (cm²) (384 \times 2 strips)</td>
</tr>
<tr>
<td>1.28 \times 1.36</td>
<td>50 \times 425 \mu m²</td>
<td>3.43 \times 6.36</td>
</tr>
<tr>
<td>3.43 \times 6.36</td>
<td>80 \mu m \times 3 cm (effective 80 \times 1000 \mu m²)</td>
<td></td>
</tr>
</tbody>
</table>

## Sensors/ladder

<table>
<thead>
<tr>
<th>Ladders</th>
<th>4 \times 4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensors</td>
<td>160</td>
<td>320</td>
<td>90</td>
</tr>
<tr>
<td>160</td>
<td>320</td>
<td>1080</td>
<td>1872</td>
</tr>
</tbody>
</table>

## Radiation length (X/X₀)

<table>
<thead>
<tr>
<th>Sensor</th>
<th>0.22%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Readout</td>
<td>0.16%</td>
</tr>
<tr>
<td>Bus</td>
<td>0.28%</td>
</tr>
<tr>
<td>Ladder &amp; cooling</td>
<td>0.78%</td>
</tr>
<tr>
<td>Total</td>
<td>1.44%</td>
</tr>
<tr>
<td></td>
<td>2.1%</td>
</tr>
</tbody>
</table>

## Layer 1

<table>
<thead>
<tr>
<th>Layer</th>
<th>radius</th>
<th>Detector</th>
<th>Occupancy in Au+Au collision</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer 1</td>
<td>2.5 cm</td>
<td>Pixel</td>
<td>0.53 %</td>
</tr>
<tr>
<td>Layer 2</td>
<td>5.0 cm</td>
<td>Pixel</td>
<td>0.16%</td>
</tr>
<tr>
<td>Layer 3</td>
<td>10.0 cm</td>
<td>Strip</td>
<td>4.5 % (x-strip)</td>
</tr>
<tr>
<td>Layer 4</td>
<td>14.0 cm</td>
<td>Strip</td>
<td>2.5 % (x-strip)</td>
</tr>
</tbody>
</table>