

PHENIX Silicon Pixel Detector Construction, Operation, and the first Results

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Outline

1. Detector Hardware
2. Installation and Peripheral
3. Operation and Physics result
4. Issue and repair work
5. Summary

History

- 2004.8 First proposal
- 2007.6 Start Construction
- 2008.8 Beam test at FERMILAB
- 2010.10 Barrel assembly start
- 2010.12 Installed and operation start

Detector and Hardware

Requirements for Vertex Tracker

Heavy Ion collision and polarized proton-proton

Physics side

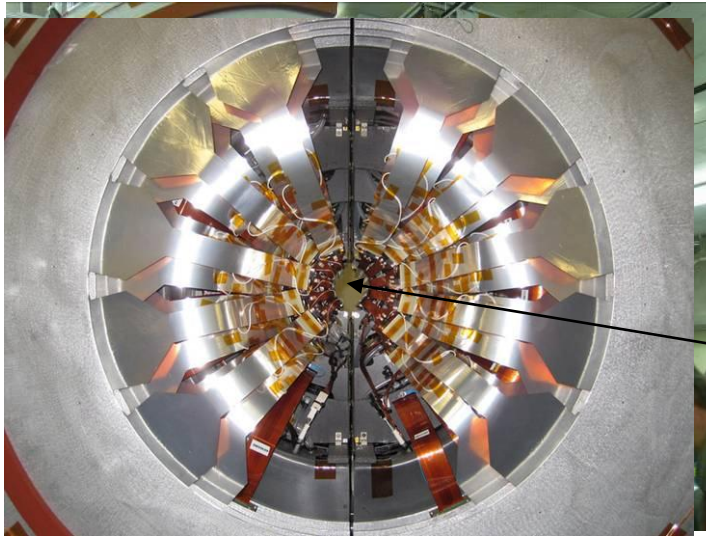
up to CMS 200 / 500GeV

- High precision tracking for displaced vertex measurement.
 - $c\tau \sim 100\mu\text{m}(D), \sim 400\mu\text{m}(B)$
- Large coverage tracking capability with momentum resolution ($|\eta| < 1.2$, and full azimuthally with $\sigma/P \sim 5\%P$)

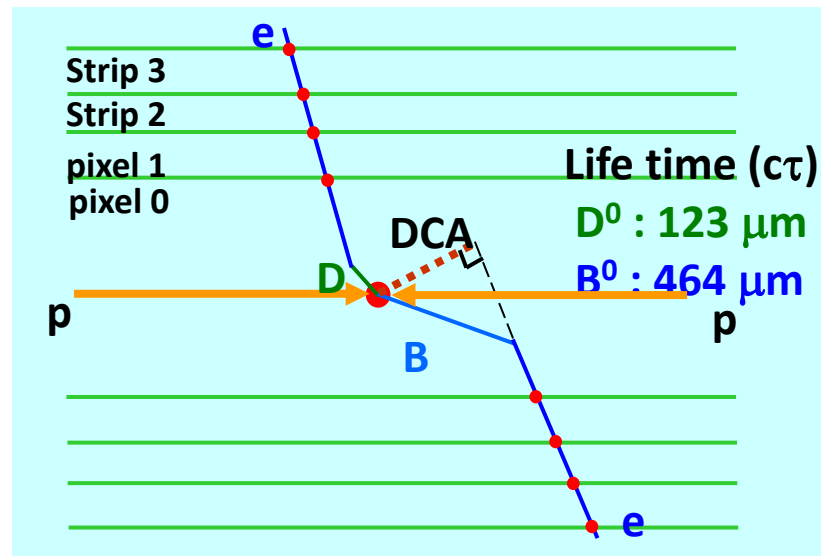
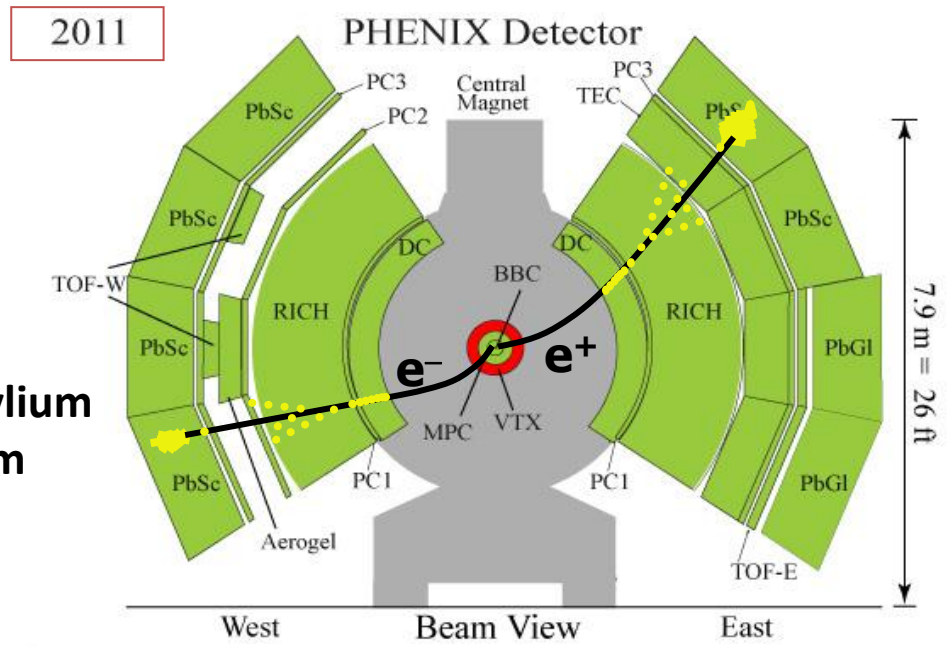
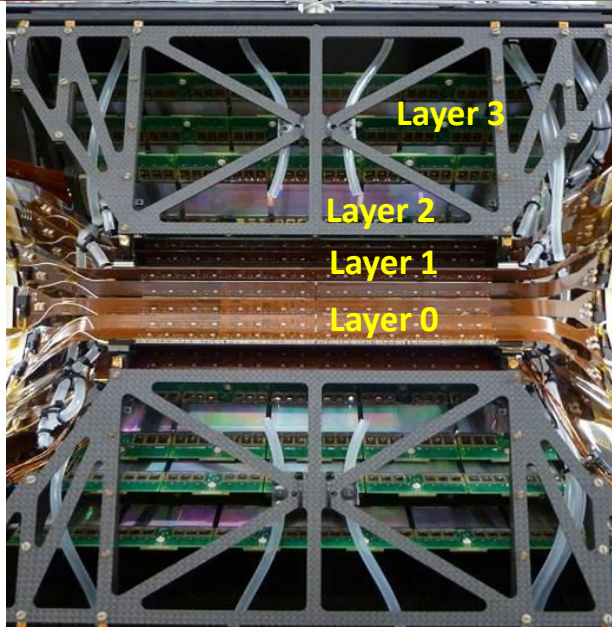
Environment side

- High charged particle density 'dN/d η ' ~ 700 @ $\eta=0 \sim 2000$ Tracks
- High Radiation Dose $\sim 100\text{KRad}@10\text{Years}$
- High Luminosity $2 \cdot 10^{32} \text{ cm}^{-2} \text{ s}^{-1}@PP \rightarrow$ High rate readout
- Low Material Budget \leftarrow avoid multiple scattering and photon conversion for electron measurement by outer detectors.

VTX: Silicon Barrels $\sim 2\pi$

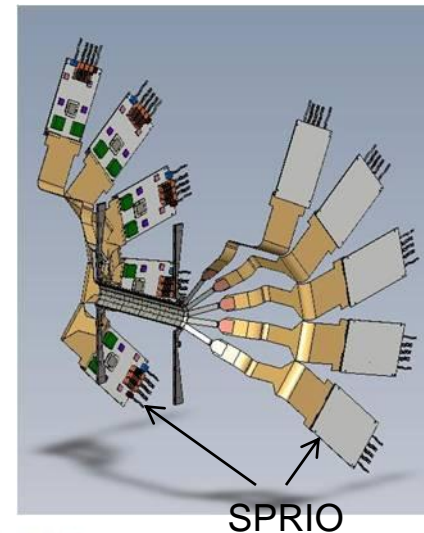
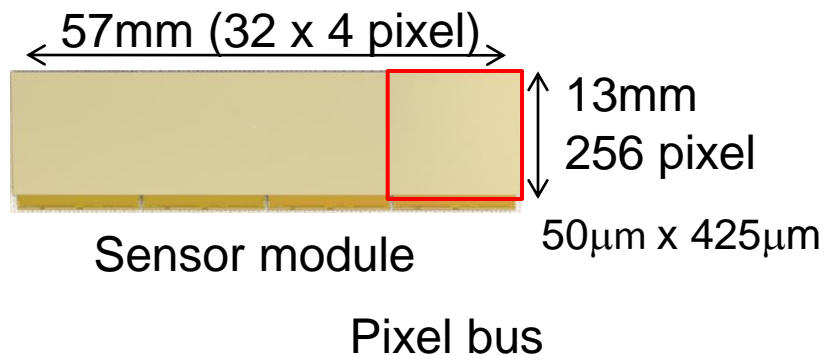
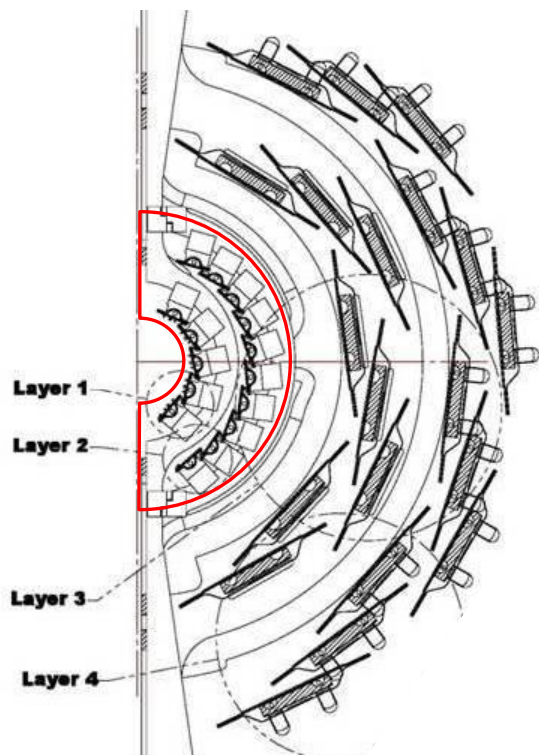


Beryllium beam pipe



Pixel : inner 2 layers and Stripixel: outer 2 layers

Pixel Detector



Pixel sensor modules



Pixel stave (with cooling)

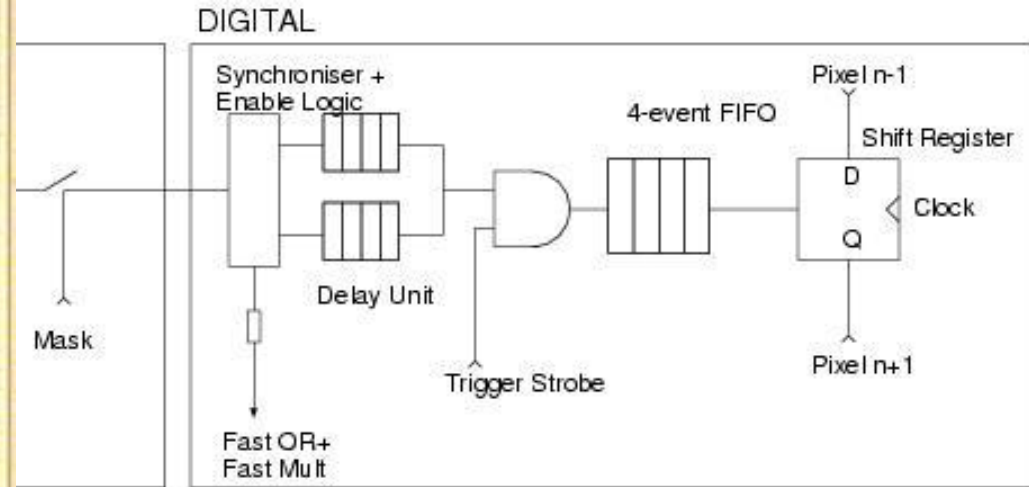
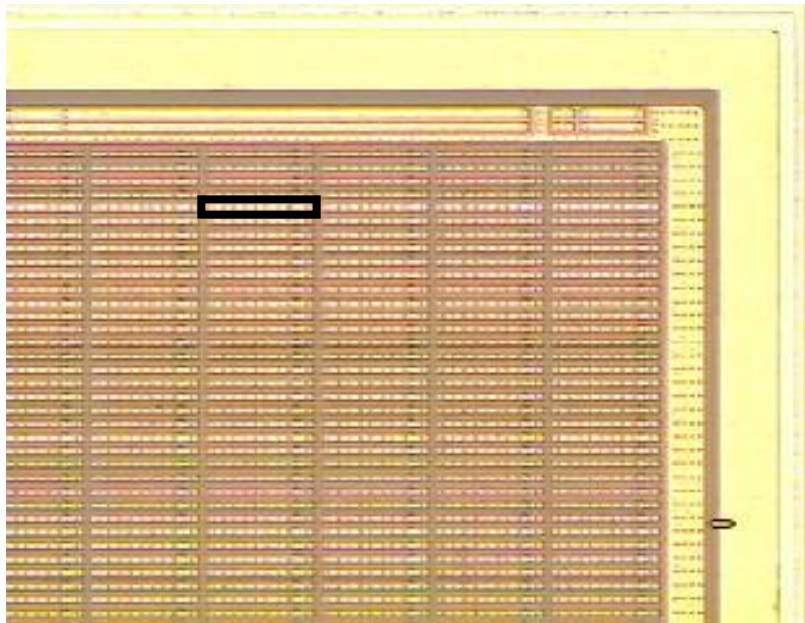


Pixel detector = inner 2 layers of VTX

1st layer: 10 full pixel ladders = 20 half ladders = 40 sensor modules

2nd layer: 20 full pixel ladders = 40 half ladders = 80 sensor modules

PIXEL (Sensor and Readout, bump bonded)



Pixel size($\Phi \times z$) $50 \mu\text{m} \times 425 \mu\text{m}$
Sensor Thickness $200 \mu\text{m}$
 $\Delta r\Phi = 1.28\text{cm}$, $\Delta z = 1.36 \text{cm}$ (Active area)
 $256 \times 32 = 8192$ channel / sensor
4 chip / sensor
4 sensor / stave
Total 4M Pixel

Readout by ALICE_LHCB1 chip

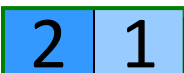
- Amp + Discriminator / channel
- Bump bonded to each pixel
- Running 10MHz clock (RHIC 106nsec)
- Digital buffer for each channel $> 4 \mu\text{sec}$ depth
- Trigger capability $>$ FAST OR logic for each crossing
- 4 event buffer after L1 trigger

Readout overview

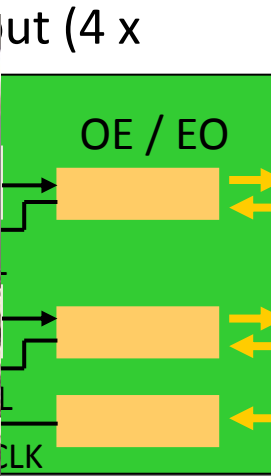
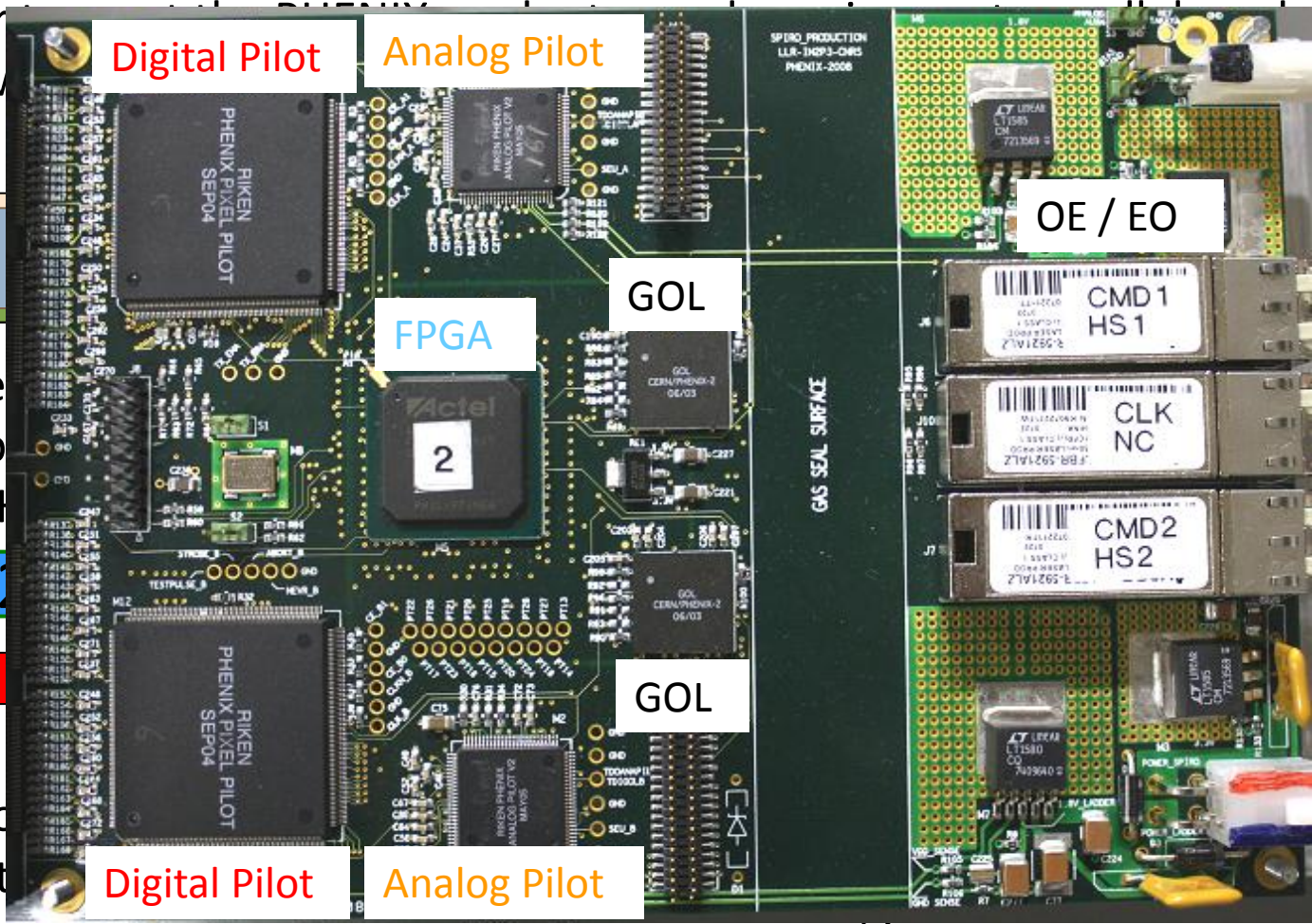
Readout scheme

In order to read out (4 x 32 bit) v

parallel 4 x 32 b at 10 MHz



- Number of channels
- Readout time = 51.2 μs



data from R/O

stage for R/O

chips.

- Monitoring supply, bias voltage and temperature on the detector.
- GOL : Transmit data with 1.6 Gbps

Bus structure

6 layers structure

Wire bonding

Through hole

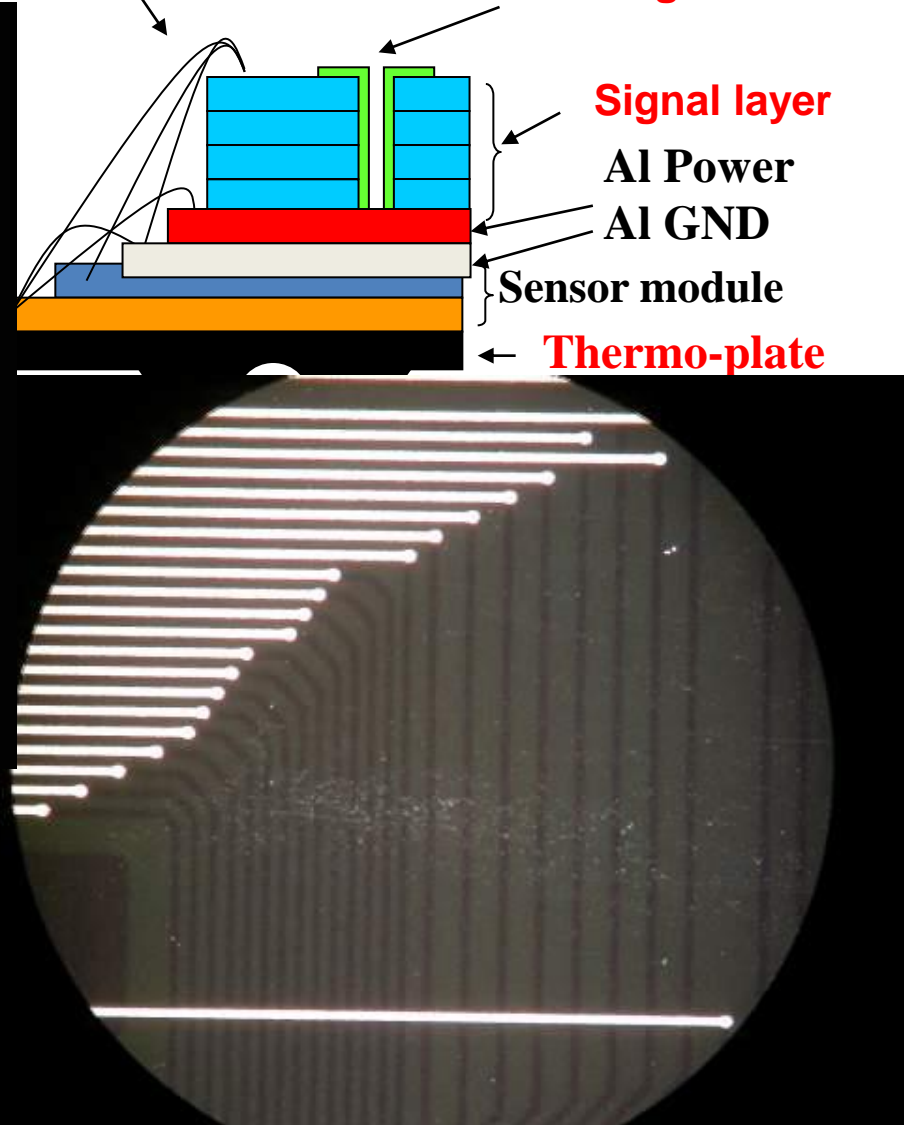
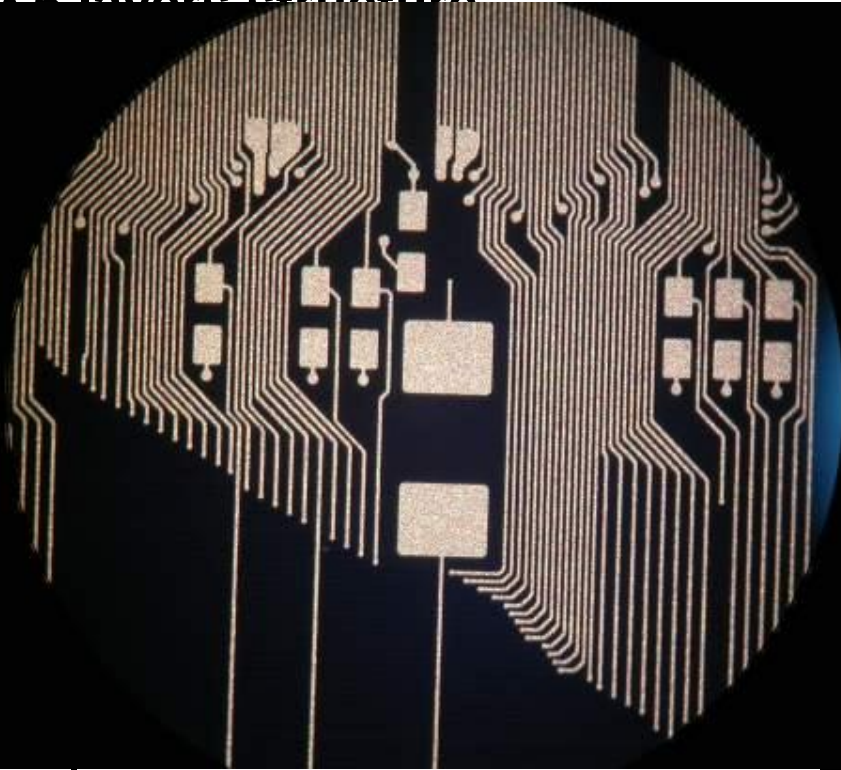
Signal layer

Al Power

Al GND

Sensor module

Thermo-plate



Power 50 µm Al

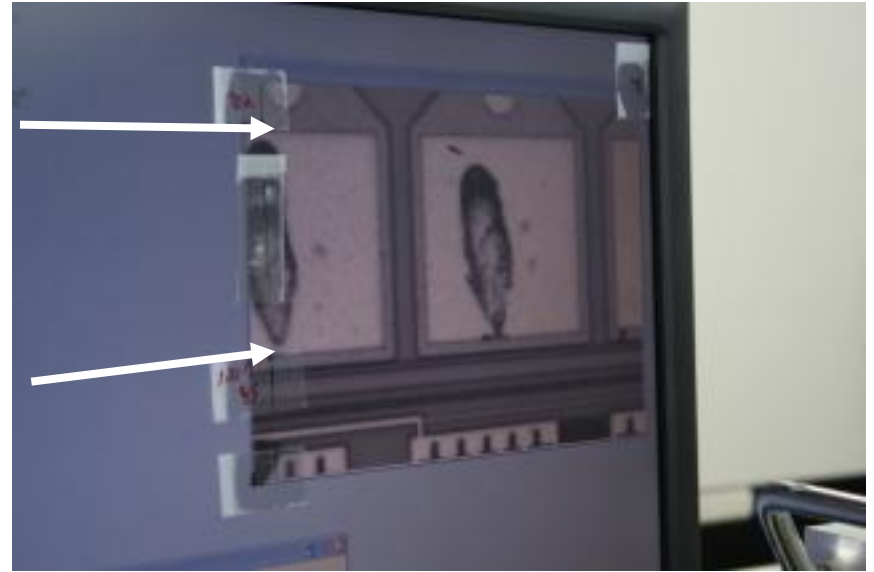
GND 50 µm Al

Signal lines; 60 µm pitch

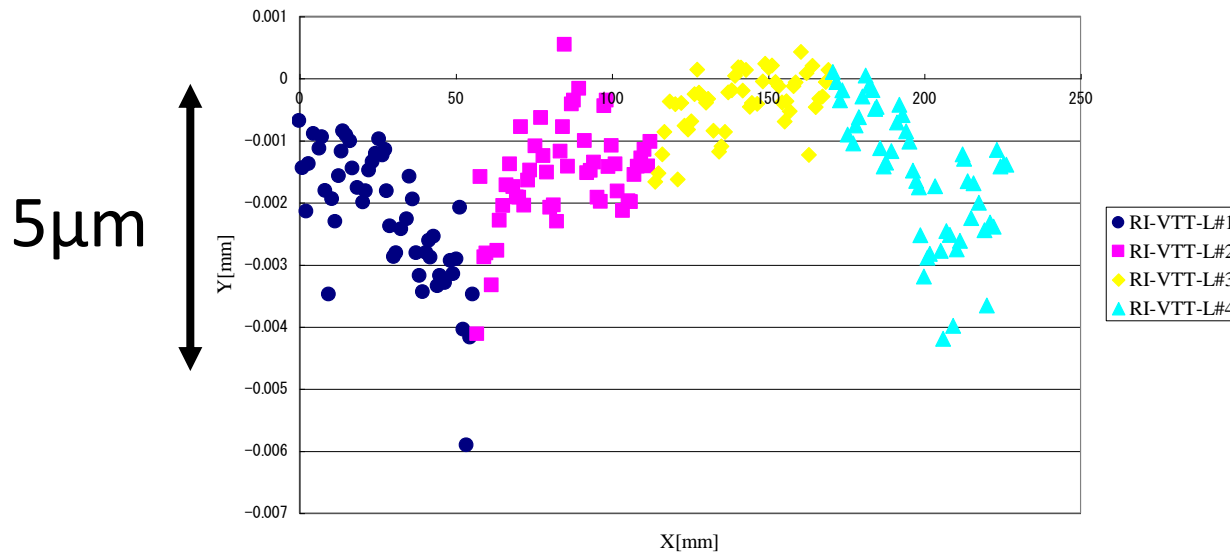
Material Budget; Total ~ 0.26 %

Procedure 3

3. Align each sensor module

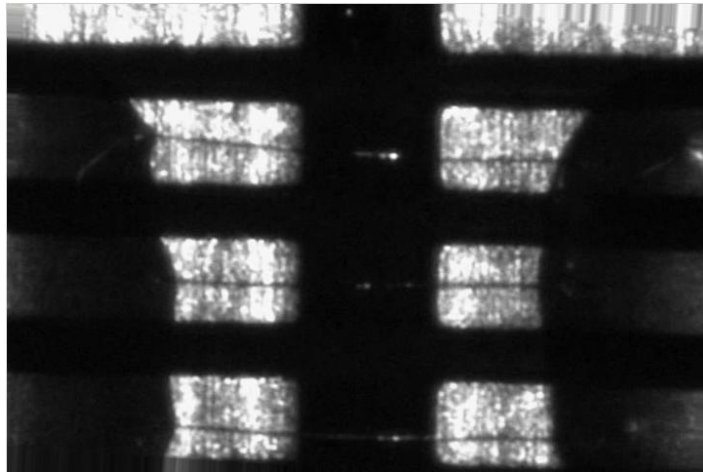


Alignment of FullLadder#1

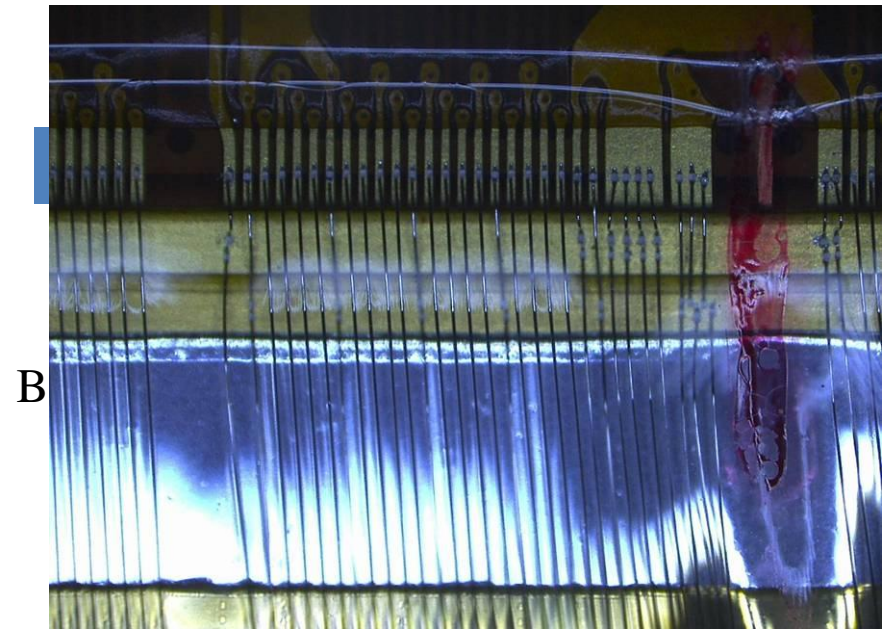


Encapsulation of wire

Side view of bonding wire



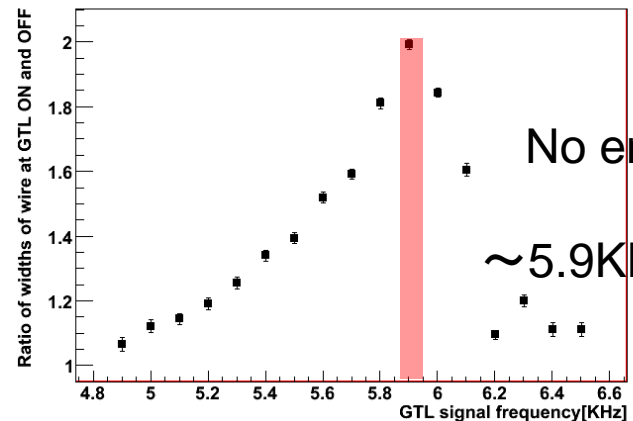
- Wire has intermittent current due to readout synchronized the level 1 trigger.
- Wire vibrates in magnetic field and may break



Cross section

Resonance

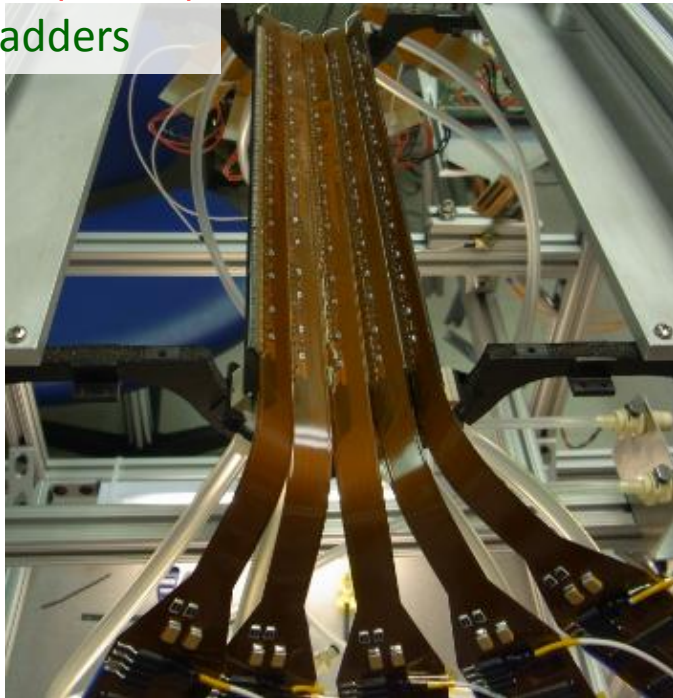
Resonance frequency of 8mm length



Installation and Peripheral

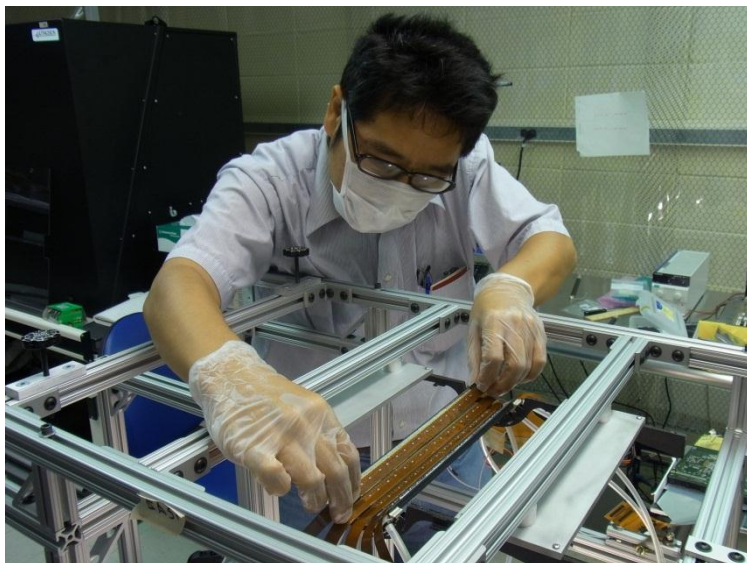
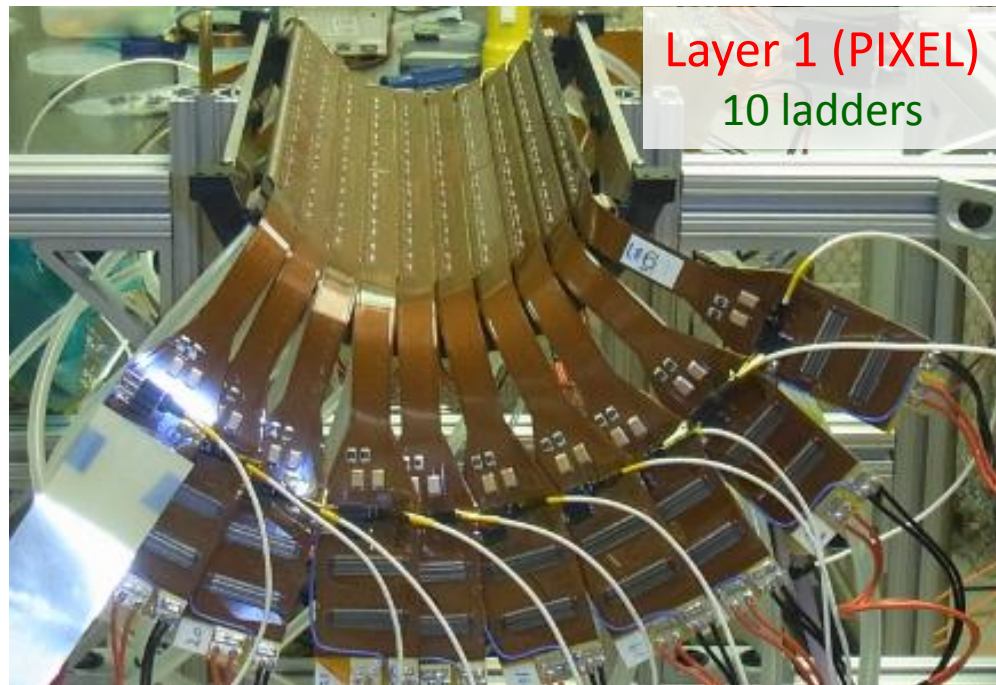
Layer 0 (PIXEL)

5 ladders



Layer 1 (PIXEL)

10 ladders

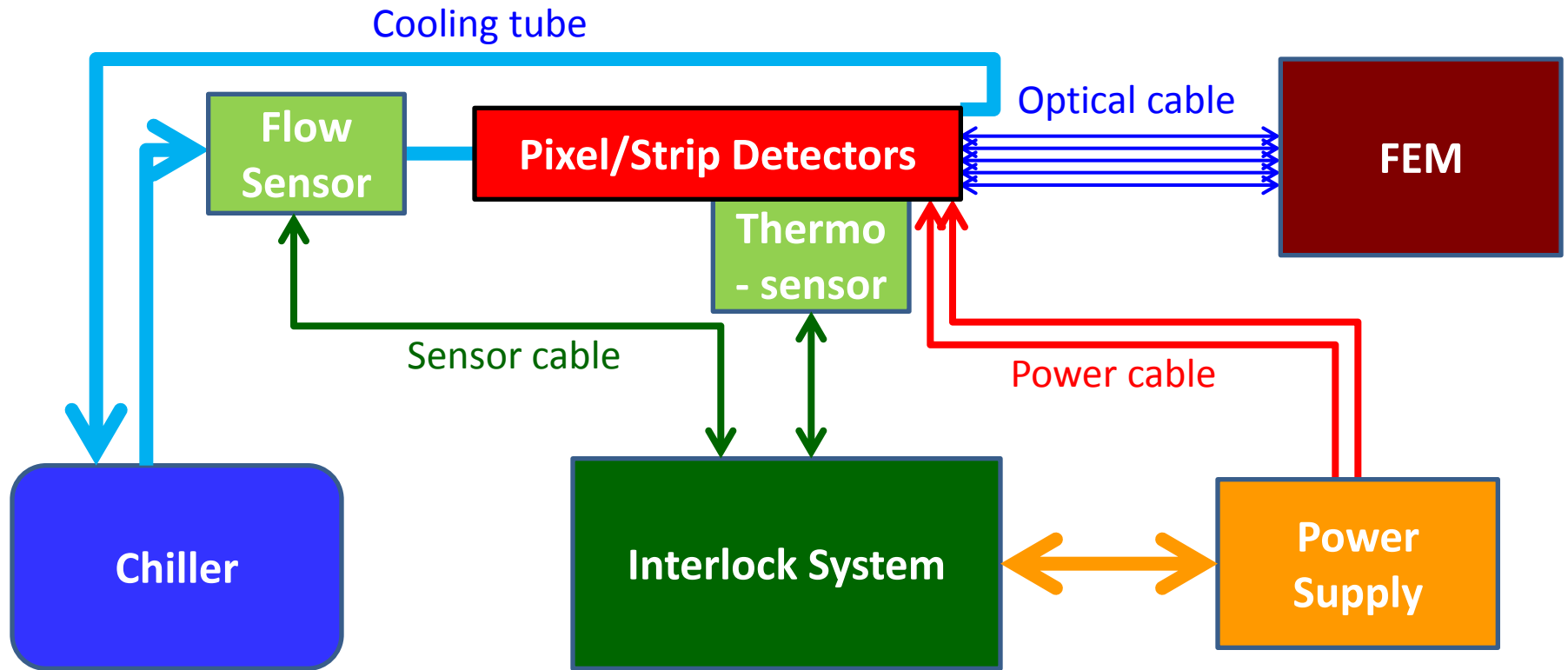


Completed and installed on 2011.12



Beryllium
beam
pipe

VTX System

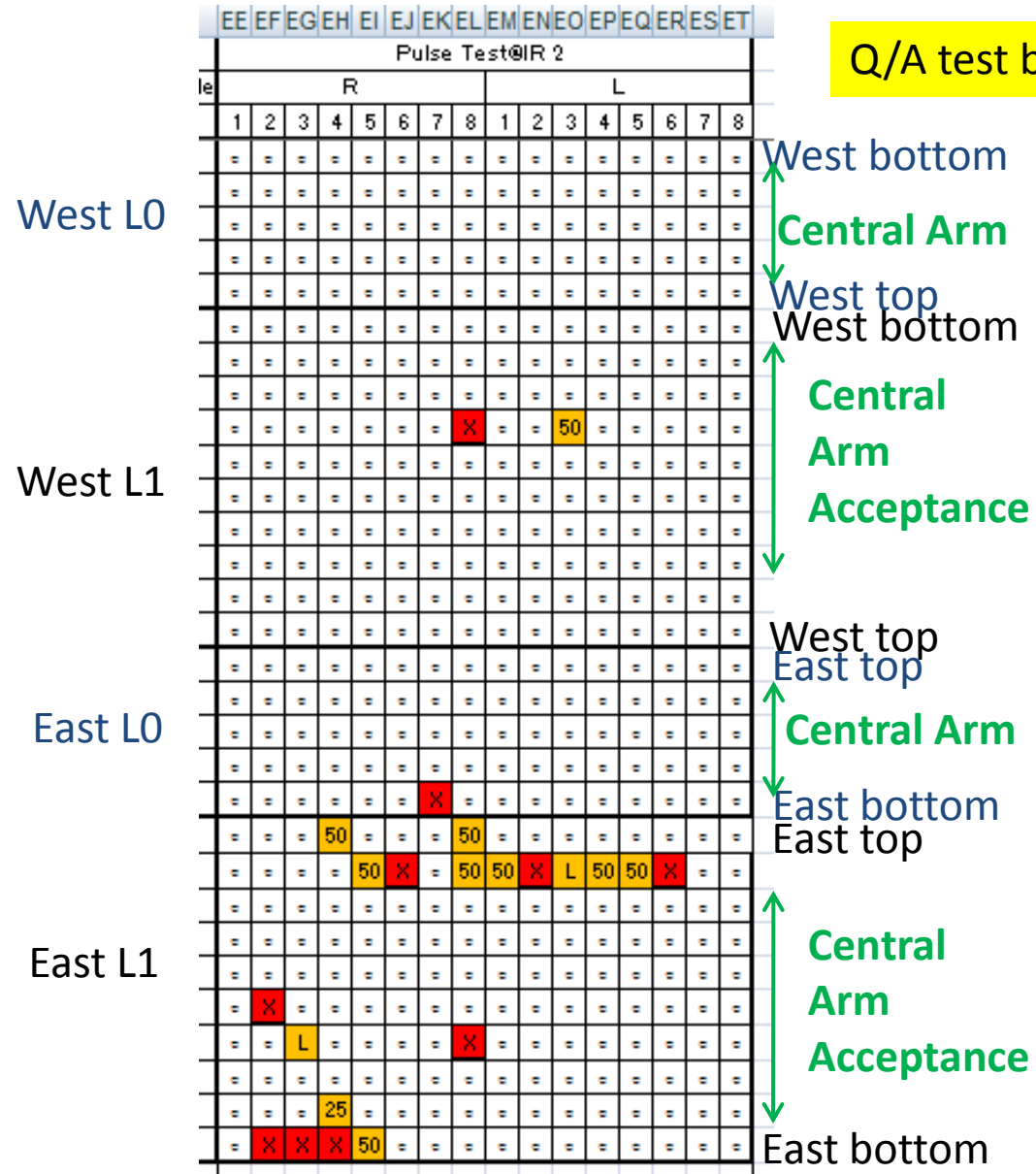


- To remove power dissipation 1560W/VTX, need to cool down pixel/strip detectors.
- To avoid detector destruction by heating, need safety interlock system
 - Interlock trips off power supply by temperature and flow of coolant.

Operation and Physics result

Pixel ladder as of 2011 January 15

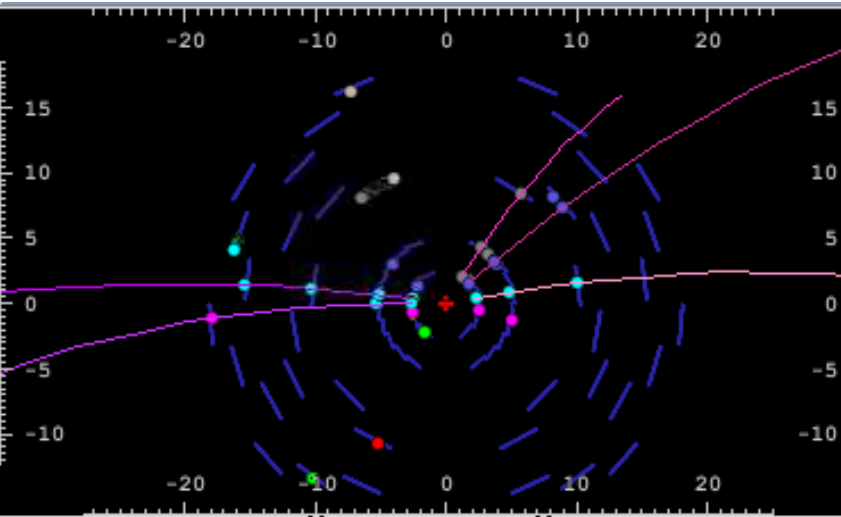
Q/A test by Asano and Akimoto



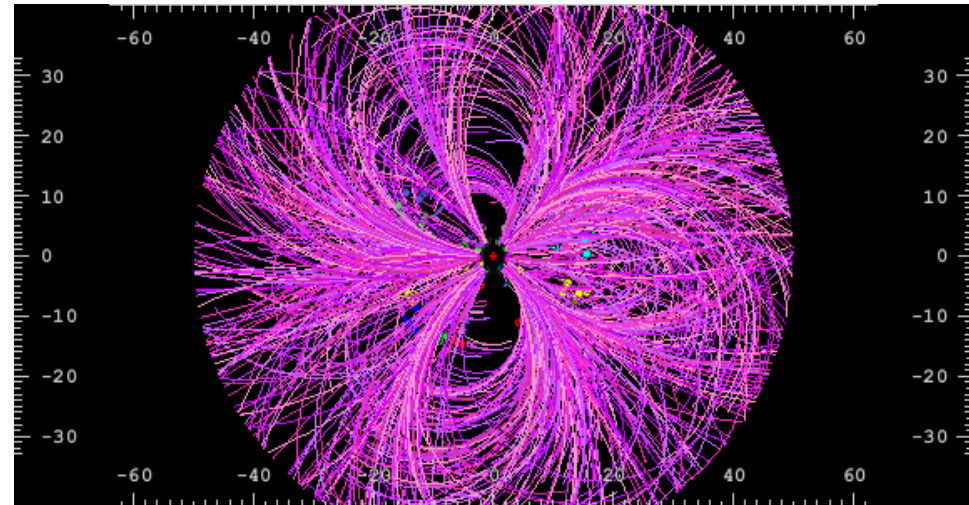
Date: Jan, 15th, 2011

Compiled by H. Asano

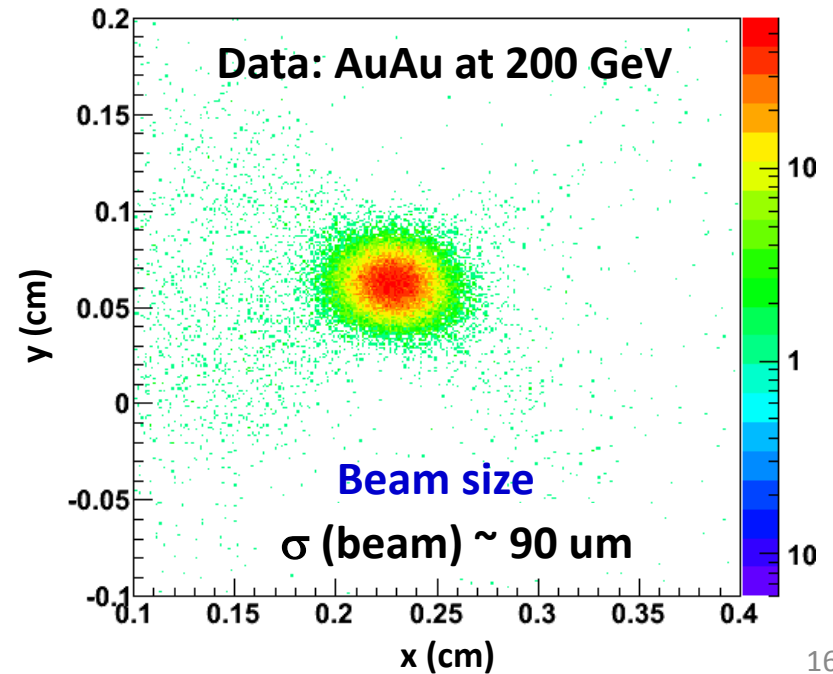
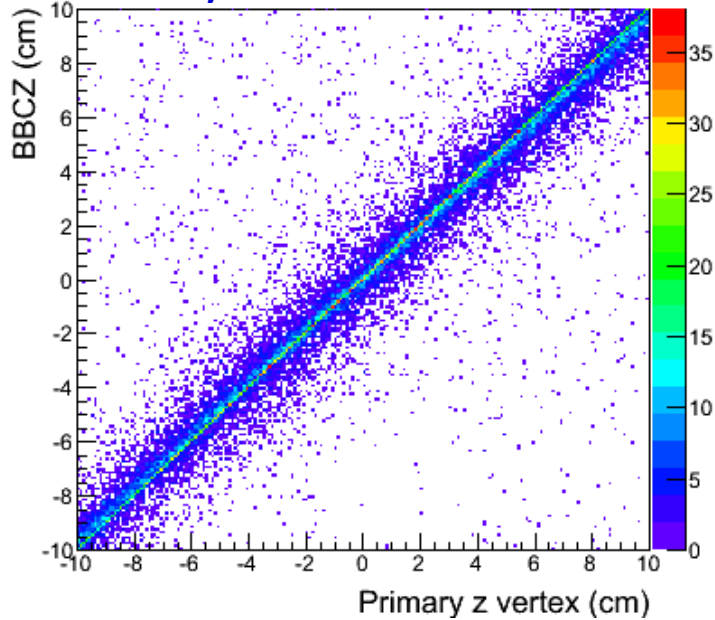
VTX in Run 2012: p+p at 200 GeV



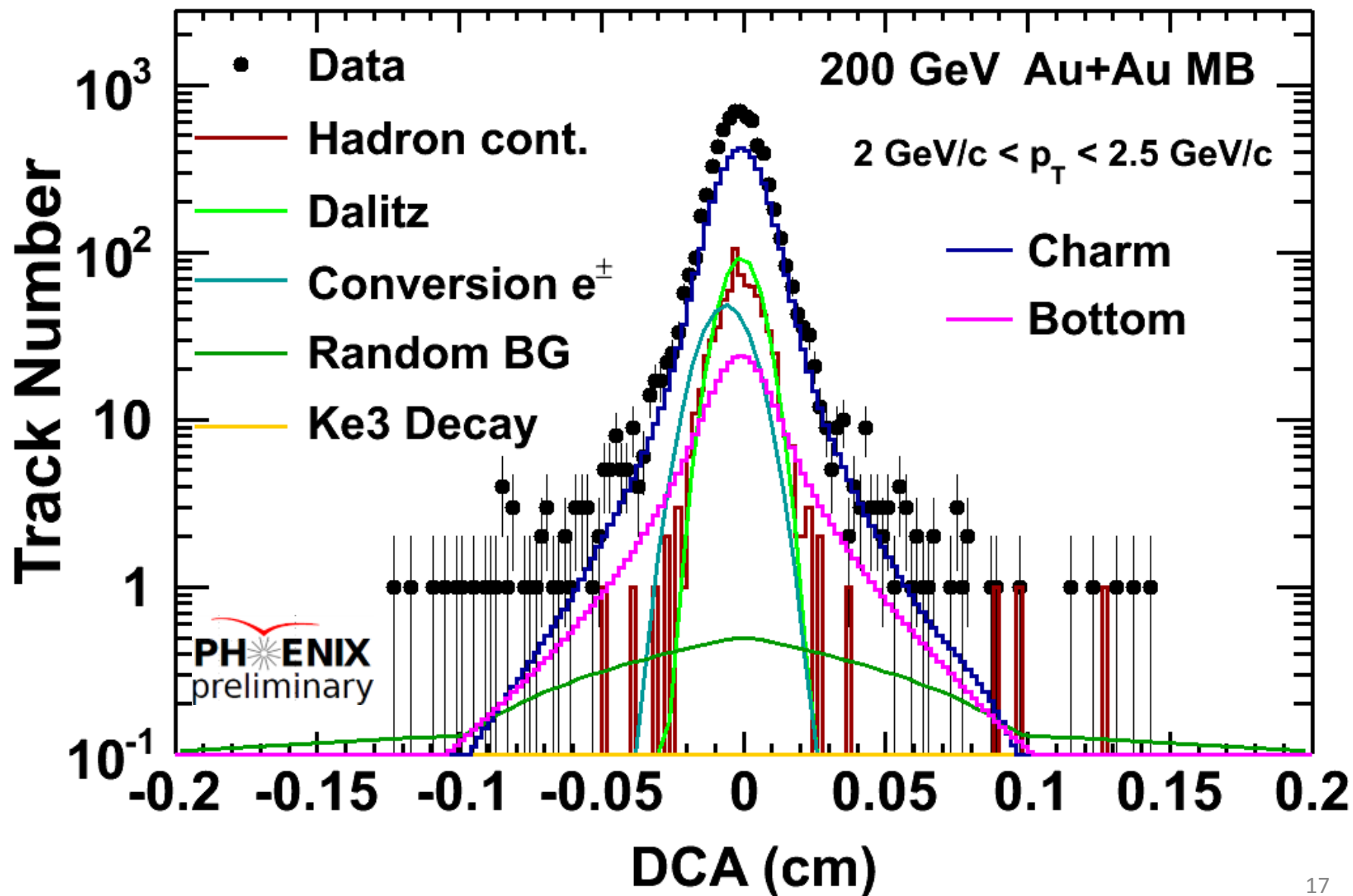
VTX in Run 2011: Au+Au at 200 GeV



Primary Vertex: BBC vs VTX



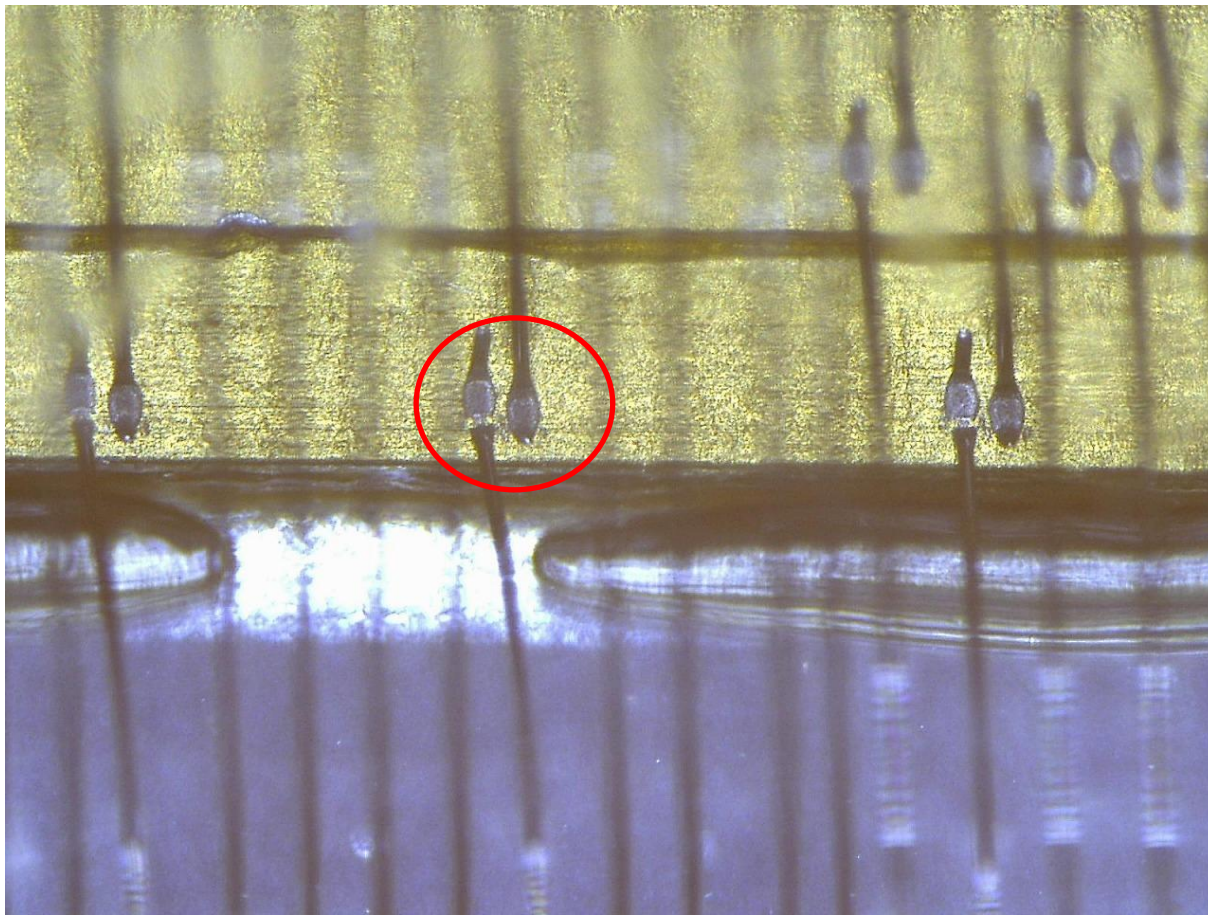
Electron



Pixel at PHENIX VTX completed

- Since 2011.12, Operation started.
- We archived
 - ✓ Large acceptance $\rightarrow |\eta| < 1.2, \Delta\phi \sim 2\pi$
 - ✓ Primary vertex resolution(DCA) $\rightarrow \sigma \sim 77\mu\text{m}$
 - ✓ b->e and c->e separation
- Issues: Damage to wires of pixel detectors during 1st run

Issue and repair work



Bus side

5mm long

Chip side

Large temperature excursion due to the cooling interlock broke wires.

- Wire breaks at neck. -> not problem on wire bonding, problems on extra tensions
- 5-10deg -> -5deg for a few minibus, by turning off power $\sim 1\text{W}/\text{cm}^2$, but running cooling system
- Expansion coefficient Encapsulant $\sim 300\text{ppm}/\text{deg}$ (Sylgard 184 and 186)
Other material (Myler, Si, Al, Cu Carbon) $20\sim 30\text{ppm}/\text{deg}$

Repair



1. Removing encapsulant
2. Clean up pad
 - But fear to damage pad
 - Decide wire on bond mark.

- After re-wire bonding, pull tests were performed.
- Always neck breaks with 6-8g tension.

Actions and Repairing work

- Fix interlock system, minimize unnecessary LV off.
- Operate 15-20deg, to decrease thermal shock.
 - No additional broken wire.
- Repair work
 1. Remove encapsulant
 2. Clean up bonding pad
 3. Re-wire bonding
 4. encapsulation
- Encapsulant
 - Available encapsulation material 300ppm/deg
 - Use soft material to minimize extra tension.
 - Penetration 65 (JIS K2207)
- Survive Heat shock test (0<->40deg 1min 50 times)

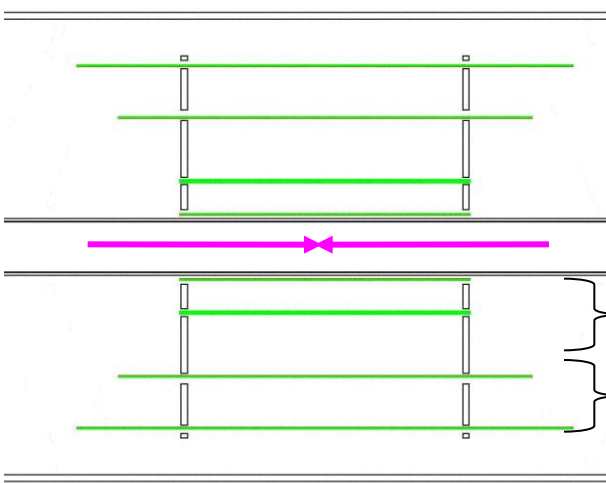
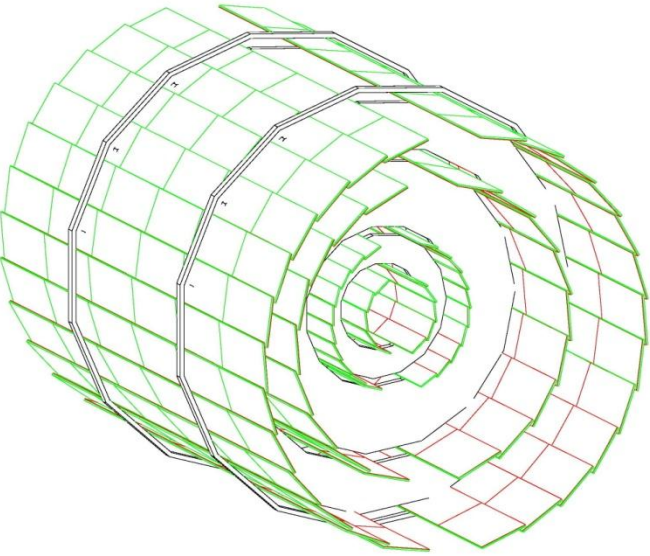
Summary

- We constructed Si Pixel detector for heavy ion collision experiments.
- It works and performs well for physics
 - Vertex resolution $77\mu\text{m}$.
- Some of pixel ladders were damaged in the first run. Repair work is underway

Backup

VTX parameters (in proposal)

Pixel detector Strip detector



VTX	Layer	R1	R2	R3	R4
Geometrical dimensions	R (cm)	2.5	5	10	14
	Δz (cm)	21.8	21.8	31.8	38.2
	Area (cm ²)	280	560	1960	3400
Channel count	Sensor size R \times z (cm ²)	1.28 \times 1.36 (256 \times 32 pixels)		3.43 \times 6.36 (384 \times 2 strips)	
	Channel size	50 \times 425 μm^2		80 $\mu\text{m} \times$ 3 cm (effective 80 \times 1000 μm^2)	
	Sensors/ladder	4 \times 4		5	6
	Ladders	10	20	18	26
	Sensors	160	320	90	156
	Readout chips	160	320	1080	1872
	Readout channels	1,310,720	2,621,440	138,240	239,616
Radiation length (X/X ₀)	Sensor	0.22%		0.67 %	
	Readout	0.16%		0.64 %	
	Bus	0.28%			
	Ladder & cooling	0.78%		0.78 %	
	Total	1.44%		2.1 %	

Layer	radius	Detector	Occupancy in Au+Au collision	
Layer 1	2.5 cm	Pixel	0.53 %	
Layer 2	5.0 cm	Pixel	0.16%	
Layer 3	10.0 cm	Strip	4.5 % (x-strip)	4.7 % (u-strip)
Layer 4	14.0 cm	Strip	2.5 % (x-strip)	2.7 % (u-strip)

