Progress of SOI
Pixel Process

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OUTLINE

• Introduction of SOI Technology
• Recent Progress
• Summary
KEK-Lapis SOI Pixel Related Presentations

Sep. 3. Session 3:
- "Development and Deployment Status of X-ray 2D Detector for SACLA", T. HATSUI.

Sep. 4, Session 4:
- "High-Resolution Monolithic Pixel Detectors in SOI Technology", T. MIYOSHI.
- "A thin fully-depleted monolithic pixel sensor in Silicon On Insulator technology", S. MATTIAZZO.
- "Development and characterization of the latest X-ray SOI pixel sensor for a future astronomical mission", S. NAKASHIMA
- "3D Integration for SOI Pixel Detector", M. MOTOYOSHI.

Sep. 6, Session 6
- "Monolithic Active Pixel Matrix with Binary Counters (MAMBO) ASIC, using a nested well structure to decouple the detector from the electronics", F. KHALID.
- "Test of TRAPPISTe Monolithic Detector System", L. SOUNG YEE.

Poster:
- "High Resolution X-ray Imaging Sensor with SOI Technology", A. TAKEDA.
- "Development of the Pixel OR SOI Detector for High Energy Physics Experiments", Y. ONO.
- "Characterization of SOI Monolithic Detector System", R. ALVAREZ.
- "A study on the dynamic range of integrating SOI chips", Lu YUNPENG
SOI Wafer Production (Smart Cut by SOITEC)

1. Initial silicon
2. Oxidation
3. Implantation
4. Cleaning and bonding
5. Splitting
6. Annealing and CMP touch polishing
7. Donor wafer becomes new wafer A
SOI Pixel Detector (SOIPIX)

Monolithic Detector having fine resolution of silicon and data processing power of CMOS LSI by using Silicon-On-Insulator (SOI) Technology.

Diagram:
- **Si Sensor** (High Resistivity Substrate)
- **Si Sensor** (Buried p-Well)
- **BOX (Buried Oxide)**
- **PMOS**
- **NMOS**
- **LSI Circuit**
- **Charged Particle** (X-ray, Electron, Alpha, ...)
- **Backside Implant**, **Laser Annealing**, **Al deposit**

Dimensions:
- 8 μm
- 40 nm
- 200 nm
- 50~500 μm
SOI Performance: Smaller Junction Capacitance

**Bulk**

**SOI**

Cj is 1/10 of Bulk technology. Gate Capacitance is 30-40% Lower.

High Speed / Low Power
Radiation Tolerance

SOI is Immune to Single Event Effect

But not necessary strong to Total Ionization Dose due to thick BOX layer

This must be remedy for the application under high radiation environment.
Operation at Cryogenic Temperature

Bulk MOS

SOI MOS

4.2K
Feature of SOI Pixel Detector

• No mechanical bonding. Fabricated with semiconductor process only, so high reliability, low cost are expected.

• Fully depleted thick sensing region with Low sense node capacitance.

• On Pixel processing with CMOS transistors.

• Can be operated in wide temperature (4K-570K) range, and has low single event cross section.

• Based on Industry Standard Technology.
# Lapis (*) Semiconductor 0.2 \( \mu \text{m} \) FD-SOI Pixel Process

| Process          | 0.2\( \mu \text{m} \) Low-Leakage Fully-Depleted SOI CMOS  
|                  | 1 Poly, 5 Metal layers.  
|                  | MIM Capacitor (1.5 fF/\( \mu \text{m}^2 \)), DMOS  
|                  | Core (I/O) Voltage = 1.8 (3.3) V  
| SOI wafer        | Diameter: 200 mm\( \phi \), 720 \( \mu \text{m} \) thick  
|                  | Top Si : Cz, \( \sim18 \ \Omega\text{-cm} \), p-type, \( \sim40 \ \text{nm} \) thick  
|                  | Buried Oxide: 200 nm thick  
|                  | Handle wafer: Cz (n) \( \sim700 \ \Omega\text{-cm} \),  
|                  | \quad FZ(n) \( \sim7k \ \Omega\text{-cm} \), FZ(p) \( \sim25 \ k \ \Omega\text{-cm} \)  
| Backside process| Mechanical Grind, Chemical Etching, Back side  
|                  | Implant, Laser Annealing and Al plating  

(*) Former OKI Semiconductor Co. Ltd.
SOIPIX Collaboration:
Regular Multi-Project Wafer (MPW) run. (~twice/year)

0.2 μm Fully-Depleted SOI Pixel Process of Lapis Semiconductor Co. Inc.

JAXA  RIKEN  AIST
Osaka U.  KEK  Tohoku U.
Kyoto U.  Tsukuba U.

U. of Hawaii
Fermi Nat'l Accl. Lab.
Lawrence Berkeley Nat'l Lab.
INP Krakow
U. Heidelberg
Louvain-la-Neuve Univ.

IHEP/IMECAS China

SOIPIX MPW Mask
Examples of SOIPIX Measurements

X-ray Imaging

5mm

Compton Electrons

X-ray Spectrum@-50°C

Al-Kα (1.49 keV)

188 eV (FWHM)

noise 18e- rms
Recent Progress
Easy to make Larger Sensors, and reduce cost per area.
Unit size: 5mm → 6mm
Stitching Exposure

Mask Layout

Exposed Layout

→ Hatsui's Talk
High Resistive wafers

- **CZ(n)**: 0.7 kΩcm, 260 μm
- **FZ(n)**: 7 kΩcm, 500 μm
- **FZ(p)**: 40 kΩcm, 500 μm

Graph showing leakage current versus depletion width for different types of wafers:

- Mechanical Grind
- Chemical Etch

- **VDET**:
  - 237V
  - 377V
  - 320V

- **Leakage Current [A]**
  - Values from $10^{-9}$ to $10^{-7}$

- **Wdepletion [μm]**
  - Values from 0 to 500 μm
3D vertical Integration technique is expected to play an important role in future high performance pixel detector. We have made 3D test chips. These chips were bonded with μ-bump technology (~5 um pitch) of T-micro Co. Ltd.
SOI 3D Bonded Chip

1st SOI 3D Sensor

10 μm
Issues in SOI Pixel

Sensor and Electronics are located very near. This cause ...

Back Gate  Hole Trapping  Cross Talk

We need additional back-plane to suppress these effects.
Buried p-Well (BPW)

- Cut Top Si and BOX
- High Dose

- Keep Top Si not affected
- Low Dose

• Suppress the **Back Gate Effect**.
• Shrink pixel size without loosing sensitive area.
• Increase break down voltage with low dose region.
• Less electric field in the BOX which improve radiation hardness.
\( I_d-V_g \) and BPW

**w/o BPW**

**with BPW=0V**

**NMOS**

Back gate effect is suppressed by the BPW.
• Signal is collected with the deep Buried P-well.
• Back gate and Cross Talk are shielded with the Buried N-well.
Impurity Concentration

Peaks of BNW and BPW are separated ~0.7 μm to reduce capacitance.
Double SOI Wafer

- Shield transistors from bottom electric field
- Compensate electric field generated by the trapped hole in the BOX.
- Reduce crosstalk between sensors and circuits.
Double SOI Process

- SOI1
- BOX1
- SOI2
- BOX2
- Sub Rs > 1K Ω • cm

PS2

PS

2CS

2C

2CT
SEM View of Double-SOI
(post Field-Anneal)

(Thickness of Si & SiO2 layers are not yet optimized)
Suppression of Back-Gate Effect with Middle-Si layer

a) Middle-Si Floating

b) Middle-Si = GND

Back-Gate Effect is fully suppressed with the Middle Si Layer of fixed voltage.

Nch Core Normal-Vt
L / W = 0.2 / 5.0um
Vd=0.1V
Trapped Charge Compensation (Threshold Control) with Middle-Si Layer

Threshold voltage of a transistor is controlled with the bias voltage of the Middle-Si layer. This indicates effects of the trapped charge in the BOX can be compensated with the bias voltage.

Nch Core Normal-Vt
L / W = 0.2 / 5.0 um
Vd=0.1V, Vback: floating
Summary

• SOI technology has many good features; low power, low variability, large operating temperature range, no latch up..., and Industries are moving to extremely thin SOI.

• SOIPIX is monolithic detector, and many of the technical problems initially existed are solved.

• We have ~twice/year regular MPW runs with increasing no. of users.

• The process technology is still progressing; Higher resistivity wafer, Nested well structure, Larger mask size, Stitching, etc. …

• Double SOI wafer is successfully processed.

• We welcome new users to the SOI pixel process.