Development and Deployment Status of X-ray 2D Detector for SACLA

SPring-8 Angstrom Compact free-electron LAser

Takaki Hatsui

on Behalf of SACLA Team & SOPHIAS collaboration

RIKEN SPring-8 Center

Collaborators

- RIKEN, JASRI
  All members of SACLA members, especially,
  Togo Kudo, Takashi Kameshima, Yoichi Kirihara, Shun Ono, Tomohiko Tatsumi, Kazuo Kobayashi, Motohiko Omodani, Kyosuke Ozaki
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  Mitsuhiro Yamaga, Arnaud Amselem, Akio Kiyomichi
  Takashi Sugimoto, Toru Ohata, Toko Hirono, Masahiko Kodera, Ryotaro Tanaka, Tetsuya Ishikawa
- Univ. of Hyogo
  Takeo Watanabe, Tetsuo Harada, Hiroo Kinoshita
- KEK
  Yasuo Arai, and SOIPIX collaboration
- Academia Sinica
  - Minglee Chu, Chih Hsun Lin , Shih-chang Lee
- Private Sector
  - Lapis Semiconductor, Rohm, T-Micro, A-R-Tec Corp., e2v plc, XCam Ltd, Meisei Electric, Kyocera, Clear Pulse Co. Ltd, Hamamatsu Photonics K.K., RIGAKU Corp.
  - Yokogawa Digital Computing, sgi
- Advisory Committee Members
  - Peter Denes (LBNL), Yasuo Arai (KEK), Andrew Holland (The Open Univ.), and Grzegorz Deptuch (Fermilab)

Outline

Multiport CCD *under deployment at SACLA*

SOI Sensor Technology

SOPHIAS *for SACLA*

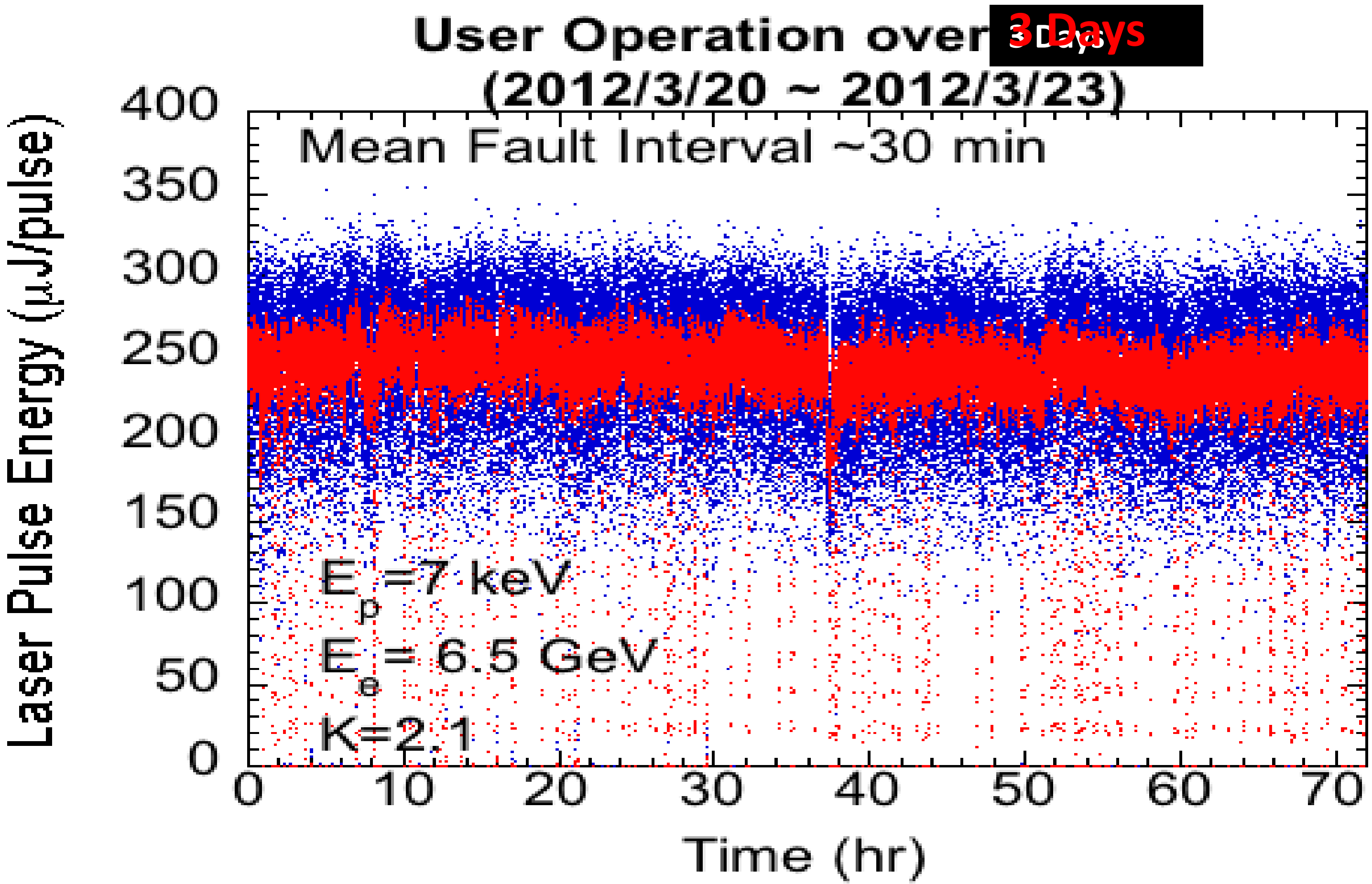
After SOPHIAS

- 2nd X-ray Free-Electron Laser Facility after LCLS
- Shortest wavelength lasing achieved
- Compact XFEL facility

T. Ishikawa et.al., Nature Photonics(2012)

Laser Stability

Laser availability was 92~95% from March to mid. April



Multiport CCD (MPCCD)

Sensor Development

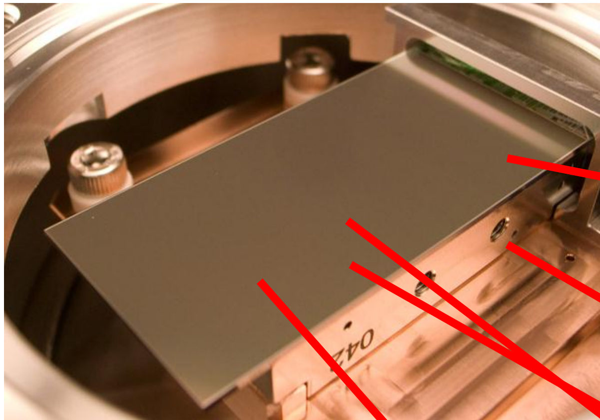
with e2v, XCam

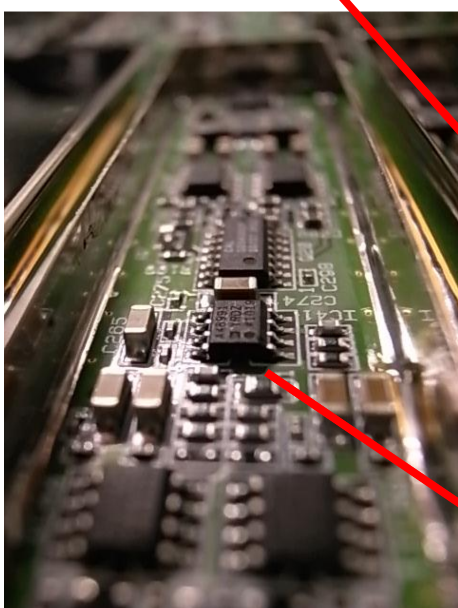
Readout Electronics Development

with Meisei Electronics Co. Ltd

Multiport-CCD (MPCCD) Sensor

Realization by Design Optimization





50 um pixel

512 x 1024 pixels/sensor

Peak signal of 4.4 Me- achieved by optimized pixel design

60 frame/sec achieved by 8 ports/sensor

Device life > 30 Mrad demonstrated

PSF 9 um (std.) for femtosecond 0.5 Me- injection demonstrated

Dead area of 300 um by optimized drive tracks

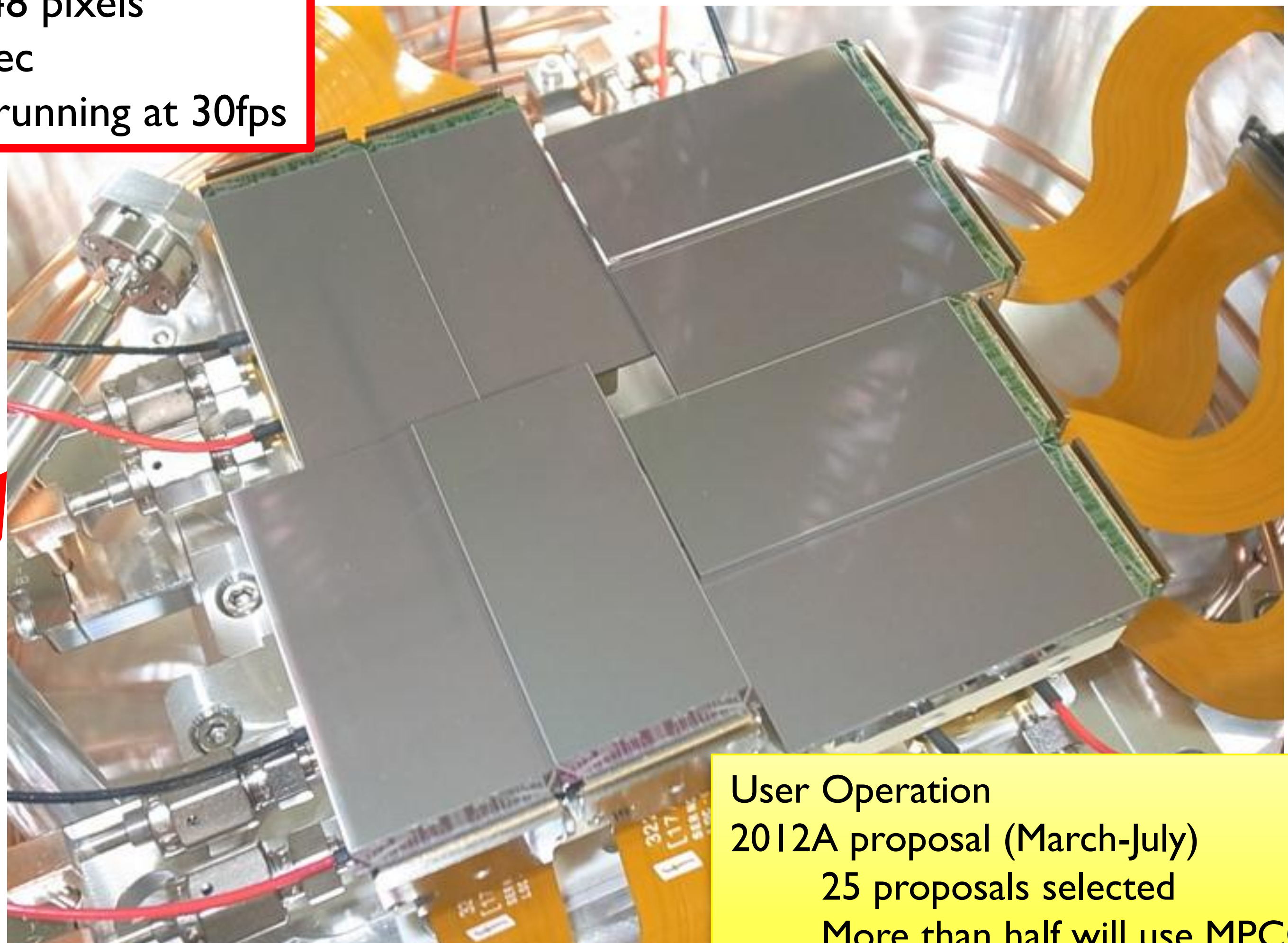
Sensitive Layer: 50 um epi

Development of 300 um deep CCD is started

Noise < 300 e- rms is achieved by dedicated CDS readout electronics.

Multiport CCD Detector with 8 sensor array

Pixel: 50 μm□
2048 x 2048 pixels
60 frame/sec
(currently running at 30fps

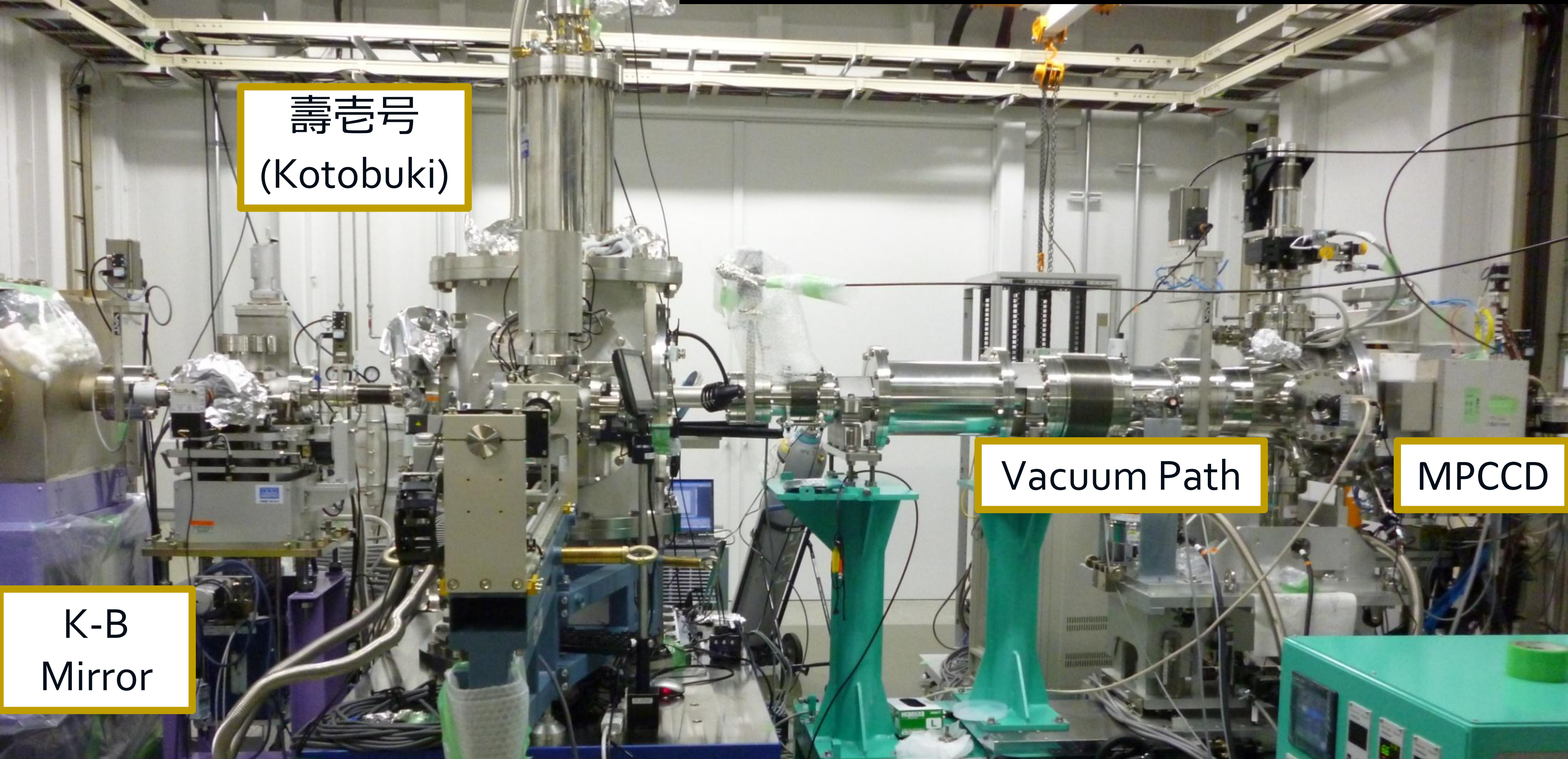


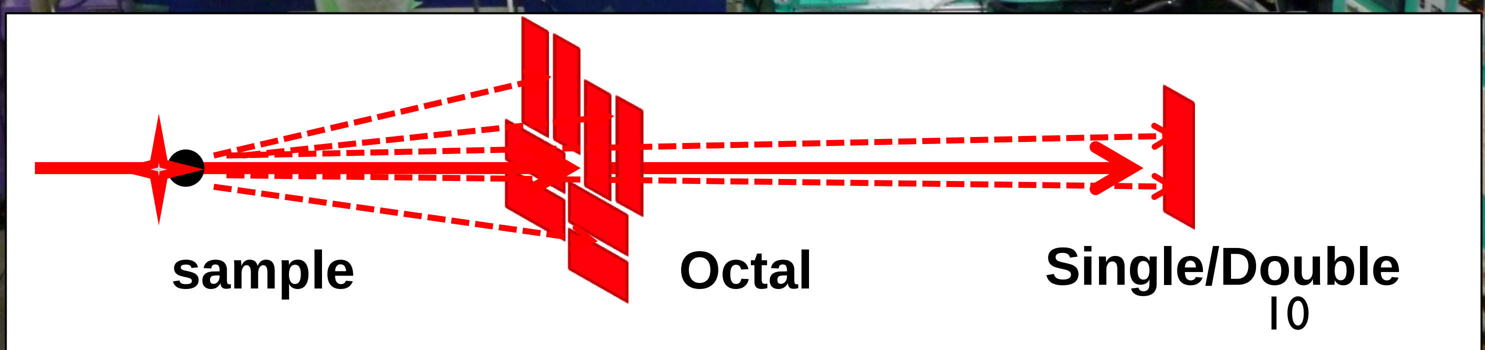
User Operation
2012A proposal (March-July)
25 proposals selected
More than half will use MPCCD detector

Coherent X-ray Imaging

Deployment Example

Cryo-imaging chamber developed by Prof. Nakasako's Gr. (Keio Univ.)





SOI Sensor Technology
from the viewpoint of SR & XFEL applications

with Lapis Semiconductor, A-R-Tec, KEK

See Poster #25 for details: Omodani et.al.

What do We need for XFEL and future (hard) X-ray SR applications?

Observables

- Intensity
- Photon Energy
- Position
- Arrival Time
- Phase

Silicon Sensor

- Single Photon Detection
- ΔE < 120 eV
- < 1 um
- ～ psec

Pixelation Technologies

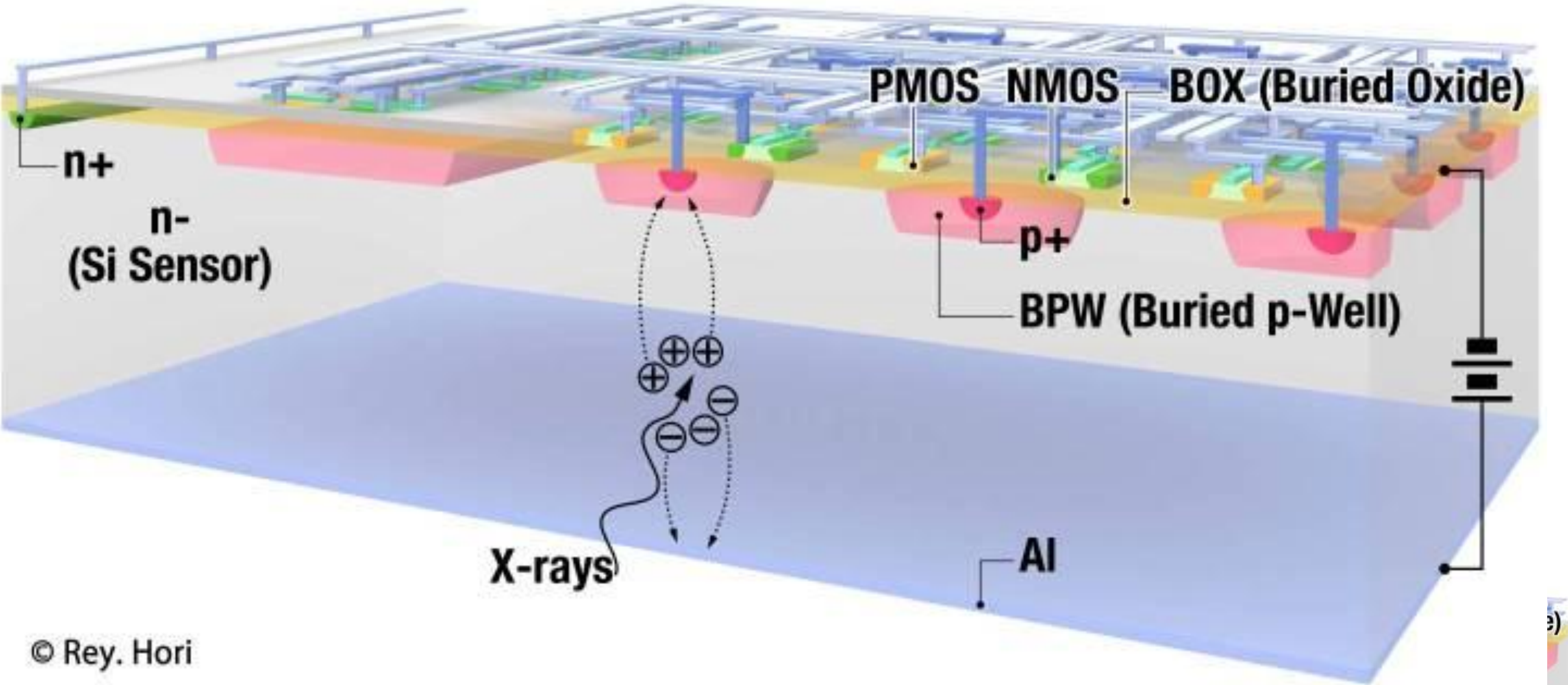
- High integration >10 Mpixel
- High Speed Processing
  In-pixel: ～ GHz/event/pixel
  I/O: Tbps/sensor

Our Choice
SOI Sensor technology

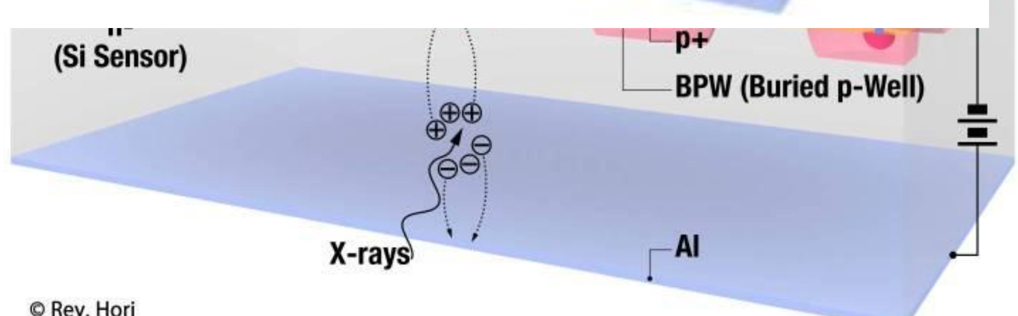
SOI Pixel Detector

Monolithic Si Pixel Sensor with VLSI

Collaboration of KEK, and Lapis Semiconductor, and other institutions



(4-570K) range.



RIKEN joined SOIPIX collaboration
from the end of 2007

SOI Pixel Technology
Process/Device/Simulation

2007 when RIKEN joined SOIPIX collaboration

Back-gate effect

Handle wafer resistivity was low after CMOS process.

- ～400 ohm/cm

Small sensor chip size compared to other technology

- 20 mm x 20 mm

Devices were for digital, not for analog circuitry.

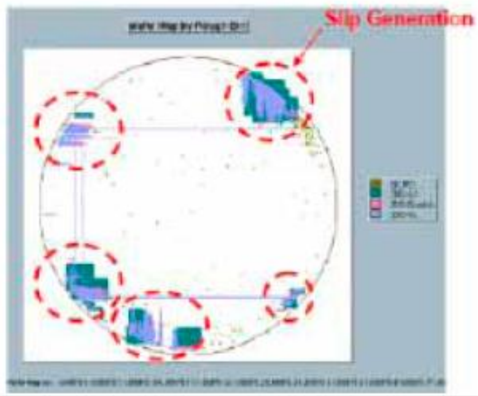
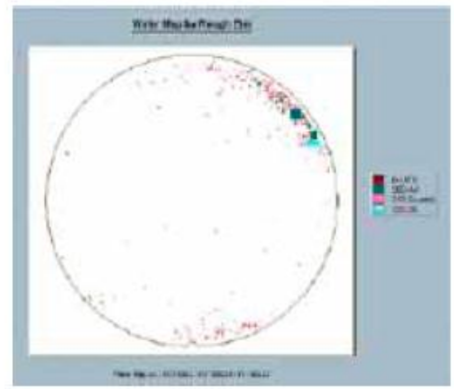
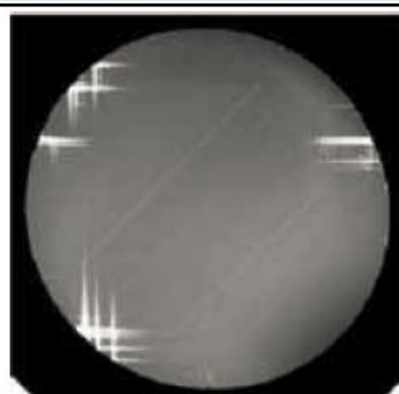
X-ray Radiation hardness was not evaluated.

Current Status

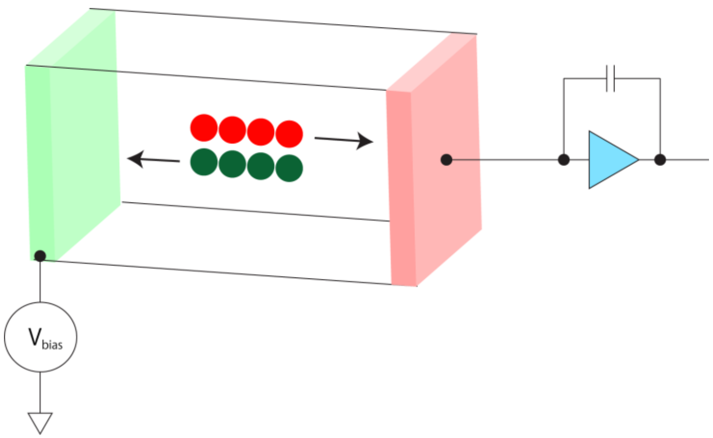
- **Buried P-well proposed by KEK, and now extensively used.**

Critical Achievements in Process Technologies for XFEL applications
8 Inch FZ SOI wafer for full depletion of 500 um

Courtesy of Lapis Semiconductor

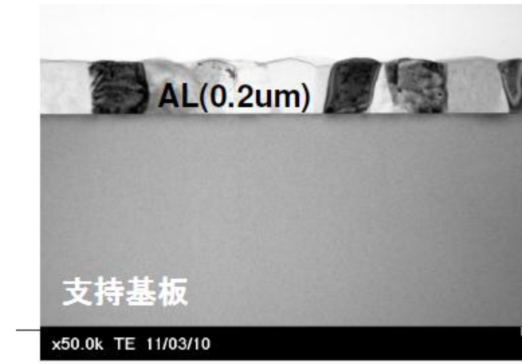
	Conventional Process	Improved Process	tool
SOI wafer fabrication			KLA Tencor SP-1
Pixel detector fabrication			X-ray Topography

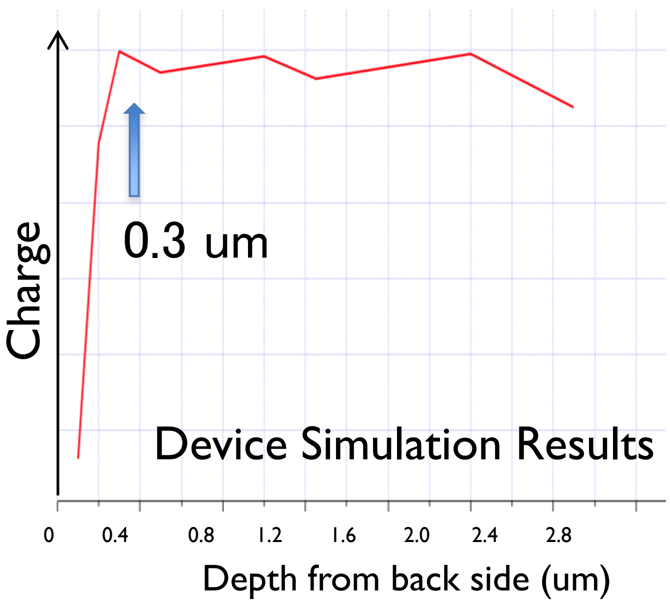
Critical Achievements in Process Technologies for XFEL applications
Backside processing



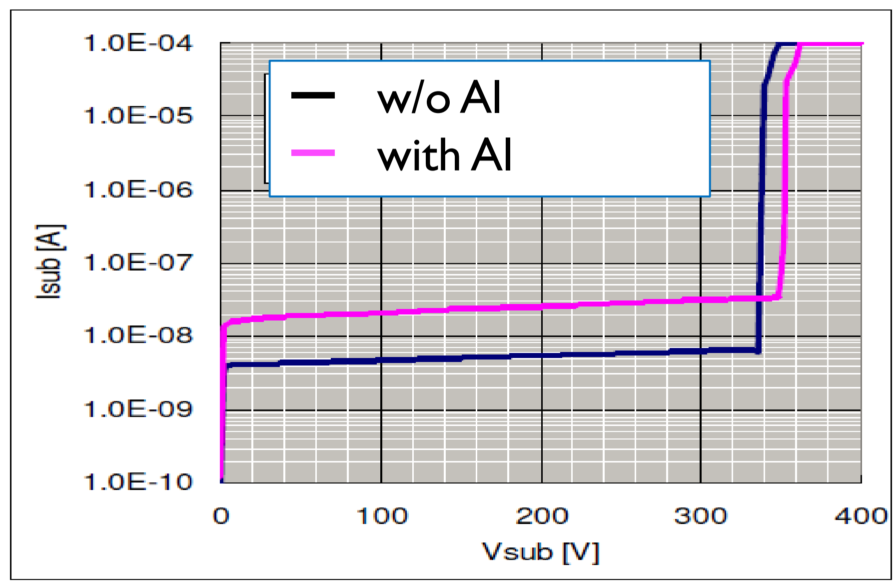
Backside Processing

- CMP
- Wet etching
- Implant
- Laser annealing
- Al deposition

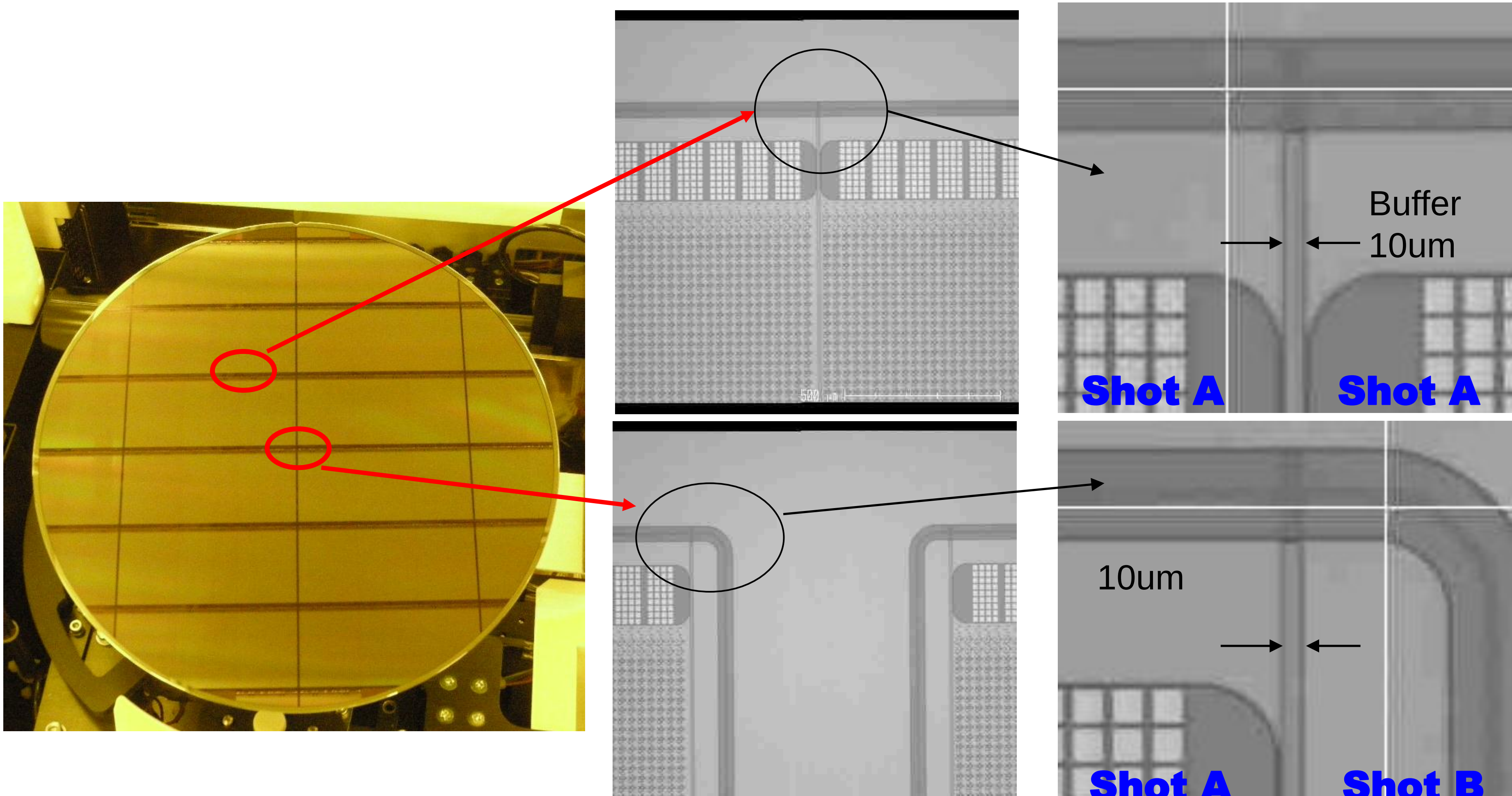




Inverse current



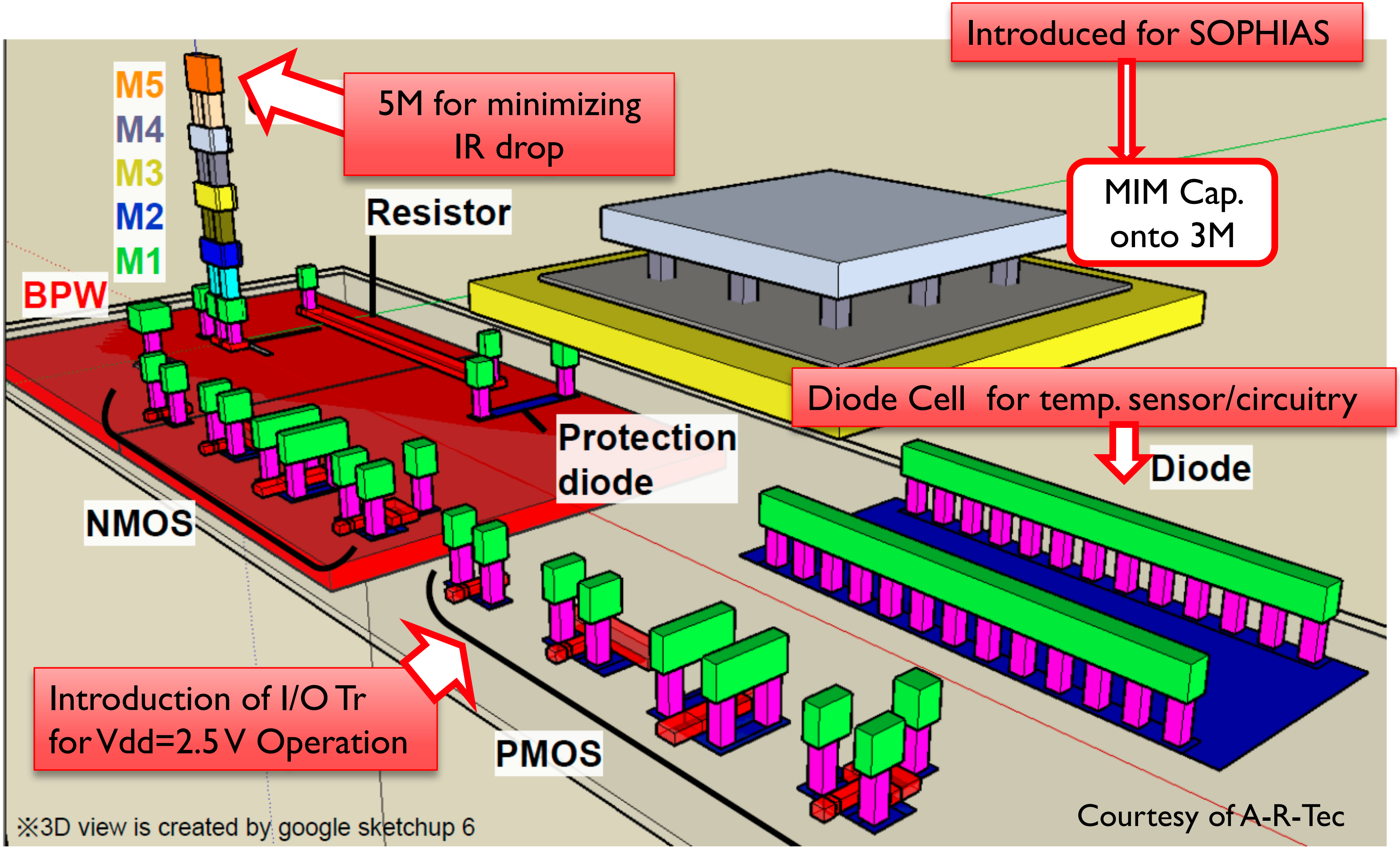
◆Stitching Process: Intermediate Observation



- ◆Stitching Layers: guard rings, M1
- ◆ Pixel Gap by Stitching is designed to match to the pixel size of 30 um
- ◆Stitching error in X/Y directions < 0.025 um

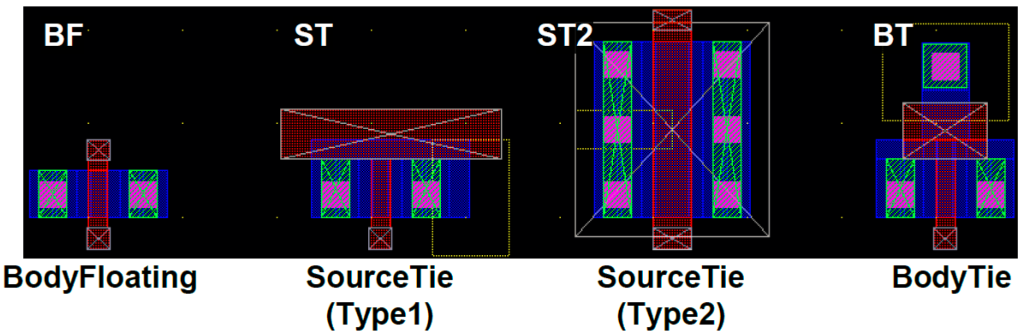
Courtesy of Lapis Semiconductor

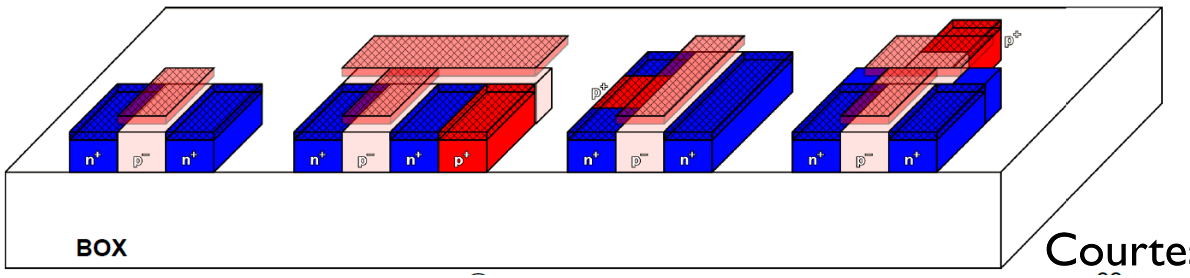
Device/Process Introduction Critical for SOPHAS



1/f & 1/f² Noise Suppression

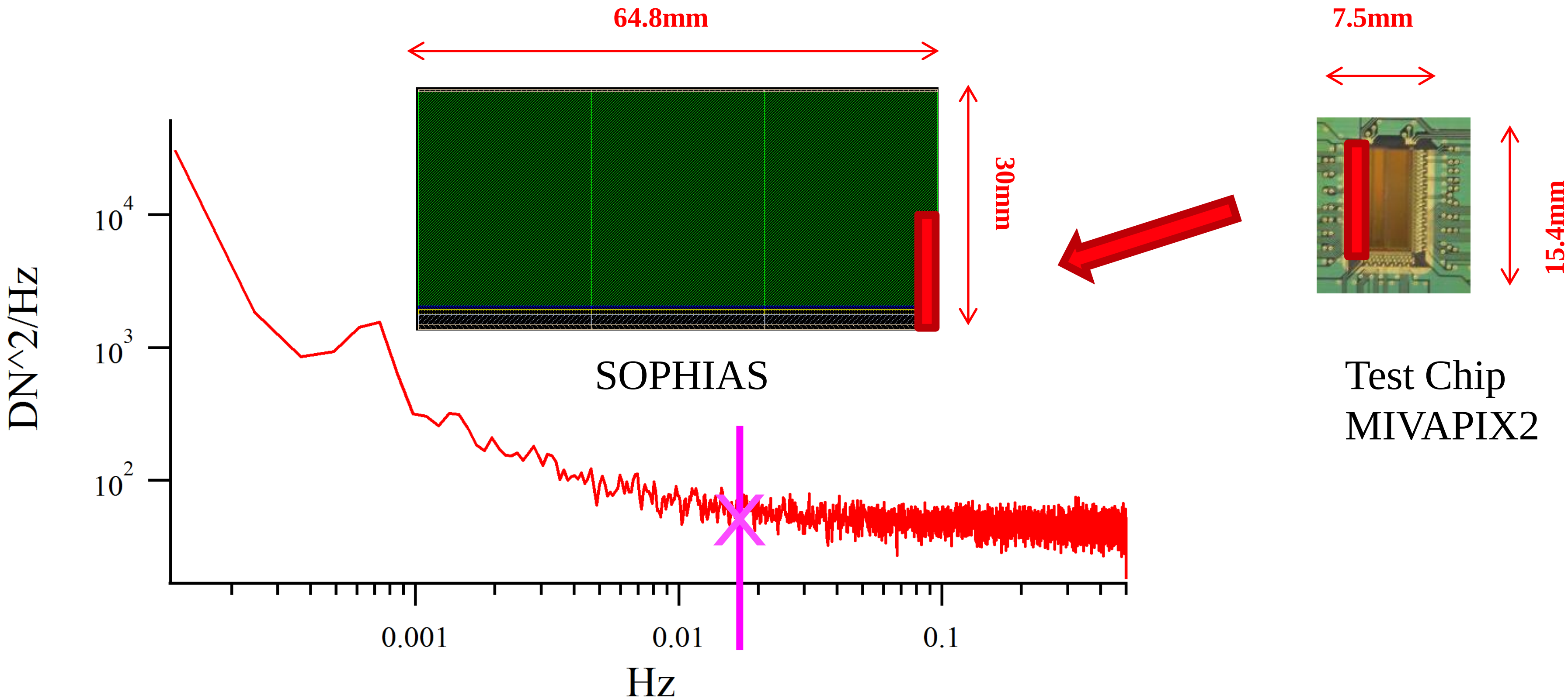
- Fully Depleted SOI Transistor (FD-SOI Tr):
  - Body Floating Tr
    - Large 1/f noise due to body floating
  - Source Tie/Body Tie Tr Pcell has been introduced.
  - 1/f & 1/f² noise simulation environment has been successfully introduced.





Courtesy of A-R-Tec

1/f Noise:
Simulation and Measurement by Test Chip



SOI Pixel Technology Process/Device/Simulation

2007 when RIKEN joined SOIPIX collaboration

Back-gate effect

Handle wafer resistivity was low after CMOS process.

- ～400 ohm/cm

Small sensor chip size compared to other technology

- 20 mm x 20 mm

Devices were for digital, not for analog circuitry.

X-ray Radiation hardness was not evaluated.

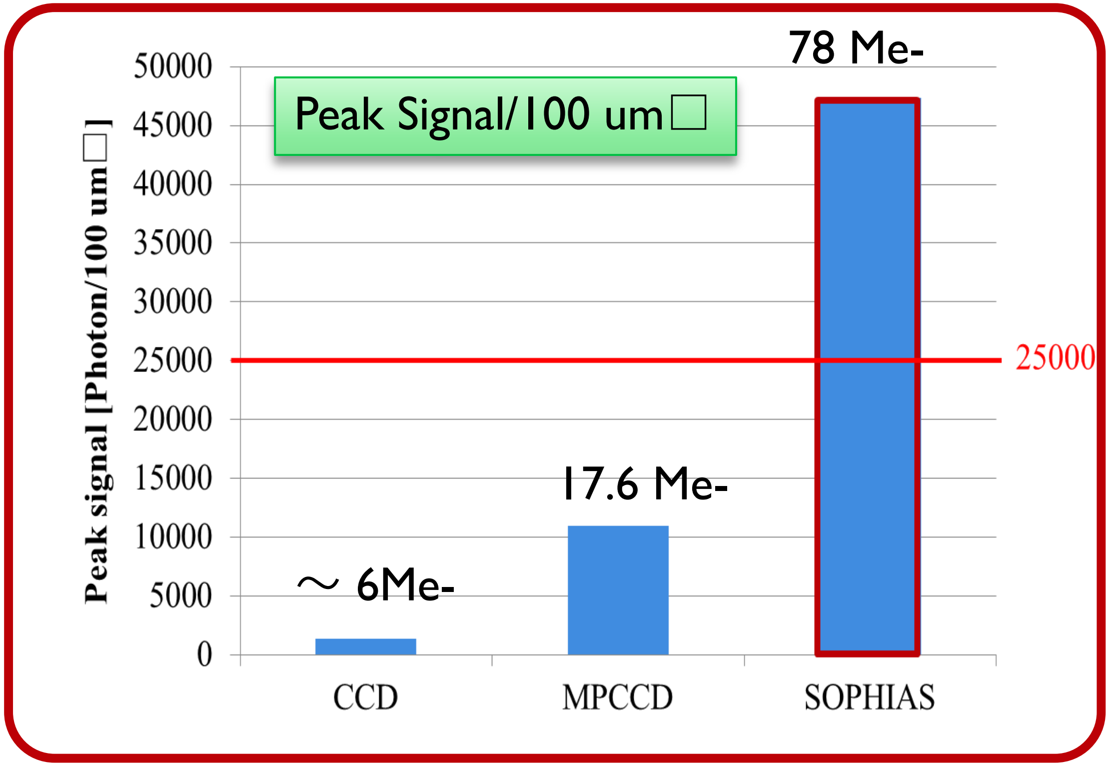
Current Status

- **Buried P-well proposed by KEK, and now extensively used.**
- **FZ with > 3 kohm/cm**
- **Stitching**
  - **66 mm x 30 mm achieved**
  - **130 mm x 130 mm is possible**
- **4M to 5M, MIM Cap onto 3M**
- **1/f noise suppression by Source-tie and body-tie Tr.**
- **Simulation environment improvement.**
- **Currently upto 150 krad for Tr.**
  → SOPHIAS is for < 7 keV with back-illumination
- **Systematic study of the radiation damage has been started**
  - **Design Optimization by radiation damaged device models**
  - **New devices**

SOPHIAS

Silicon-On-Insulator Photon-Imaging Array Sensor
by using SOI Sensor Technology

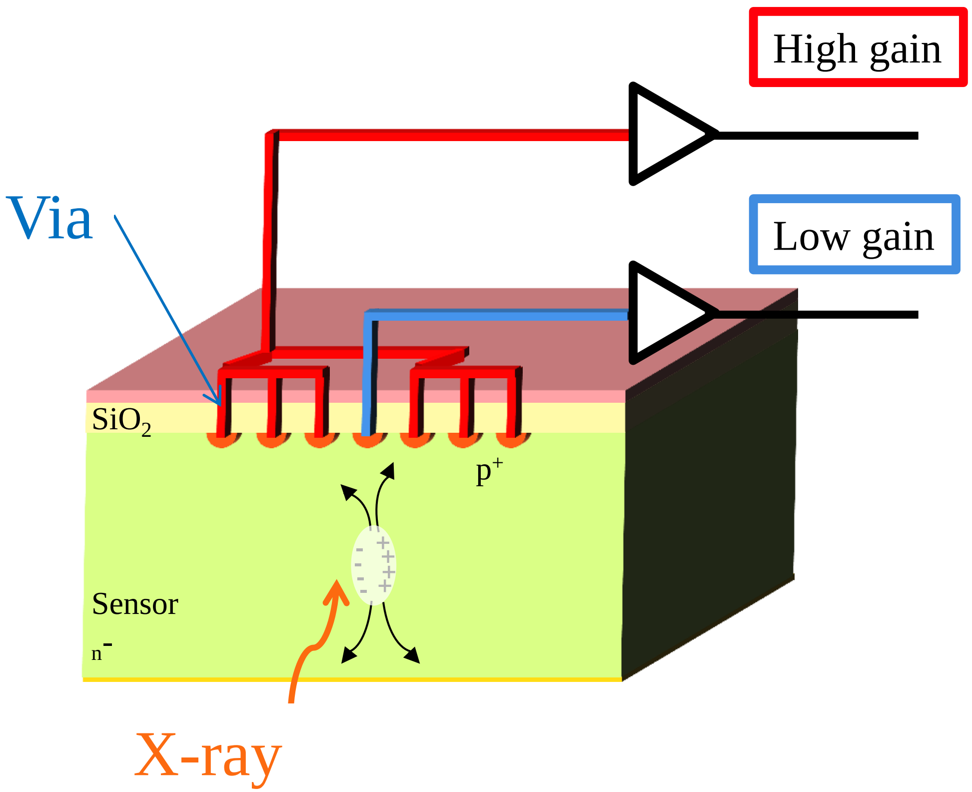
- *with A-R-Tec, ARKUS, and Tokyo Electron Devices, Kyocera*

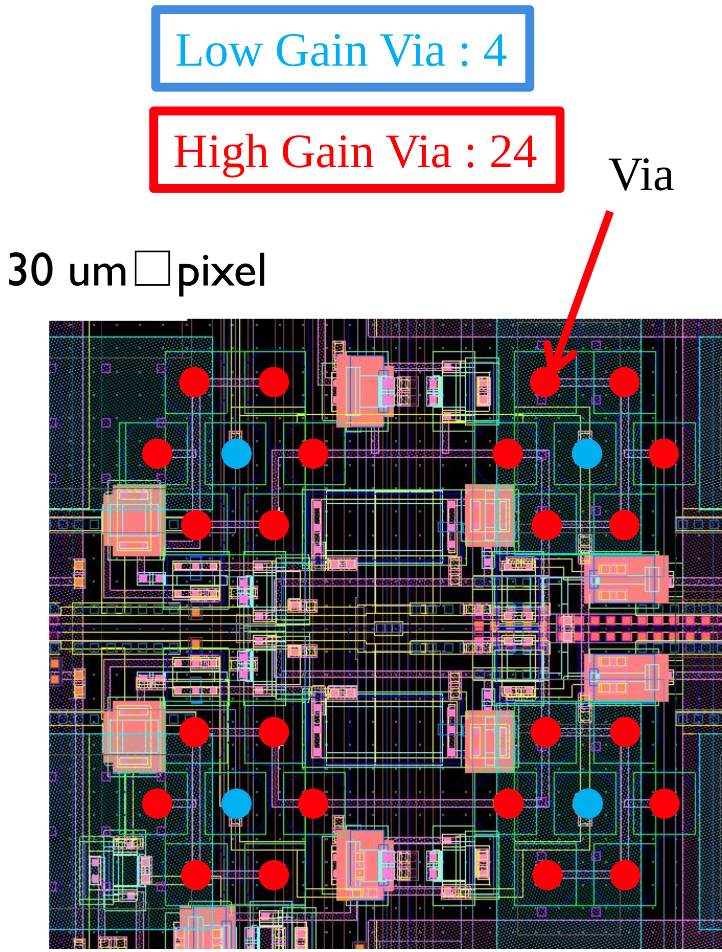


- Peak Signal 7 Me-
- Noise 100 e- (Effective 16.1 bit)
- Dual gain pixel
- 30 um□ pixel
- 1.9 M pixel/chip
- 60 frame/sec

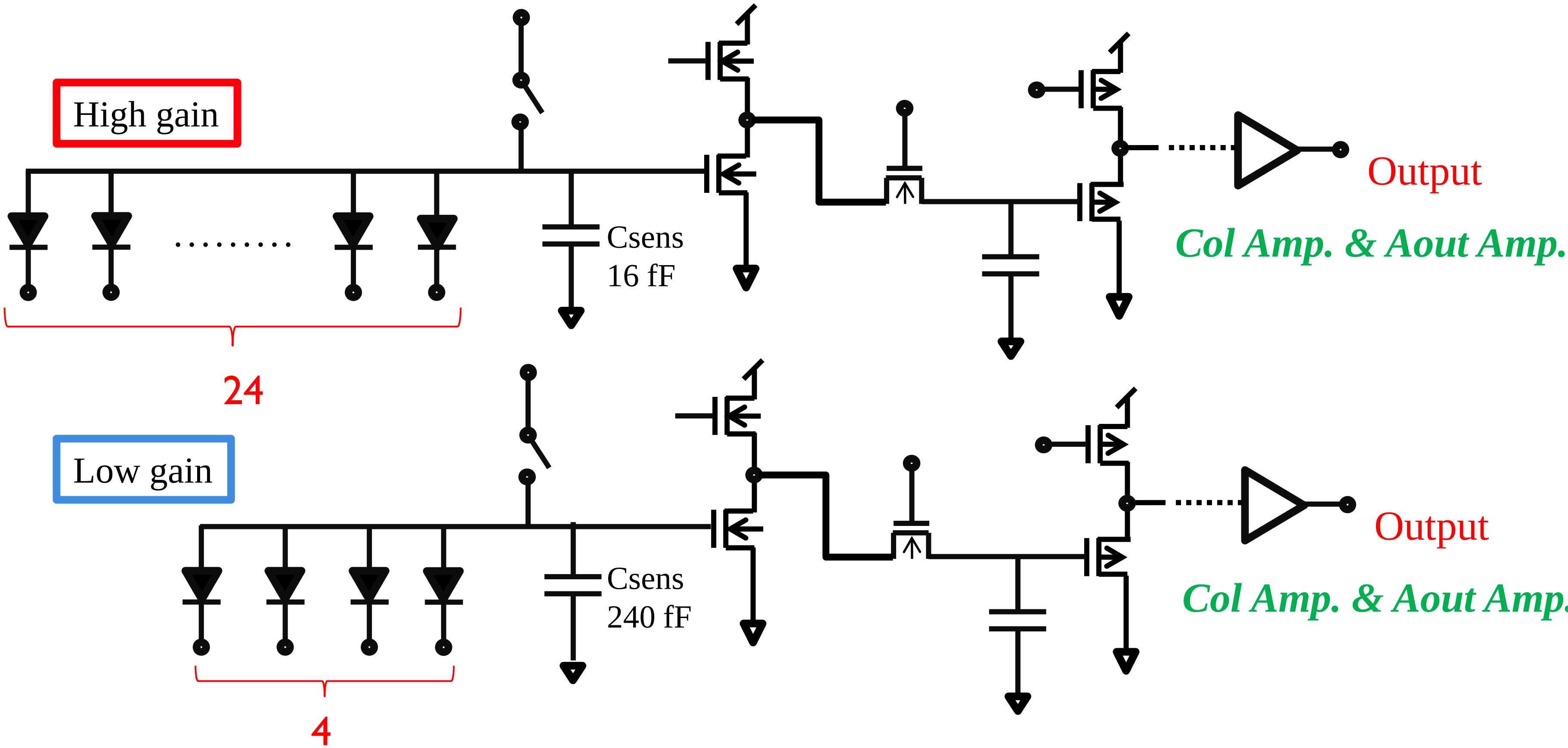
See Poster #25 for details: Omodani et.al.

SOPHIAS Pixel Layout by Multi-Via Concept





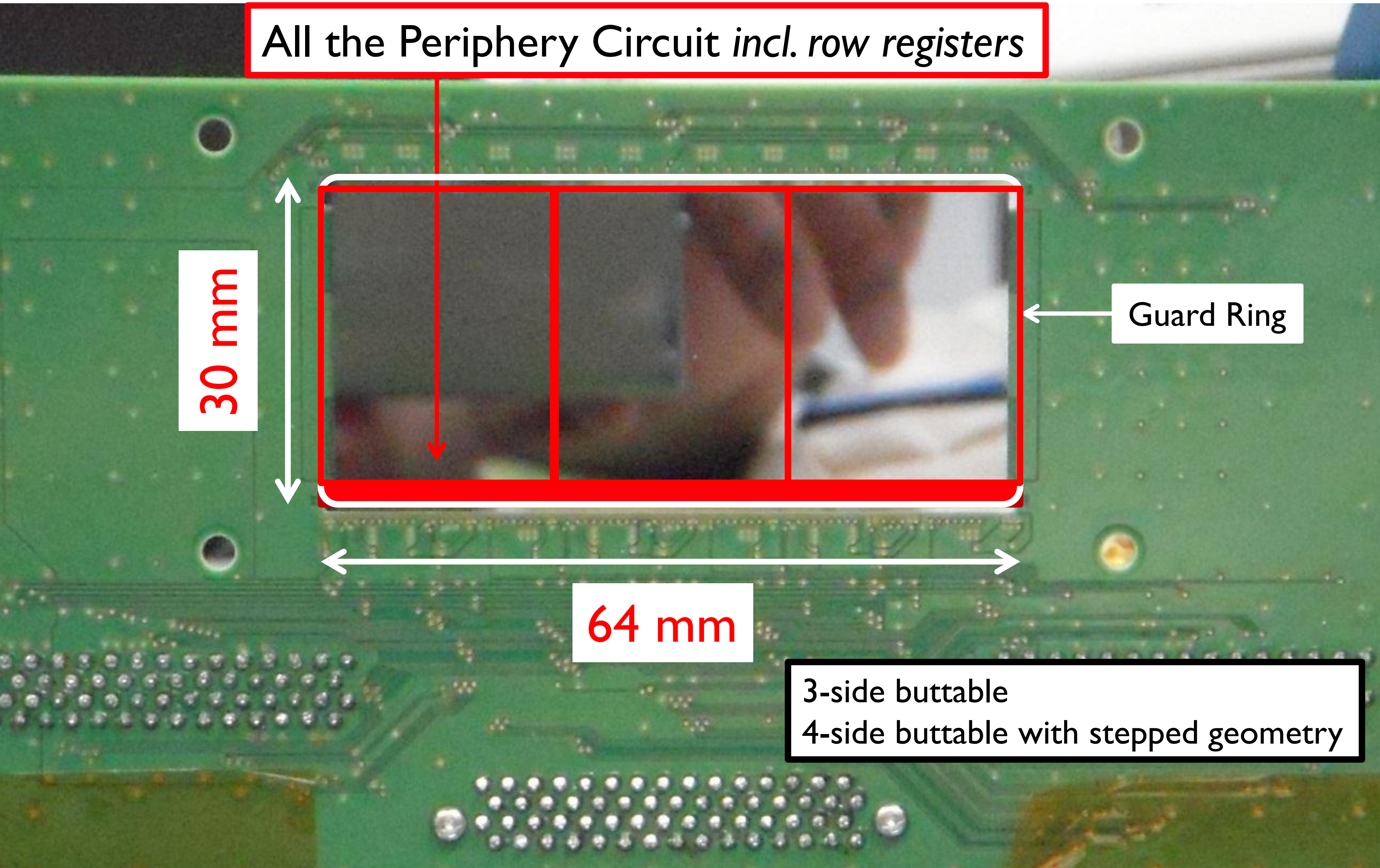
SOPHIAS
In-pixel Schematics

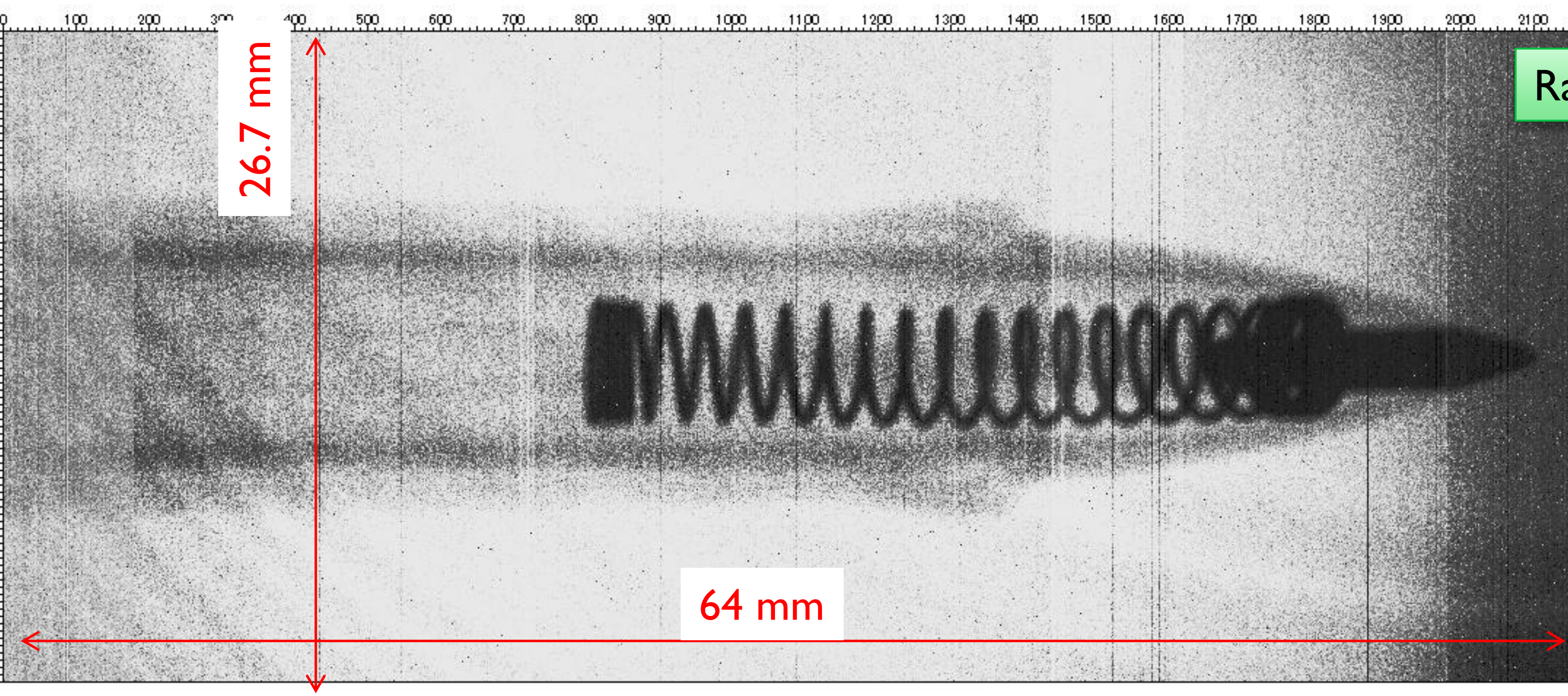


Gain	Csens [fF]	Via #	Gain [uV/e]
High	16	24	7.2
Low	240	4	0.15

x48

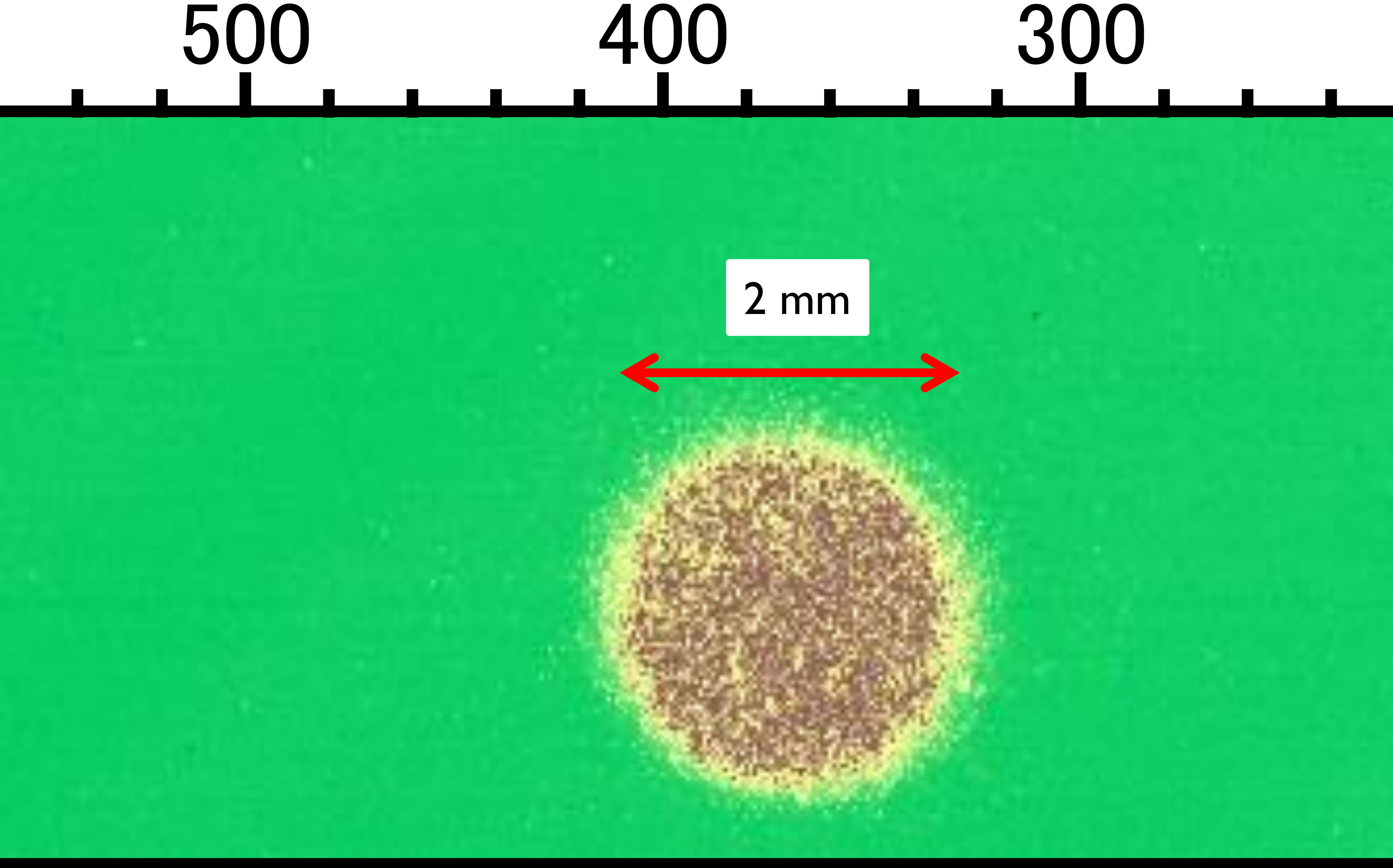
SOIPHIAS Sensor



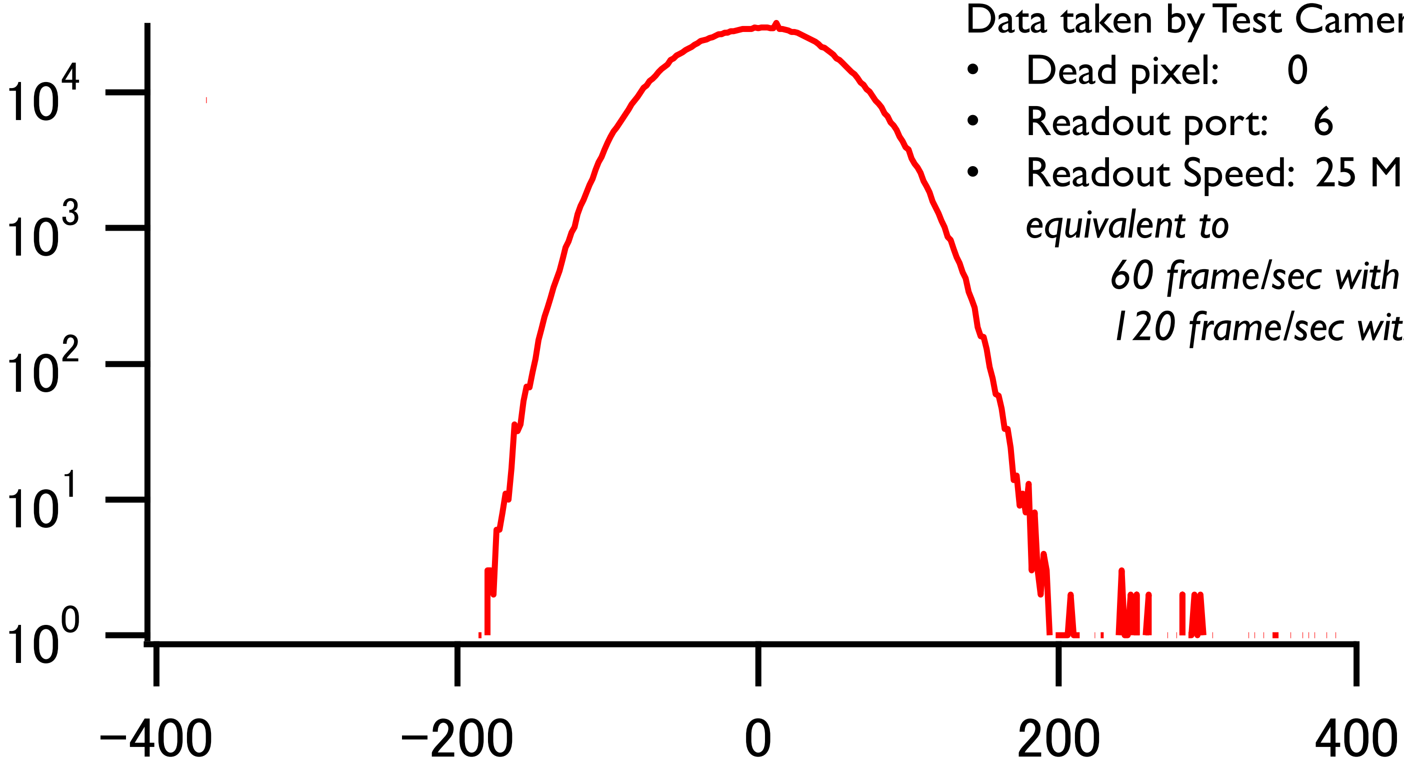


25 msec Exposure Ag 20 kV 0.2 mA

X-ray Image



1st Submission of Full Sensor Chip Offset Variation



Data taken by Test Camera
- Dead pixel: 0
- Readout port: 6
- Readout Speed: 25 MHz/pixel

  equivalent to

  60 frame/sec with off-chip Digital CDS

  120 frame/sec without off-chip digital CDS

Dead Pixel: None
Defect Pixel defined as offset > 200 meV
ratio 2.7 x 10^-5
53 pixels /1.9 Mpixel

Deployment Schedule of SOPHIAS

Dual-Sensor Detector

- Deploy to user operation in 2014
- Sensor capable of 60 frame/sec, but limited to 30 frame/sec due to Cameralink Interface bandwidth
- 3.8 Mpixel

Multi-Sensor Detector

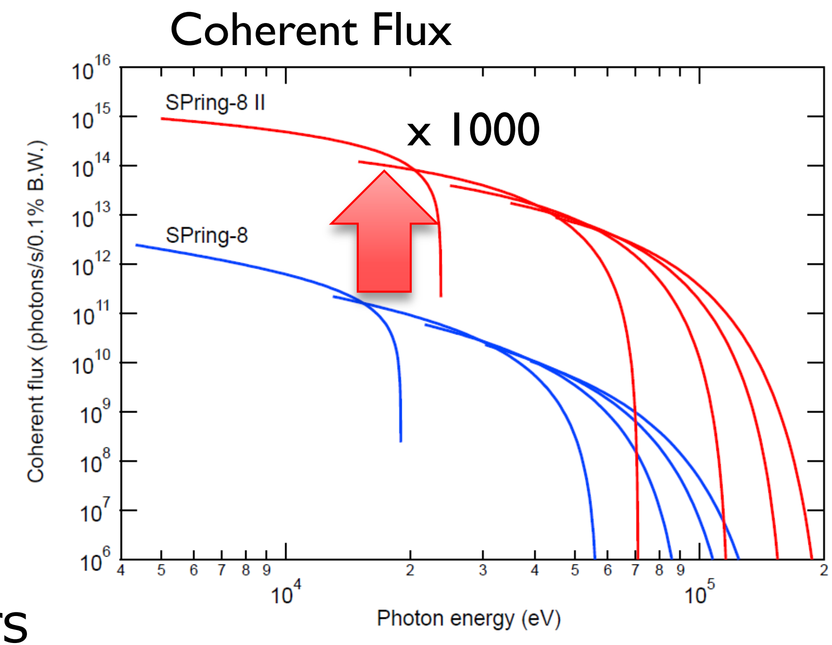
- Release target TBD
- 60 frame/sec
- max 80 Mpixel
- with E/O, calibration FPGA, and CLHS

Future Applications

- SPring-8 II
  - Coherent flux of source
    - x 1000 in 10 keV region

      More flux increase

      at sample position
  - A Target Candidate
    - X-ray Photon Correlation Spectroscopy (XPCS) in nanosecond regime
  - Provisional Demands for Detectors
    - Data frame acquisition at 23.6 nsec interval, *(or 1.966 nsec interval at best) in burst mode*



- Medical Applications
  - In collab. with Lapis Semiconductor and Rohm group.

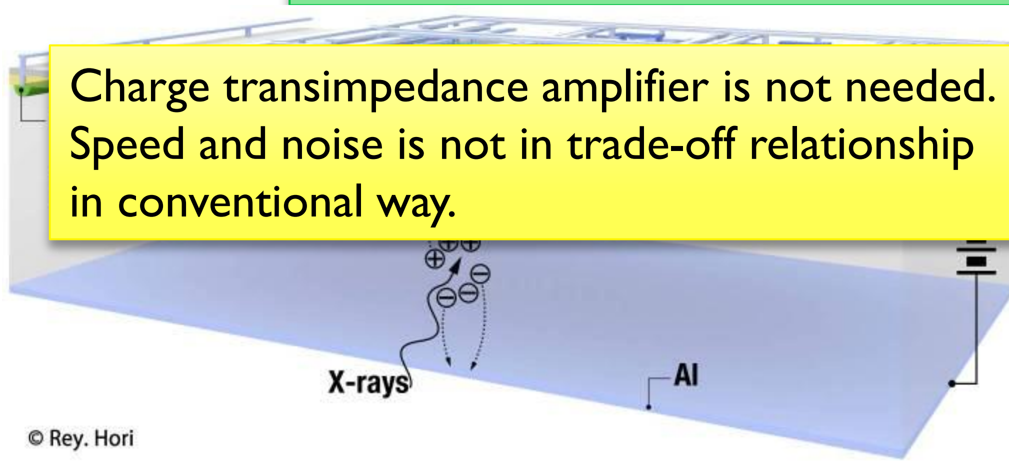
SOI Pixel Detector
Monolithic Si Pixel Sensor with VLSI
Collaboration of KEK, and Lapis Semiconductor, and other institutions

Advantages Summarized by KEK

- Bonded wafer → Thick High Resistivity Sensor + CMOS
- Monolithic Detector → High Density, Low material
- Standard CMOS → Complex functions in a pixel
- No mechanical bump bonding
  → High yield, Low cost
- Small input capacitance
  → ~10fF, High conversion gain, Low noise
- Based on Industrial standard technology
  → Cost benefit and Scalability
- No Latch Up, Low SEE
- Low Power
- Operate in wide temperature
  (4-570K) range.

Control of charge collection
SOPHIAS

Sample Hold Electronics
With 20 ENC at close to GHz rate

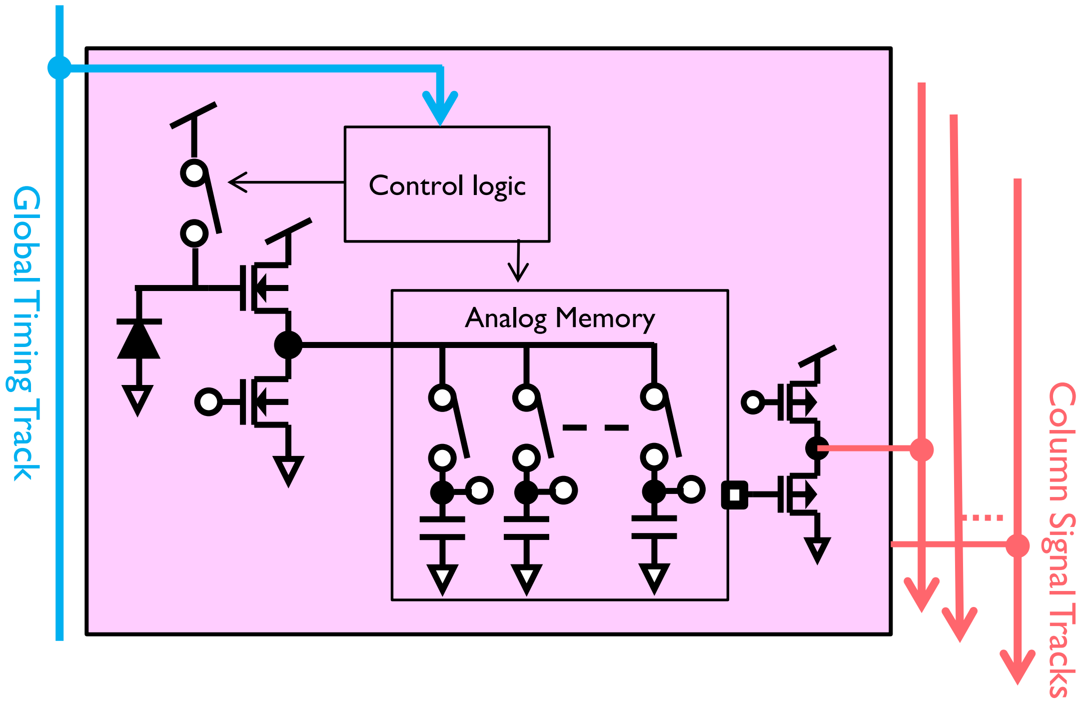


Charge transimpedance amplifier is not needed.
Speed and noise is not in trade-off relationship
in conventional way.

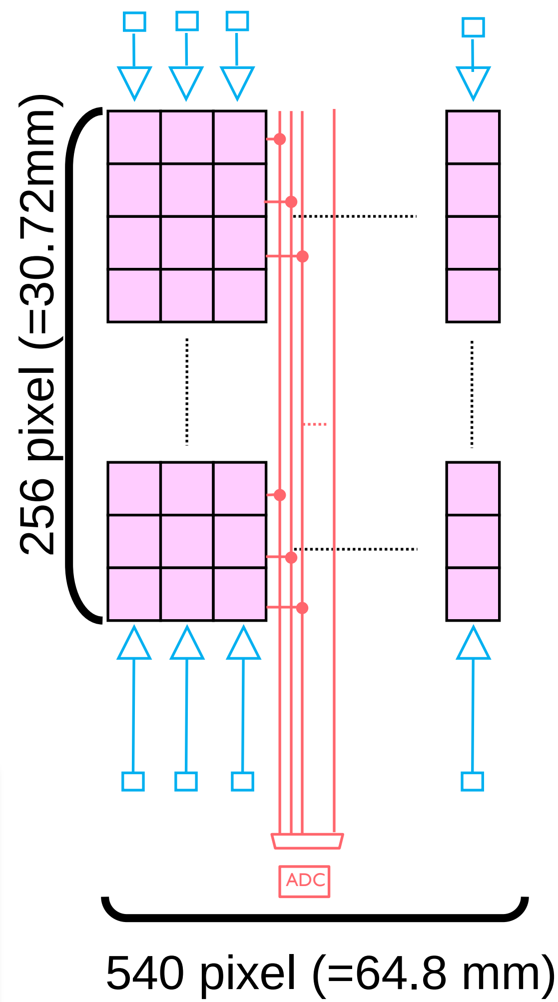
RIKEN joined SOIPIX collaboration
from the end of 2007

Preliminary Functional Blocks

Assumed Parameter:
120 um□ pixel, 10 bit ADC, Analog: noise 50 e- Peak 100 ke-



Global Timing Track from upper and lower pads
→ timing delay < 1nsc
Design optimization should be carried out.



Technology for **1 nsec framing** will be in our hand.
Readout remain in 10-100 kframe/sec.
Exposure/readout ratio is low.

- Optimized operation
- Off-pixel processing
  - Integrate new technology, such as 3D integration for higher readout rate

Summary

MPCCD *under deployment*

- Large Peak Signal of 4.4 Me- achieved.
- Upgrade with Deep 300 um CCD process has started

SOI Sensor Technology

- Ramping up to real (hard) X-ray applications.
- For SR &XFEL, limited up to 7 keV due to rad. hardness

SOPHIAS

- Peak Signal 7 Me-, Noise 100 e-, Dual gain pixel, 30 um□ pixel, 1.9 M pixel/chip
- To be deployed in 2014 with 3.8 M pixels
- Major tasks
  - Pixel-by-pixel Calibration

See Poster #25 for details: Omodani et.al.

After SOPHIAS

- Low input capacitance
  - Fast shutter in the nanosecond regime