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VELOPix ASIC development for LHCb VELO Upgrade

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The upgrade of the LHCb experiment, planned for 2018, will transform the readout of the entire experiment to a triggerless system operating at 40 MHz. All data reduction algorithms will be run in a high level software farm, and will have access to event information from all subdetectors. This approach will give great power and flexibility in accessing the physics channels of interest in the future, in particular the identification of flavour tagged events with displaced vertices. The data acquisition and front end electronics systems require significant modification to cope with the enormous throughput of data. For the silicon vertex locator (VELO) a dedicated development is underway for a new ASIC, VELOPix, which will be a derivative of the Timepix/Medipix family of chips. The chip will be radiation hard and be able to cope with pixel hit rates of above 500 MHz, highly non-uniformly distributed over the ˜2 cmˆ2 chip area. The chip will incorporate local intelligence in the pixels for time-over-threshold measurements, time-stamping and sparse readout. It must in addition be low power, radiation hard, and immune to single event upsets. In order to cope with the datarates and use the pixel area most effectively, an on-chip data compression scheme will integrated. This contribution will describe the requirements of the LHCb VELO upgrade, give an overview of the digital architecture being developed specifically for the readout chip, and describe the off-detector signal processing, including time ordering, clustering and pattern recognition algorithms. First results from prototype sensors and ASICs will be presented.

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