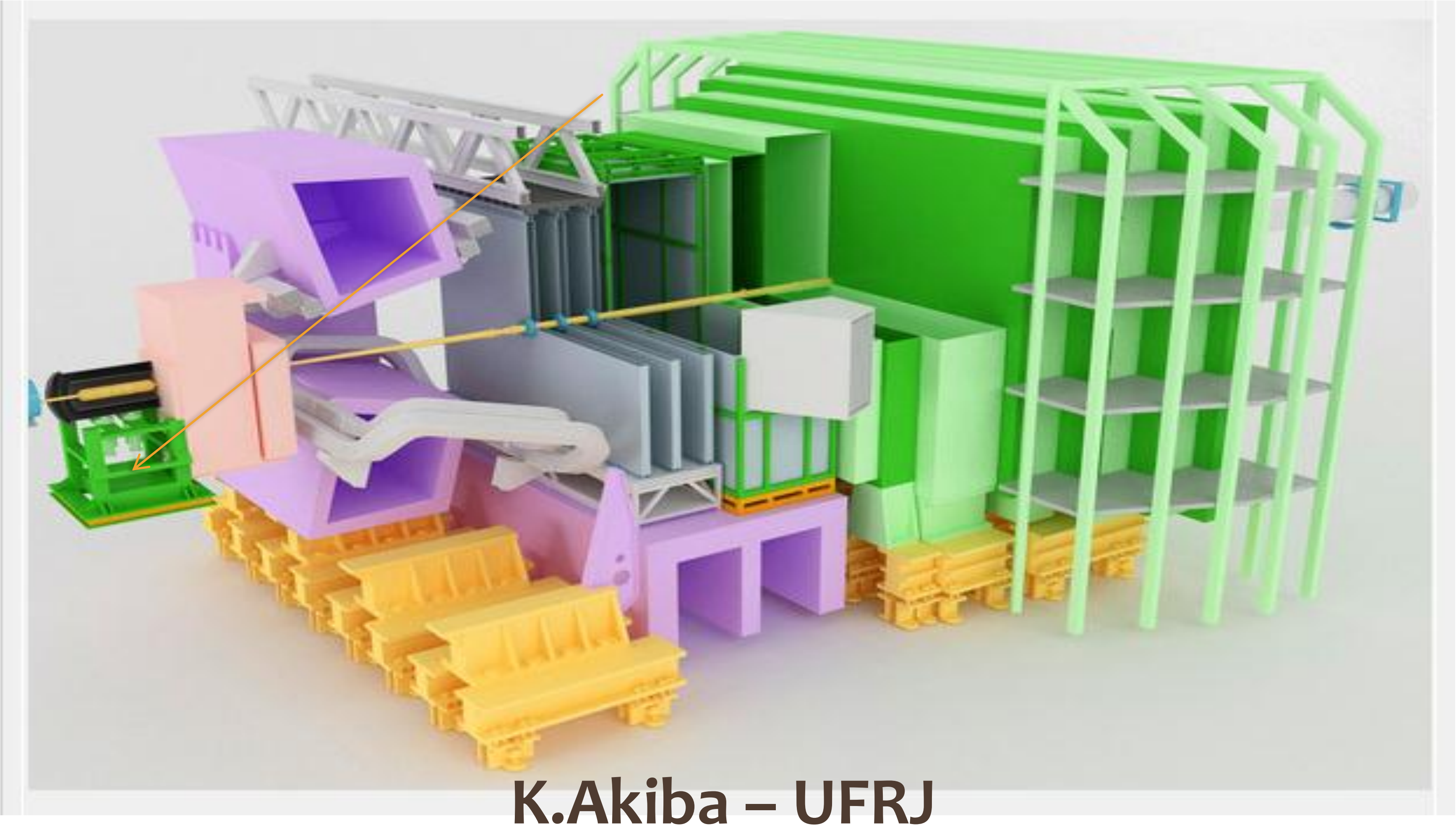
LHCb VELO Upgrade



K.Akiba – UFRJ

On behalf of the VELO Project

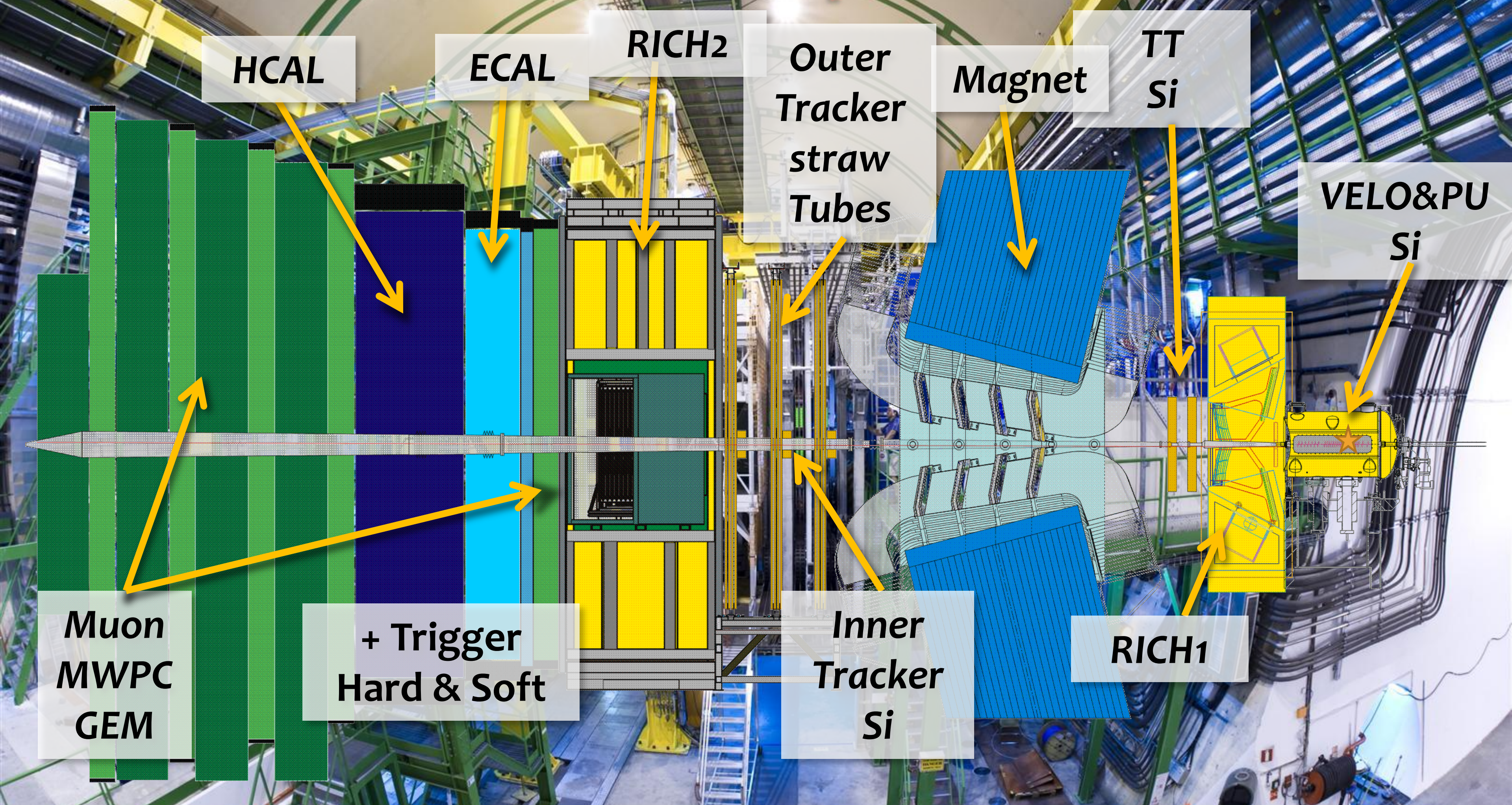
Outline

- Current detector overview
- Upgrade motivation
- VELO Upgrade plan
- Upgrade R&D
  - Sensors
  - ASIC
  - Cooling
  - Infrastructure
- Prototype evaluation
- Schedule
- Summary

The LHCb Experiment

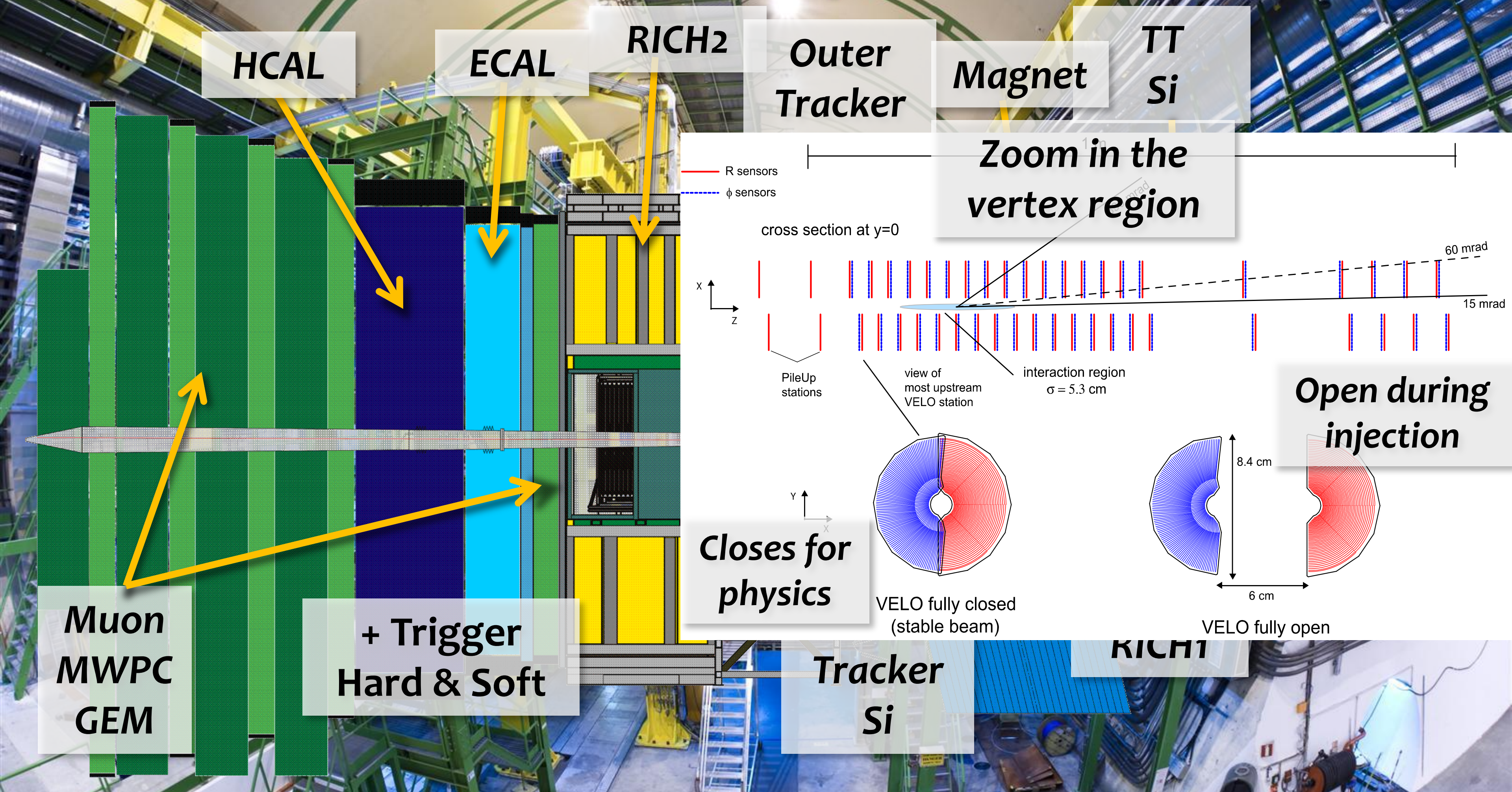
Large Hadron Collider beauty Experiment for CP violation and Rare B Decays.

The LHCb Experiment



Large Hadron Collider beauty Experiment for CP violation and Rare B Decays.

The LHCb Experiment



Large Hadron Collider beauty Experiment for CP violation and Rare B Decays.

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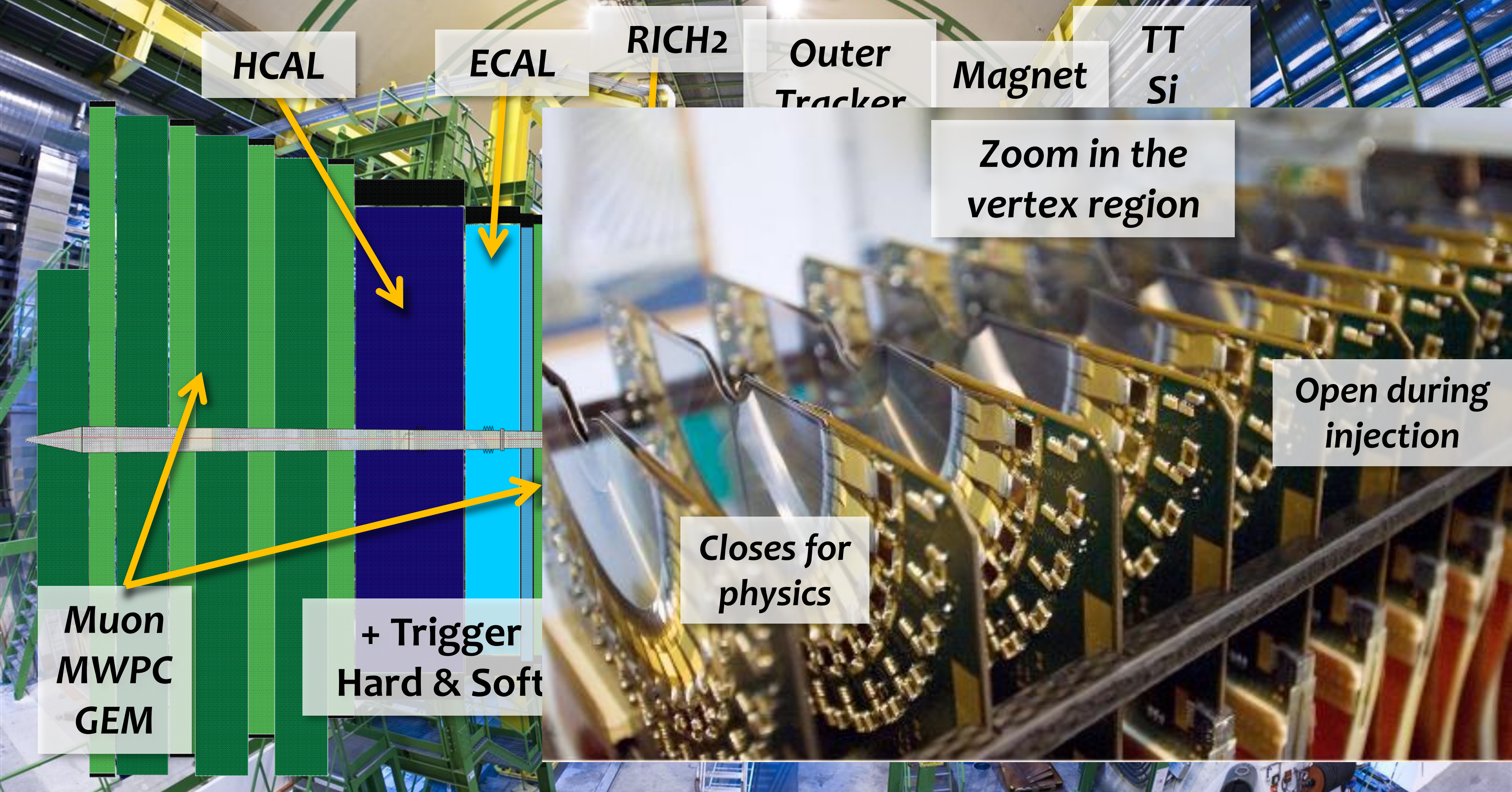
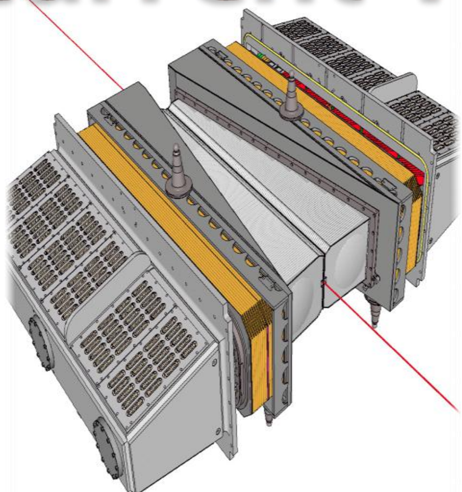
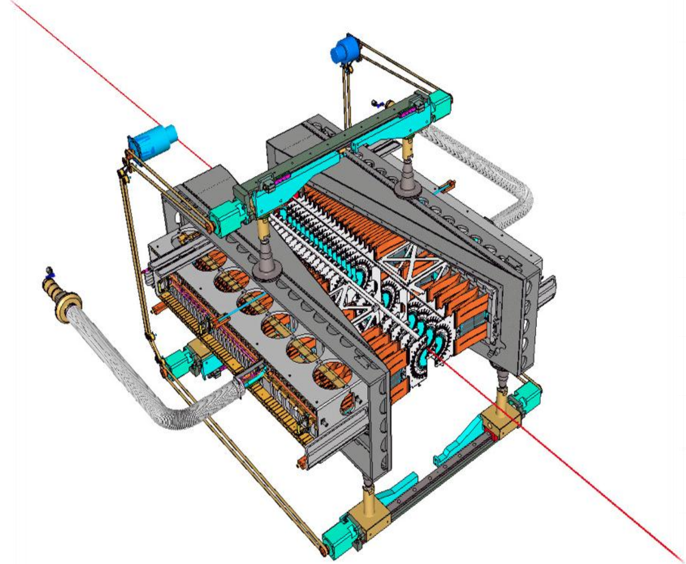


Large Hadron Collider beauty Experiment
for CP violation and Rare B Decays.

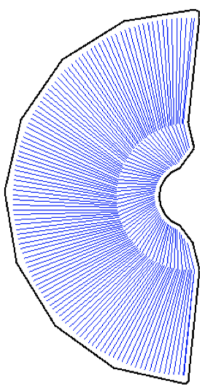
The current VELO



Operates in vacuum



Cooled by evaporative **CO_2** system



88 silicon sensors

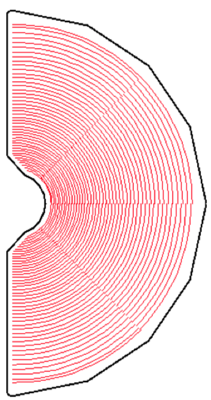
R-φ design

300 μm, n^+n Si

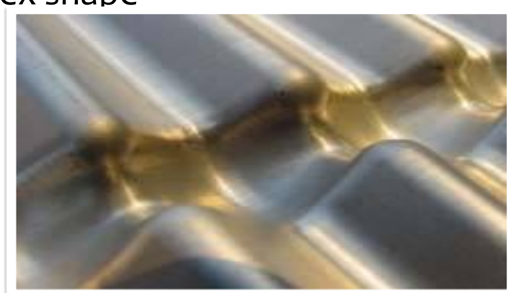
2048 strips

r_{active} = 8.2mm

$pitch_{min}$ = 40 μm



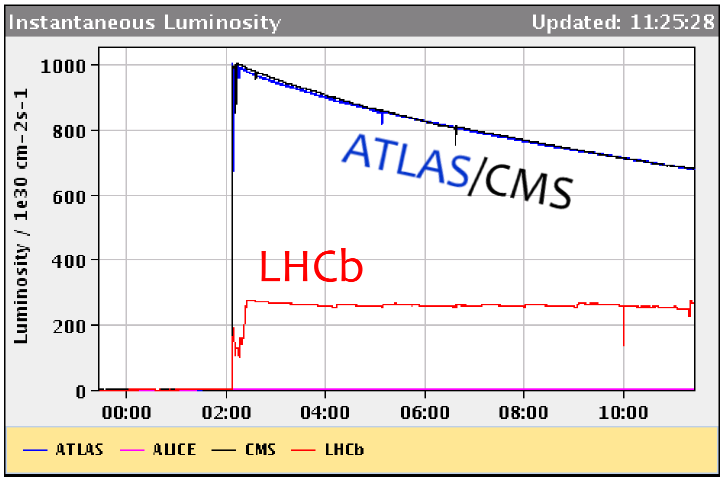
Separated from primary vacuum by RF foil with complex shape

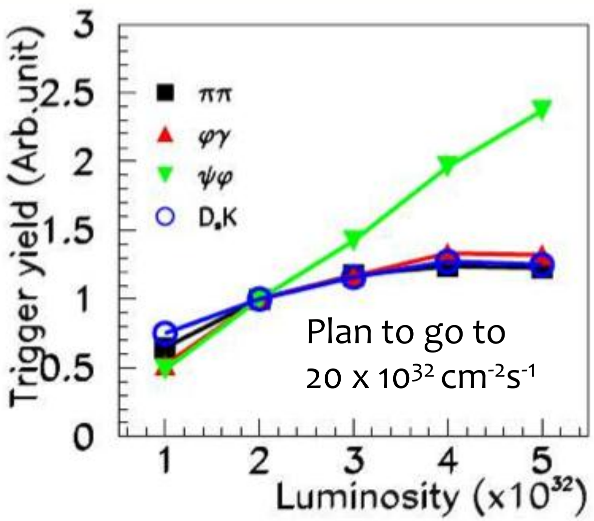


Moves away every fill and
centers around the beam with self measured vertices

Why upgrade LHCb

- Currently LHCb design can cope with inst. Lumi. $L > 2L_{design}$
  - LHC still provides more than what we can handle:

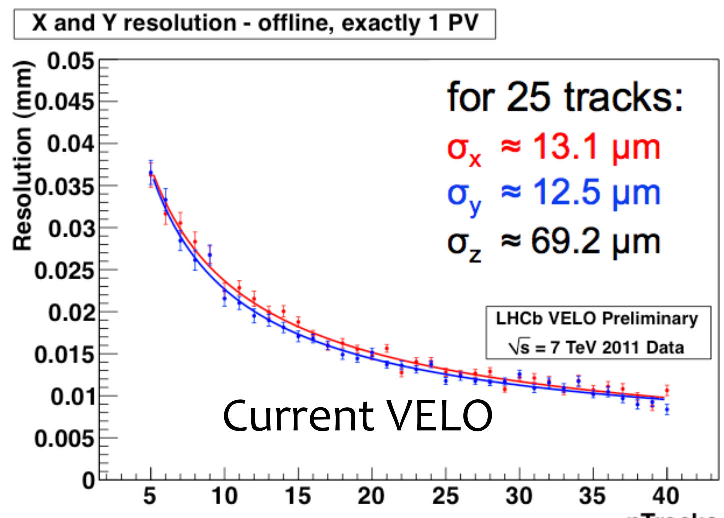




  - Current detector is limited due to 1 MHz readout.
  - Higher Luminosities do not translate to higher yields many (hadronic) channels.
- The upgrade is planned as a major Trigger/Readout upgrade:
  - From 1 to 40 MHz full readout ➔ Every collision read out to a computing farm
  - Higher instantaneous Luminosity ➔ Higher occupancies

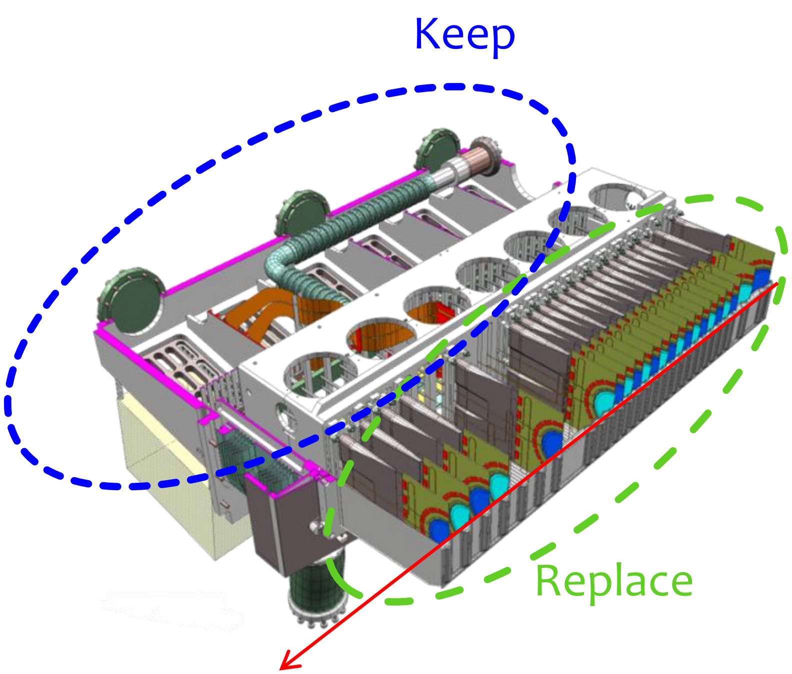
Main Challenges for the Upgrade: Operation@ 40 MHz & 2 x 10^{33} $cm^{-2}s^{-1}$

- Completely new front-end electronics and sensor
  - Fast Analogue front-end
  - Able to withstand radiation levels of ~ 370 MRad or 8 x 10^{15} n_{eq}/cm^2 (5 times bigger/year)
- Huge data rate in the front-end and back-end
  - Capable of dealing with huge data rate
- Completely new cooling interface
  - Thermal Runaway risk at inner most region
- Improve the excellent performance
  - Proper time resolution ~ 50 fs
  - IP resolution ~ 13 + 25/pT µm



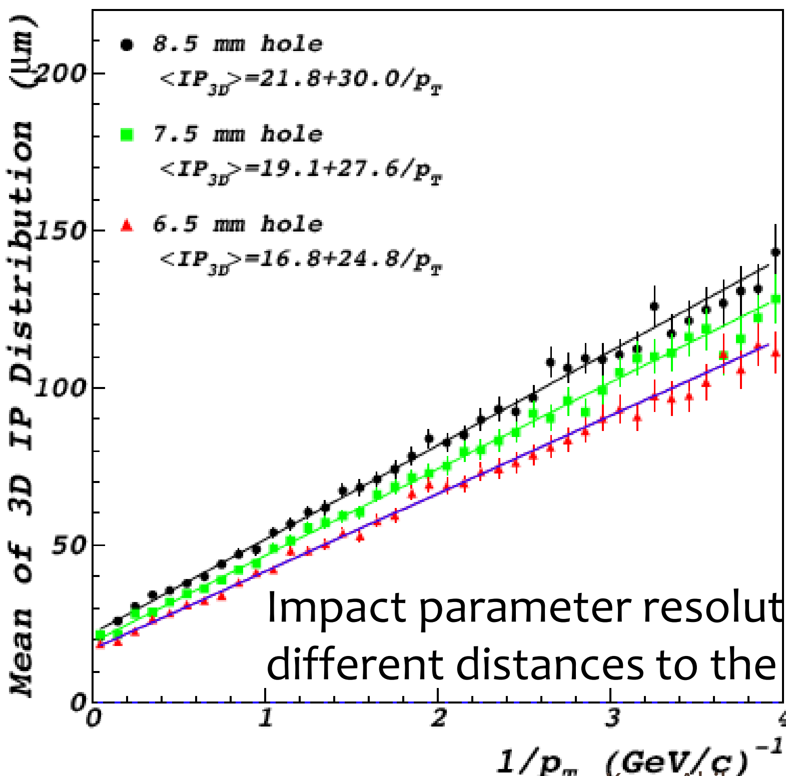
Upgrade plan

- Keep the common infrastructure of the VELO:
  - Bi-phase CO_2 cooling
  - LV & HV power supply systems
  - Vacuum and Motion systems
- New components:
  - Detector modules
  - Readout ASICs
  - New design of lower material RF foil
  - Multi Gbps readout system



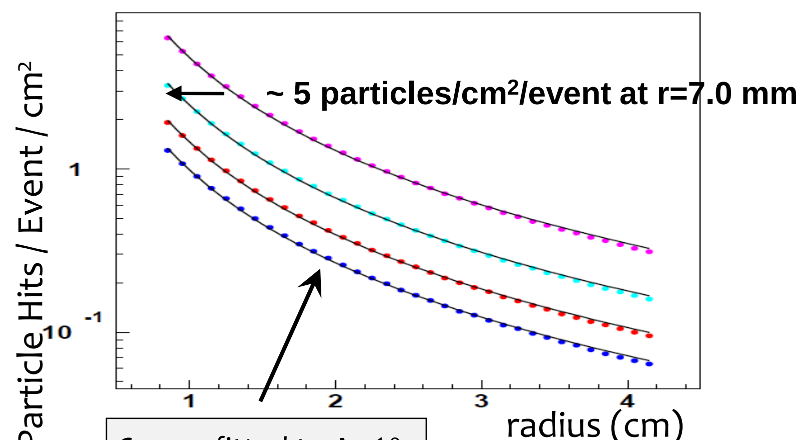
Design Considerations on the upgrade

- Intant Lumi 5 times higher:
  - much higher radiation damage.
  - Much larger bandwidth (up to 12 Gbps @ hottest pixel chip) and occupancies.
  - Needs fast robust, reliable, **pattern recognition**
- ***Material budget*** and ***distance*** to the collision point affect the ***IP resolution***.
- Two main design options to consider: ***Strips*** or ***Pixels***.



Impact parameter resolution for different distances to the beam axis

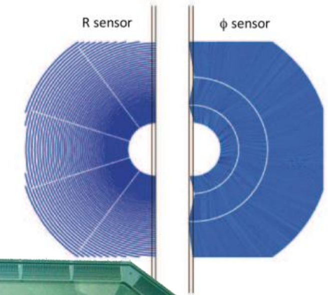
Particle occupancy per event (simulation)



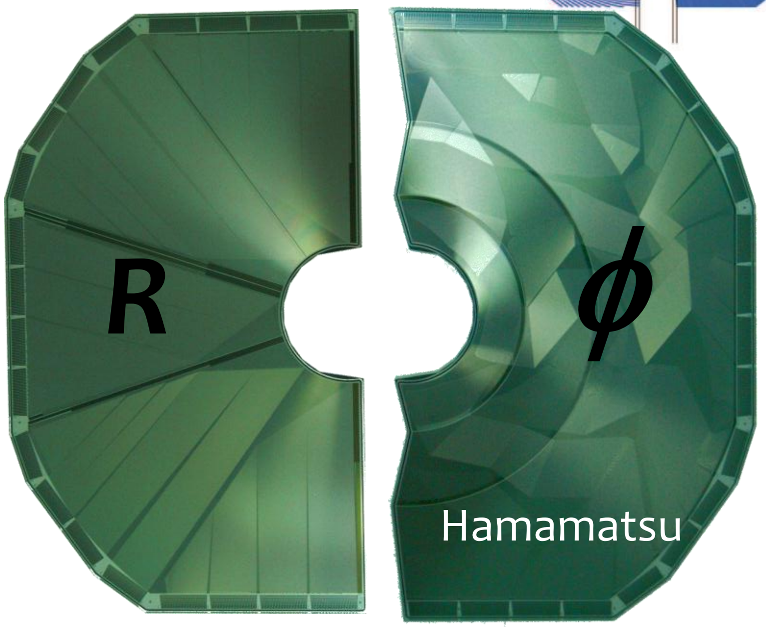
Curves fitted to $A.r^{-1.9}$

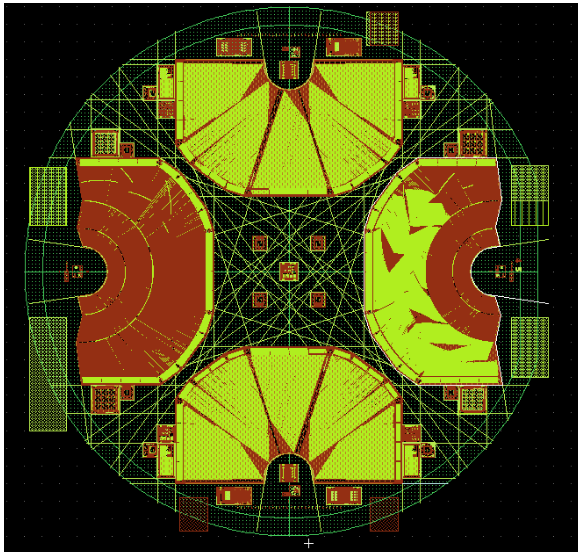
Luminosity ($cm^{-2}s^{-1}$)	2.10^{32} Current	5.10^{32}	**10.10^{32}**	20.10^{32}
A=	0.98	1.46	**2.46**	4.80

Strip Design



- similar to current detector (Rϕ geometry)
  - 30 μm minimum pitch, 20 x 128 strips per sensor
  - keep occupancies < 0.6 % at $10^{33} cm^{-2} s^{-1}$
  - Keep capacitances low ➔ higher lifetime
  - No pitch adapter (compared to now)
  - Sensitive area close to the edge
  - Active @ 7 mm from the beam
- Sensor prototypes (Hamamatsu) being tested
- Sensor hybrid to be developed
  - Cooling options shared with Pixel alternative.
- New ASIC chip under development:
  - on-chip common mode subtraction, clustering and zero suppression





Pixel design

- Will be built with VeloPix ASIC
  - Based on Timepix3 (TPX3) design ← successor of Timepix
  - Silicon Planar Sensors 55x55 μm pixel, 256^2 matrix

  ➔Telescope built with this tech. already has very good results: < 2 μm Resolution at the DUT.
  - simultaneous measurement of time-over-threshold (ToT) and time-of-arrival (ToA) ➔ ideal for time stamp and inter pixel positioning
  - Requirements: peaking time < 25 ns, timewalk < 25 ns @ 1ke$^-$
  - hit rate up to 500 MHz (hottest chip @ L = 2×10^{33} cm^{-2}s^{-1})
  - Super pixels and data driven read-out.
- Many sensor options being investigated.
- (more details on the chip in M.v. Beuzekom – Session 5)

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  - … m
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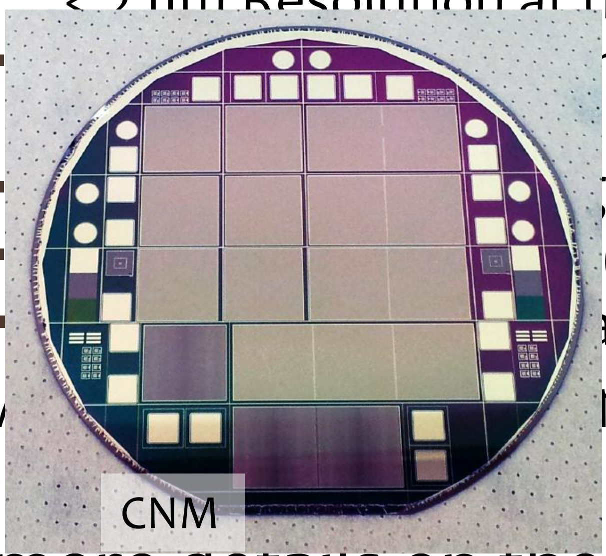
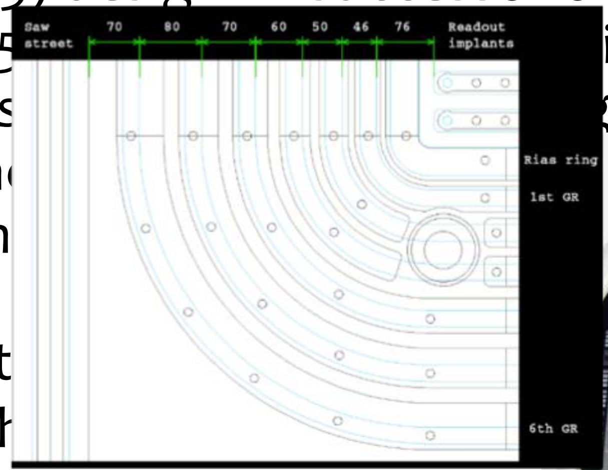
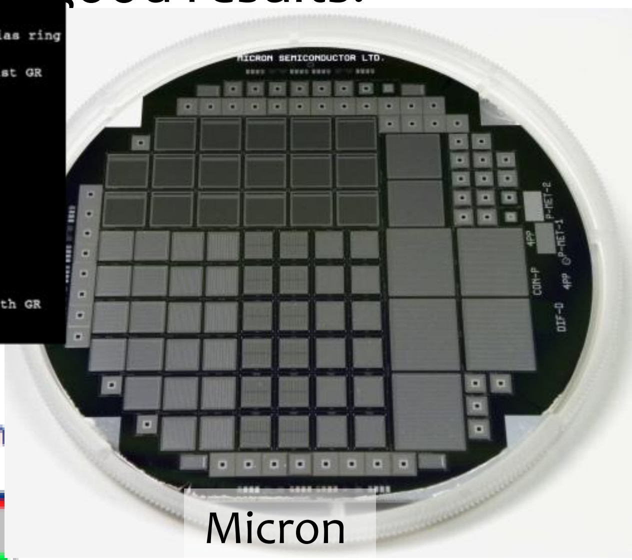
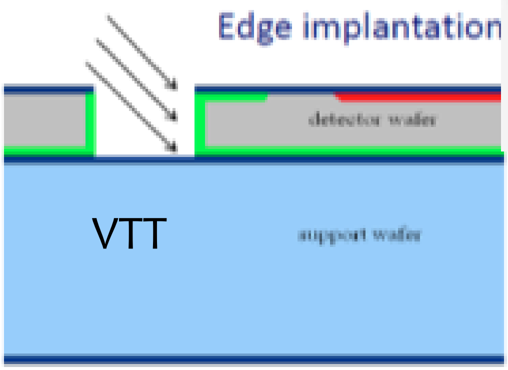
  - … a driven read-out.
- M … n





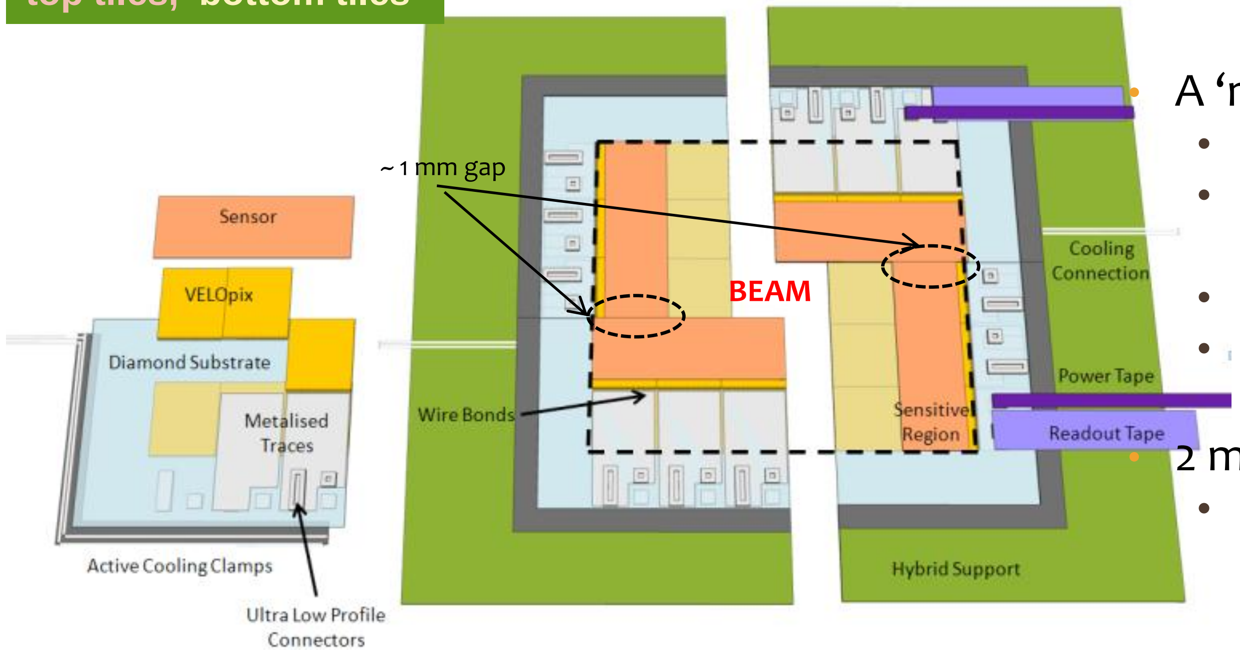




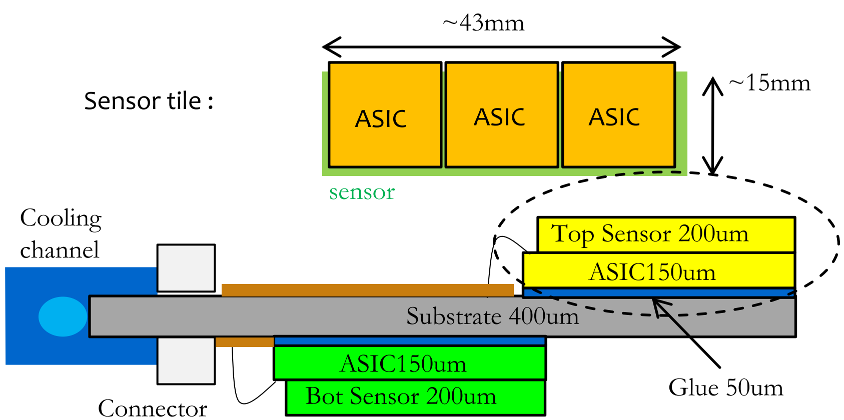
- (more details on the … ekom– Session 5)

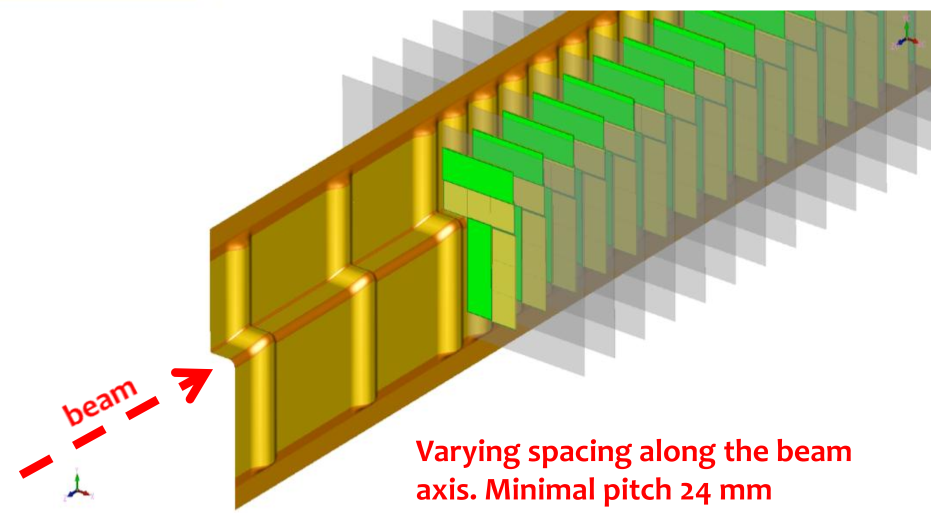
Pixel Module

top tiles, bottom tiles



- A 'module' is made of 4 sensor tiles.
  - active area ~100% (except small gaps)
  - Closest pixel is at 7.5 mm from the beam center
  - Each tile has 3 ASICs
  - 2 tiles on each side of the substrate
- 2 modules make 1 station
  - 26 stations in total

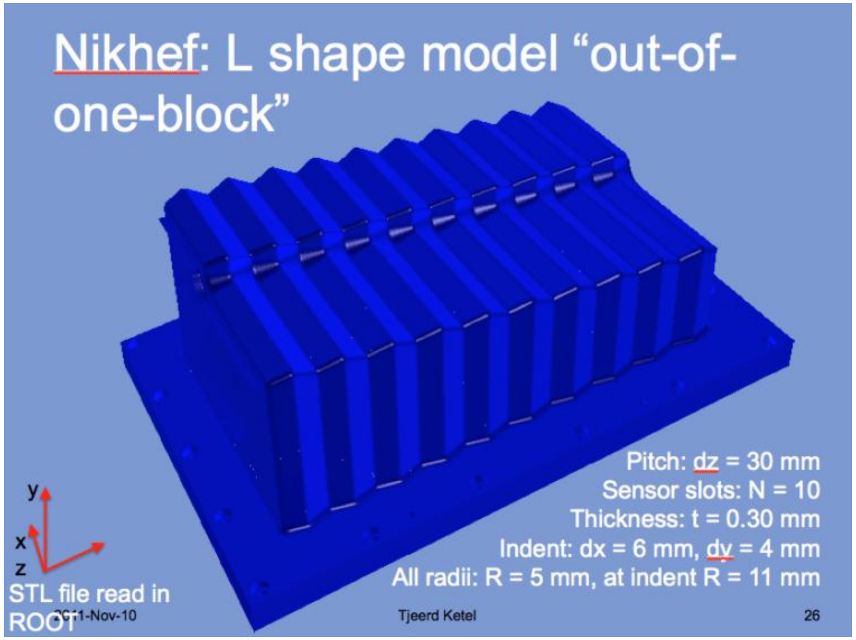


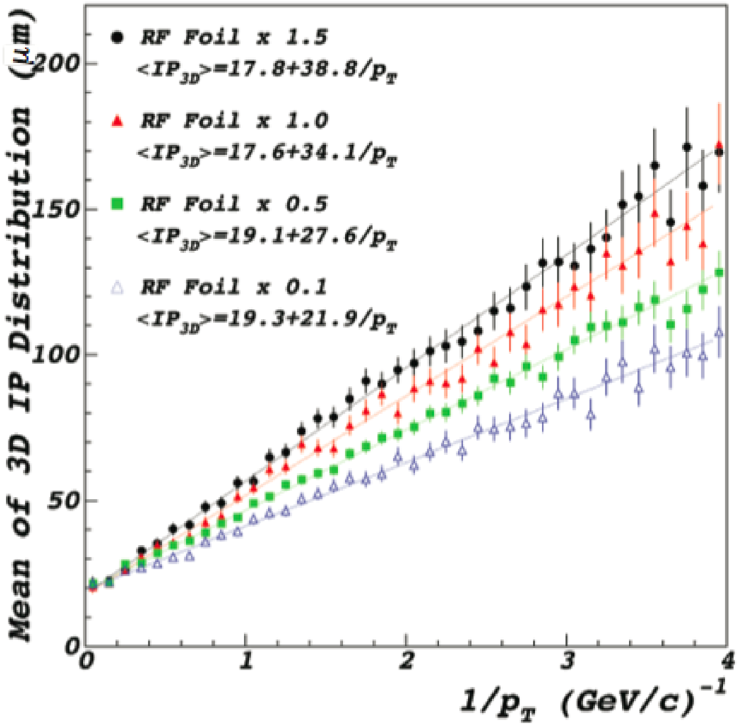


Varying spacing along the beam axis. Minimal pitch 24 mm

Upgrade RF Foil

- Requirements
  - Vacuum tight (< 10^{-9} mbar l/s)
  - Radiation hard
  - Low Mass
  - Good electrical conductivity
  - Thermally stable and conductive





- Material and fabrication:
  - Aluminium (AlMgMn): 200-350 μm thickness:
    - By 5-axis milling of a single homogeneous block

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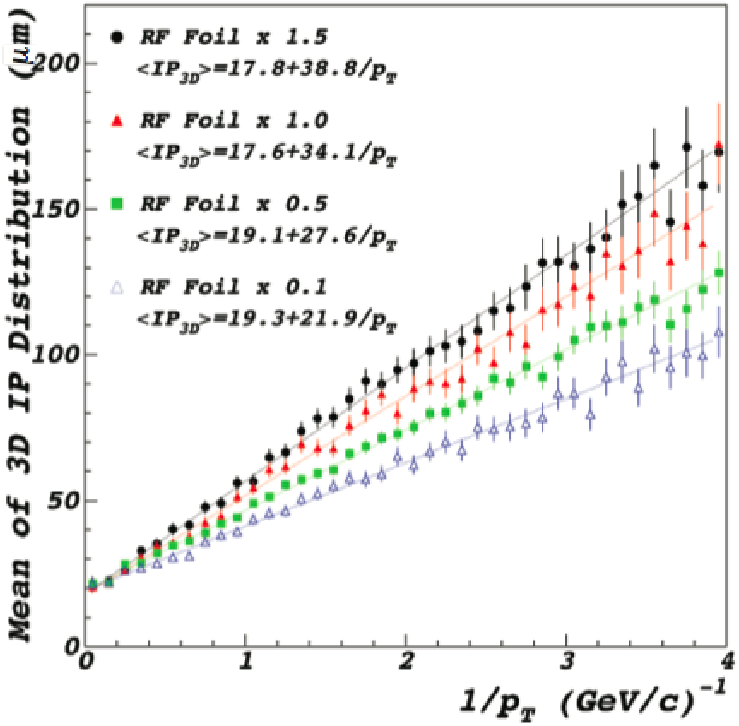

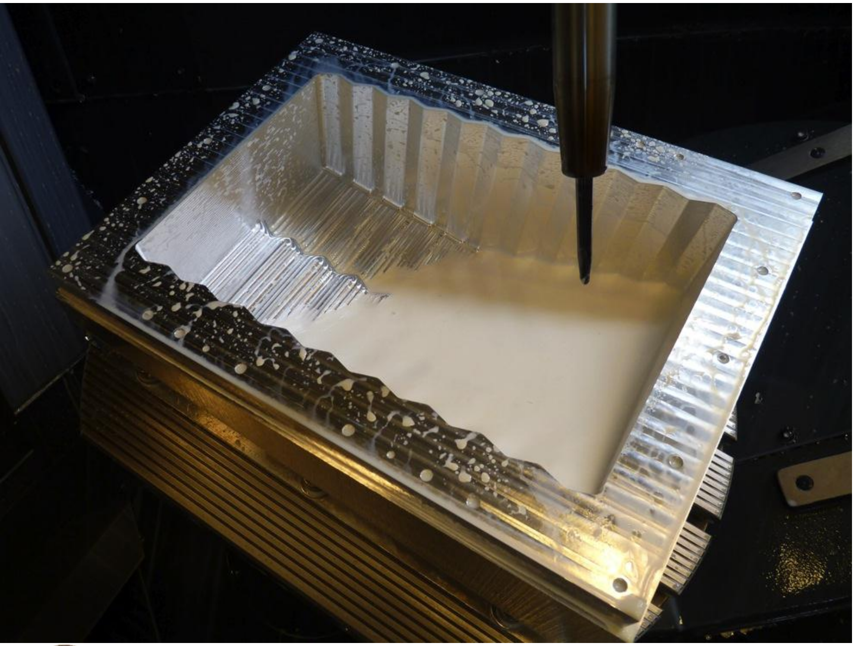

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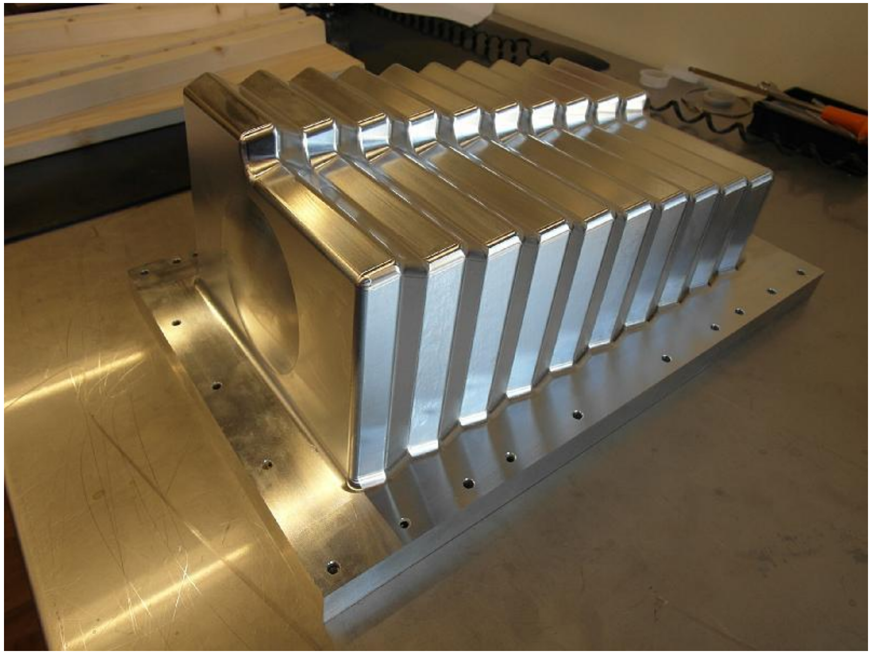

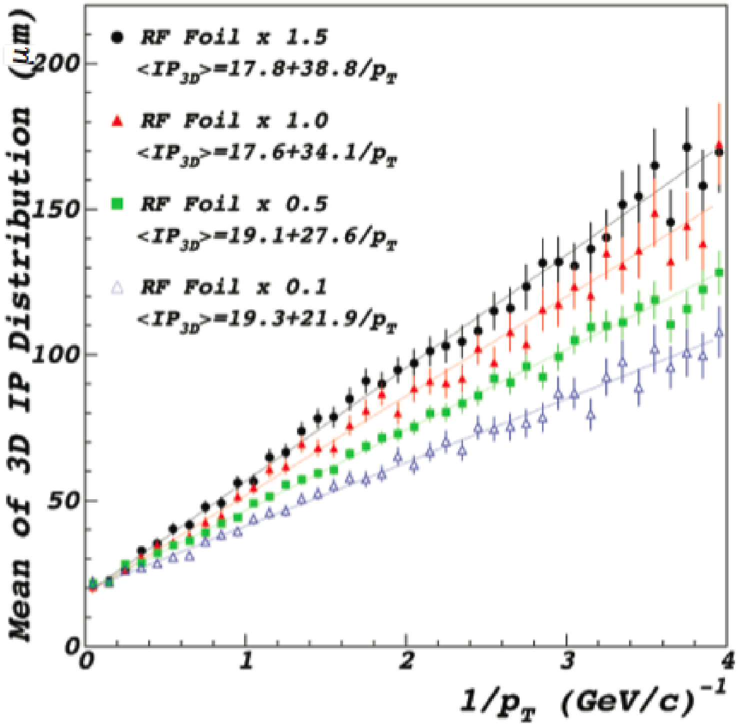

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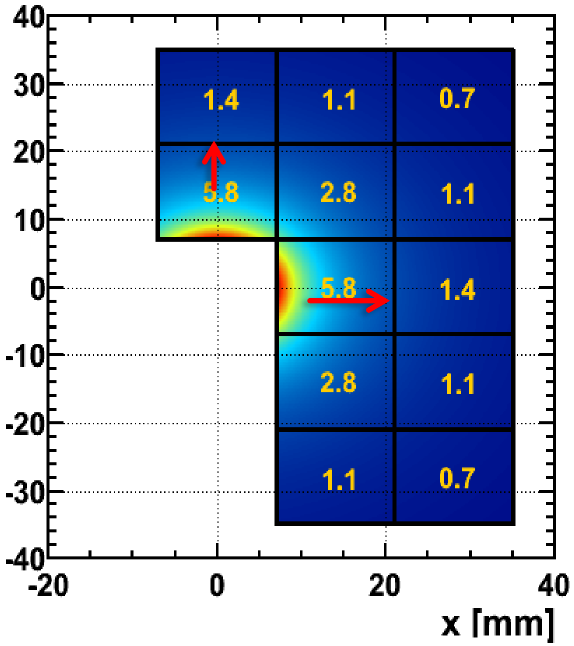
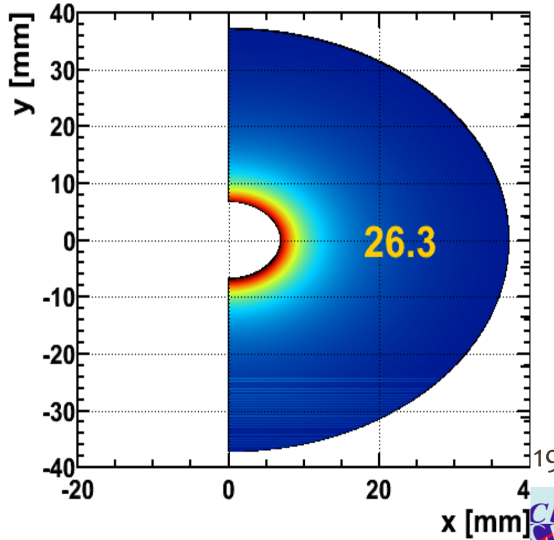
  - Aluminium (AlMgMn): 200-350 μm thickness:
    - By 5-axis milling of a single homogeneous block

Data Rate

- Occupancy is "low" but the detector is fully read every 25 ns.
  - Strips read out ZS data for each FE chip.
  - Strip design compensates occupancy with shorter strips.
  - Pixels summarize information from a 4x4 super pixel and time stamp the hits ➔ 30% reduction on the rate.
  - Intelligent column to readout data from hot to cold area
  - Huge data rate from the hottest parts.
    - 12 Gbps for inner most pixel chips
    - Hottest chip must cope with ~500 MHits/s.

Particle occupancies





- Back end electronics must cope with a huge amount of data:
  - TELL40 (upgrade of TELL1, current DAQ board) receives and builds events using FPGAs.
    - Has to wait for time stamped data from every chip.
  - All the information is assembled and passed on to computing farm, stripping down redundant data.
  - Further processing and full reconstruction in the trigger farm.

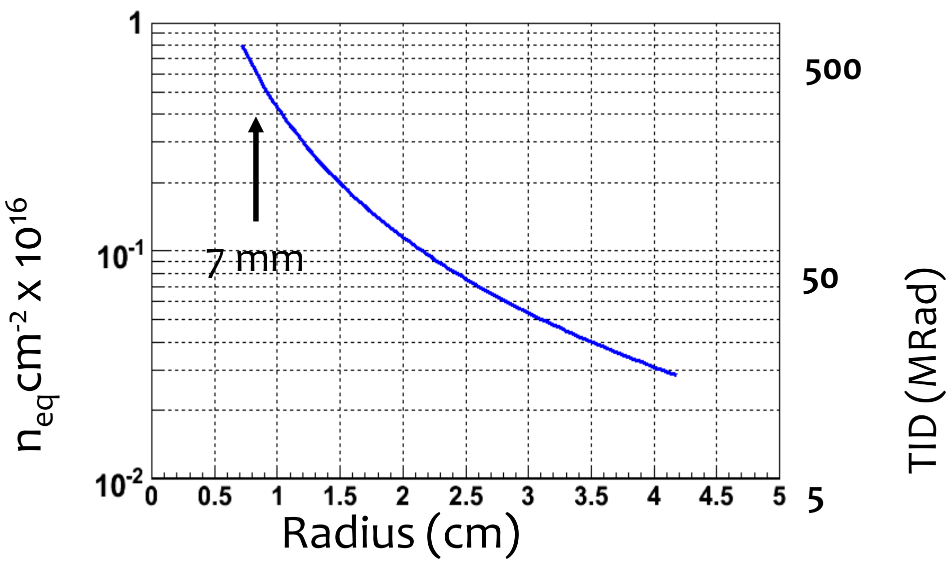
Pixels Vs Strips

	strips	pixels
# ASICS/half station	40	12
# half stations	42	52
# ASICS total	1680	624
Cluster size	1.6	2.2
# clusters / half station/ 25 ns.	52.6	25.8
# pixel(strips) hits / half station /25ns.	84.2	56.8
# bits / cluster	42.4	52.3
# bits / pixel(strip) hit	26.5	23.8
Hottest chip output rate	1.4 Gbit/s	12.2 Gbit/s
Coldest chip output rate	1.4 Gbit/s	1.5 Gbit/s
Data rate / half station	56 Gbit/s	54.3 Gbit/s
Total data rate	2352 Gbit/s	2823 Gbit/s

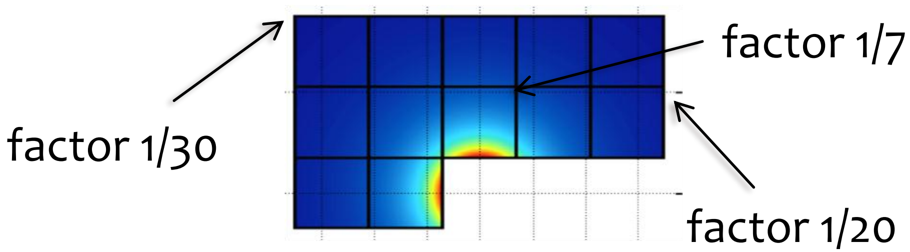
High and Uneven Radiation damage

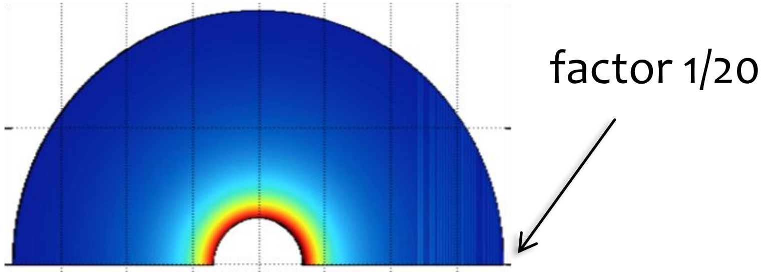
- At 7 mm from beam we accumulate ~ 370 MRad or 8 x 10^{15} n_{eq}/cm^2 for 100 fb^{-1}
- Irradiated areas require higher depletion voltage.
- Cooling must reach inner areas to avoid thermal runaway

Dose after 100 fb^{-1}



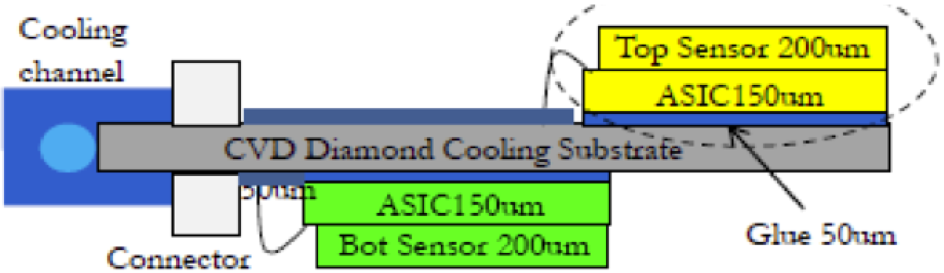
Dose is highly non-uniform – could pose a challenge, particularly for large sensors



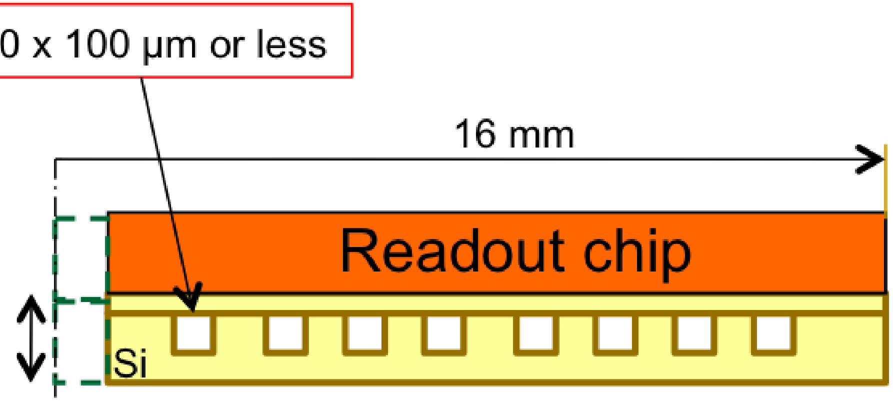


Cooling options

- Plan to use radiation hard CO2 evaporative cooling
- The main studies lie on the substrate and delivery options:
- CVD diamond and/or Thermal Pyrolithic Graphite (TPG) Substrate
- Micro channel (promising, more on J. Buytaert's talk- session 7)



CVD



Micro channel

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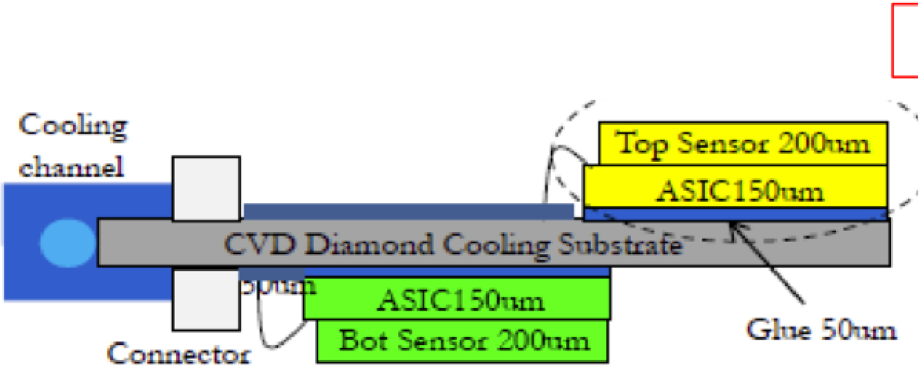
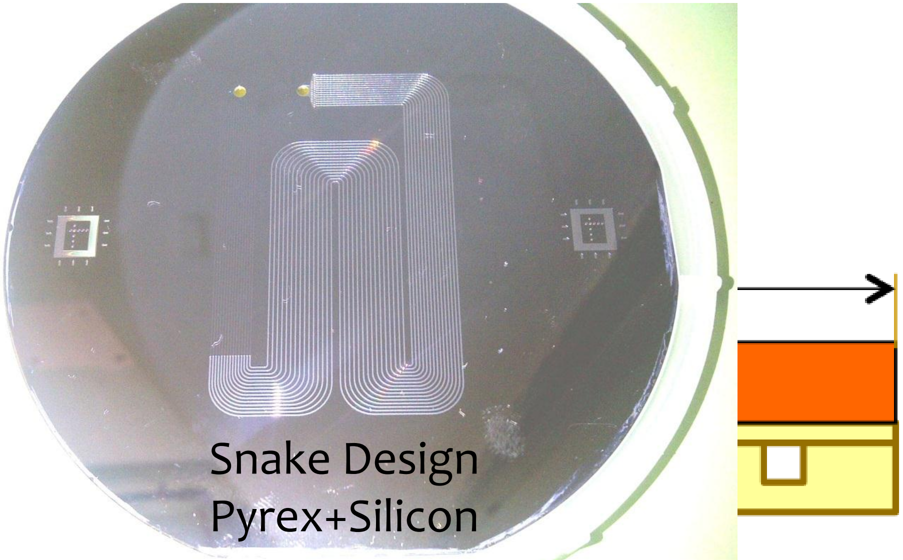




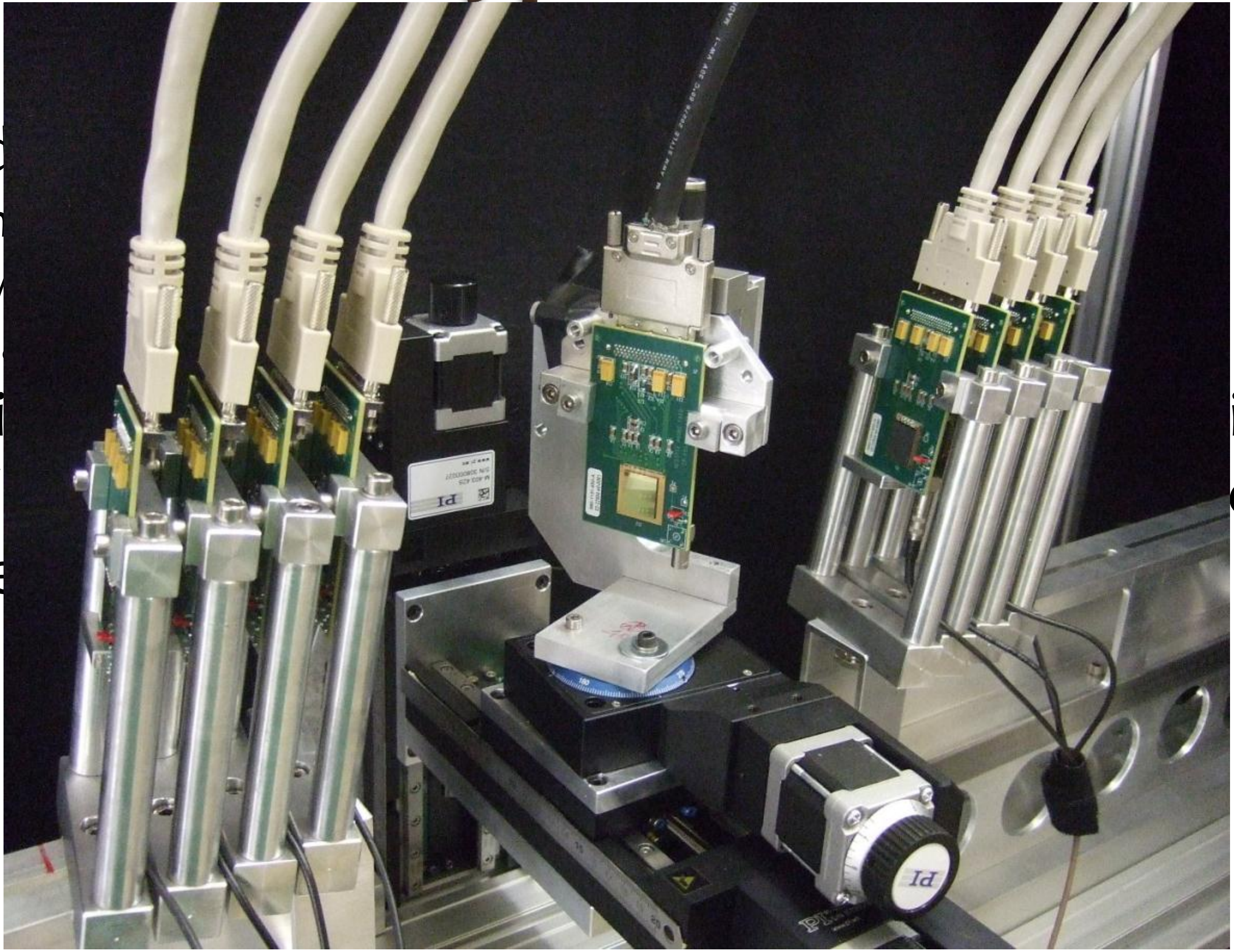
Micro channel

Prototypes and R&D

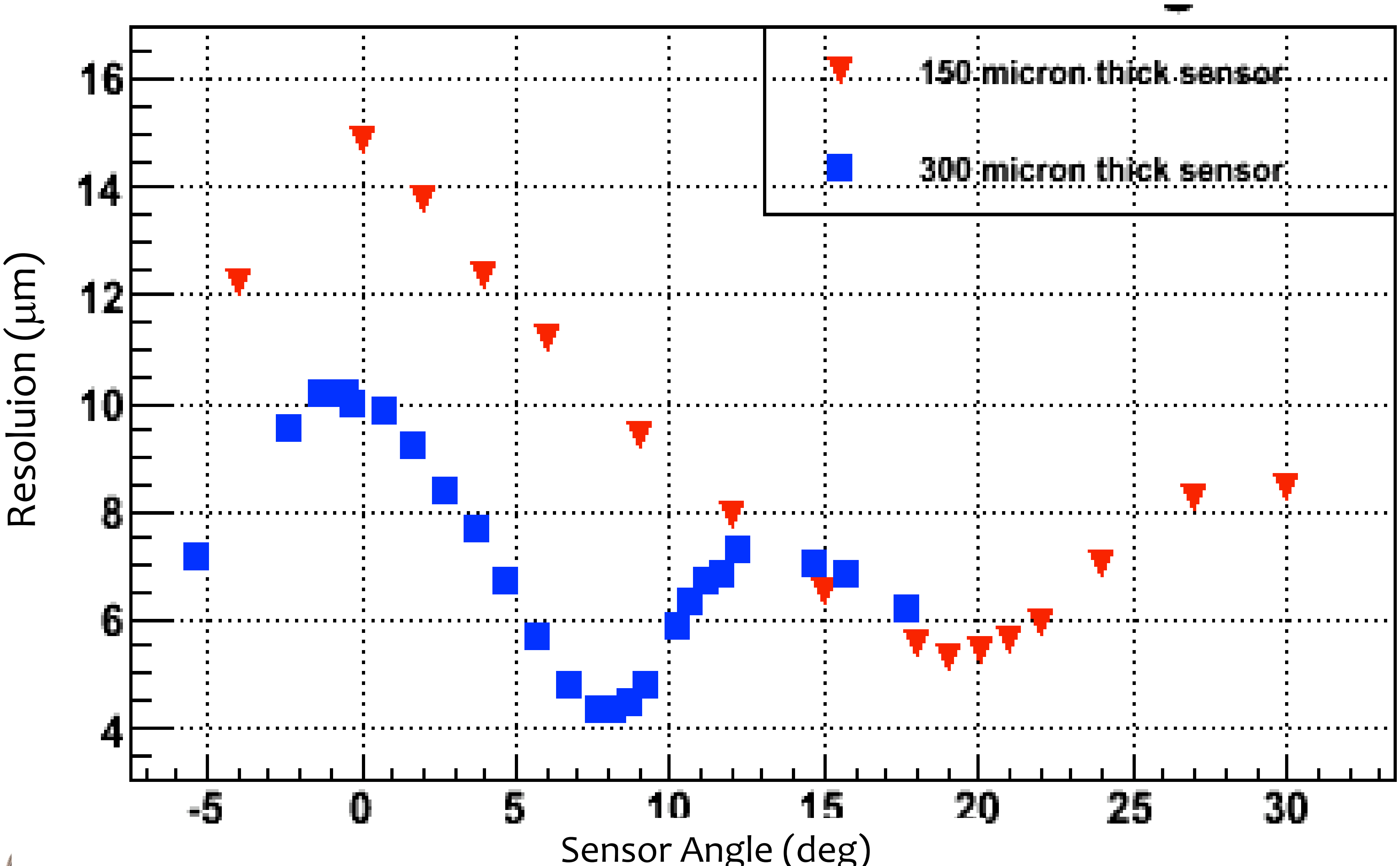
- Studies focusing on
  - Small to no Guard Ring designs.
  - Lowest material budget → Thin Sensors
  - Heavily irradiated sensors.
- Radiation hard ASICs with 130 nm IBM tech: Medipix3
- Performance evaluated using a Timepix telescope itself in beam tests.

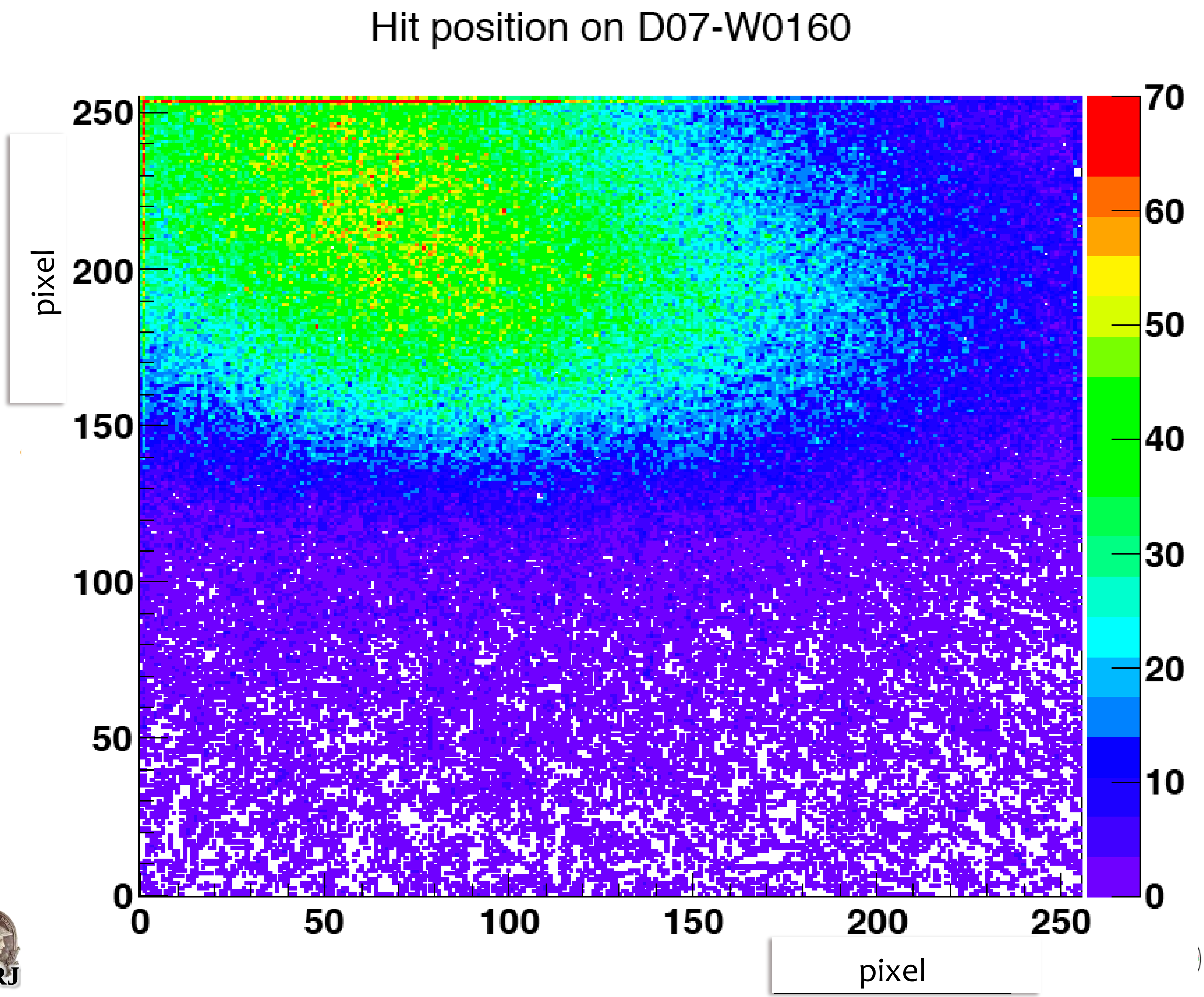
Prototypes and R&D

- Stud
  - sm
  - lov
  - he
- Radi ipix3
- Perf e itself in be

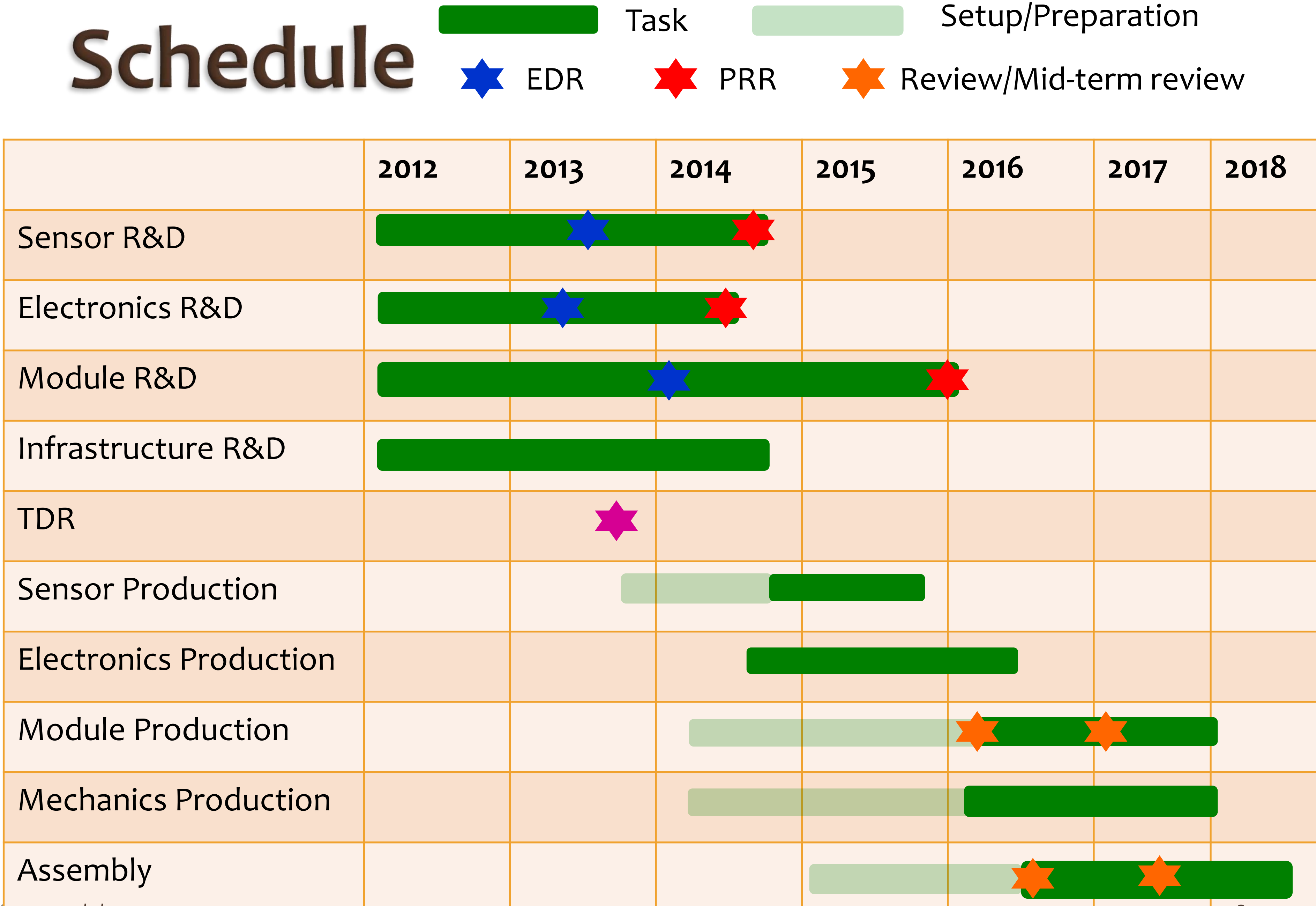


Prototypes and R&D




Hit position on D07-W0160
pixel
250
200
150
100
50
0
0
50
100
150
200
250
pixel
70
60
50
40
30
20
10
0

Schedule


Task
Setup/Preparation
EDR
PRR
Review/Mid-term review
2012
2013
2014
2015
2016
2017
2018
Sensor R&D
Electronics R&D
Module R&D
Infrastructure R&D
TDR
Sensor Production
Electronics Production
Module Production
Mechanics Production
Assembly

Summary

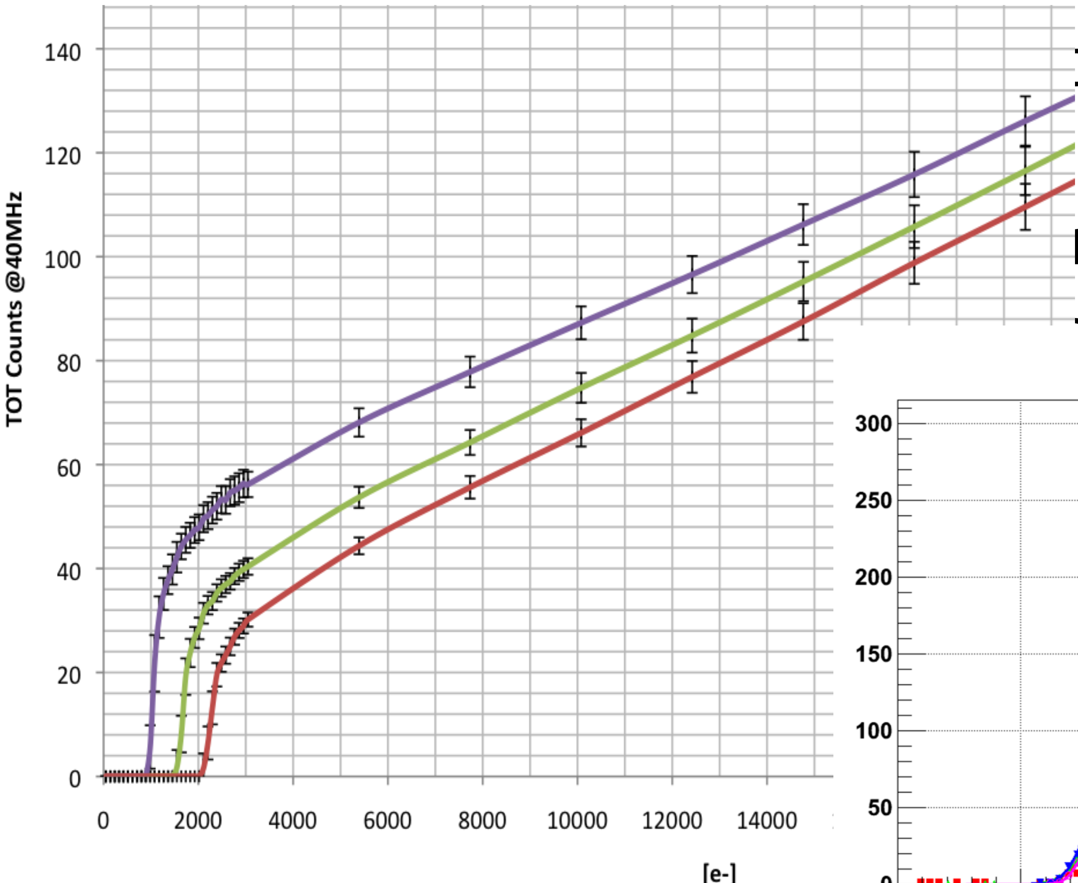
- The VELO detector is a successful vertex detector at the LHC.
- We plan an upgrade of LHCb and the VELO in the long shutdown of 2017-18
- The VELO pixel and strip options are being pursued and developed.
- We are still selecting over different sensor options
- R&D is progressing well in the key aspects of the detector: RF Foil, Cooling, ASIC, Sensors.
- Prototypes are being built and tested checking for the performance at high radiation doses.

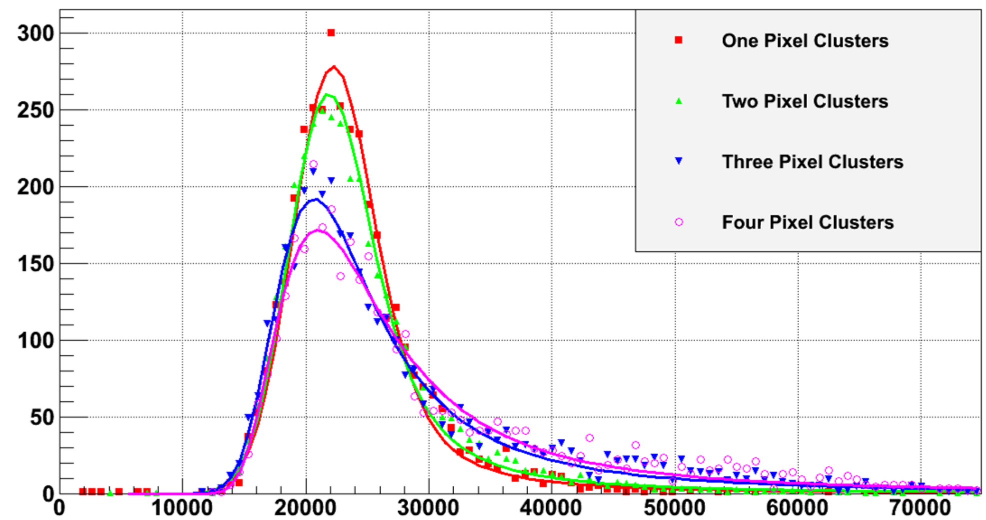
Back up

Prototypes and R&D

no Guard Ring

nm IBM tech





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  - Vacuum and Motion systems
- New components:
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  - Readout ASICs
  - New design of lower material RF foil
  - Multi Gbps readout system

- Main design concerns:
  - Enhance cooling to avoid thermal runaway
  - Huge data rate: zero suppression in the ASIC
  - Reduce material budget