Frontend Electronics development for the CMS pixel detector upgrade

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Pixel 2012, Inawashiro

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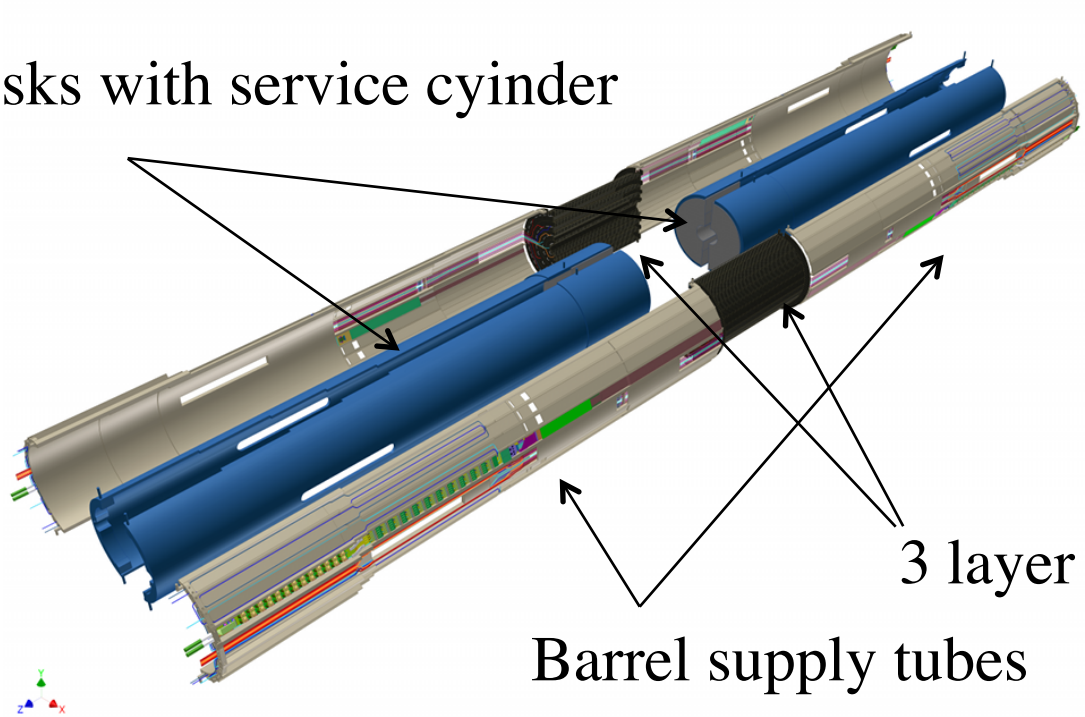
CMS Pixel System



- Designed for fast insertion (beam pipe bake out)
- Can be done in regular shutdown
- Will be replaced by improved system

Outline

- What is the phase I pixel upgrade
- Consequences for the front end electronics
  - Modules
  - Module controller ASIC: **T**oken**B**it**M**anager
  - Modified readout chip
- First preliminary results
- Conclusions

Phase I Upgrade Project

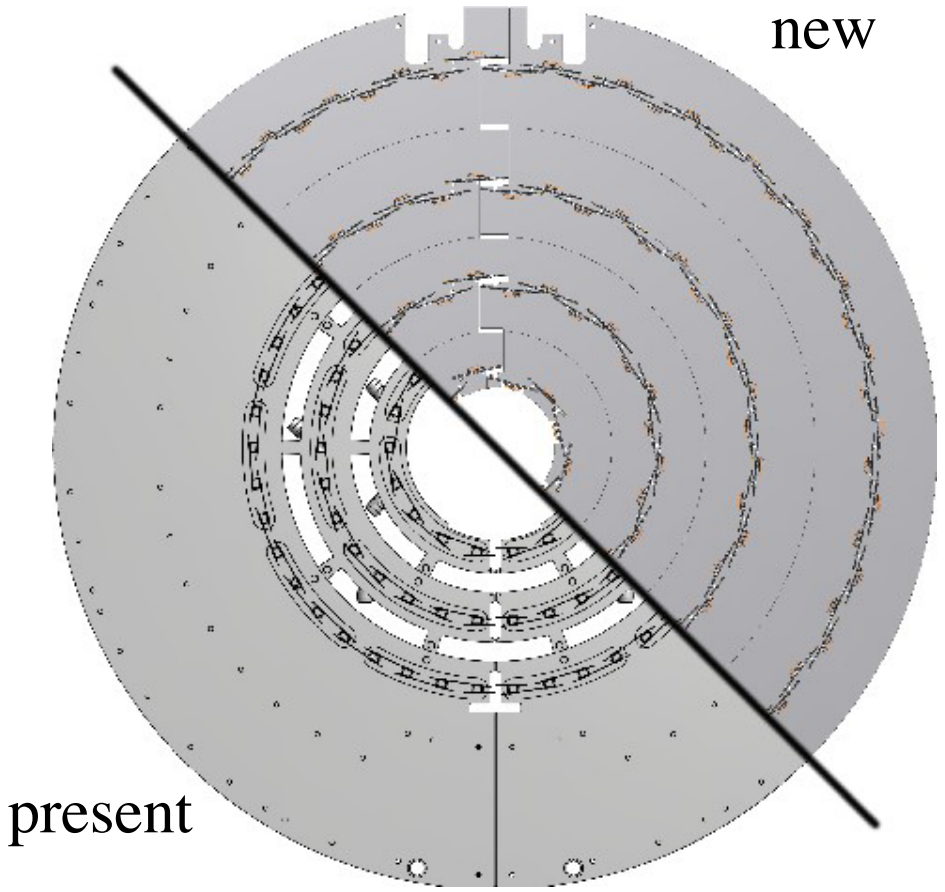
Phase I Pixel Upgrade

- Motivation: Maintain or improve physics performance under higher interaction rates. Target is 2x10^34 eventually at 50ns bunch structure -> up to 100 pile up events!
- For the pixel detector this means:
  - Track seeding: more robust with 4 point coverage and 3 out of 4 seeding. Smaller extrapolation to first strip layer with intermediate barrel and end disk layer
  - Better vertex resolution through consequent reduction in mass (multiple scattering)
- Target insertion time is 2016/17
  - Extended technical stop of LHC will be sufficient

Mechanics of Barrel

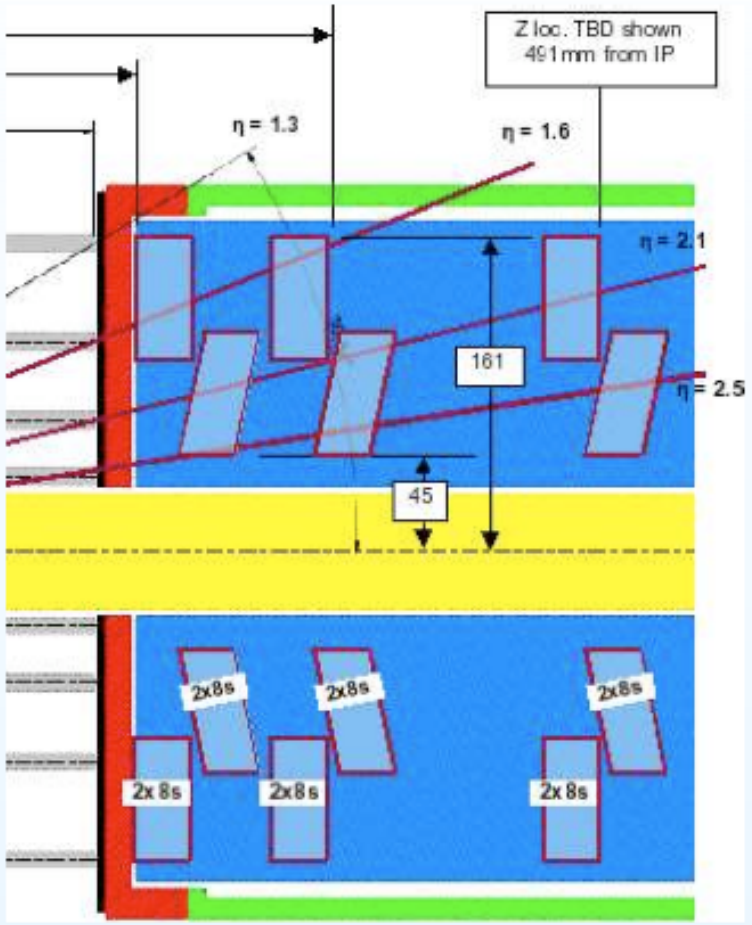
Add 4th layer :

- layers @ 29,68,109 & 160 mm
- beam pipe clearance 2.5 mm !
- 8 modules along z
- Total 1184 sensors (today 768)
- Channel number increase from 48M to 79M



Mechanics of Disks

- 3 + 3 discs @ barrel ends
- Each disc consists of:
  - 2 half discs
  - inner & outer ring of modules
  - inner ring tilted by 12°
- 4 point coverage up to η= 2.5
  - very small gap ~ η= 1.3
- Total number of modules unchanged, but larger.
  - Channel increase from 18M to 45M



Mechanics of Disks

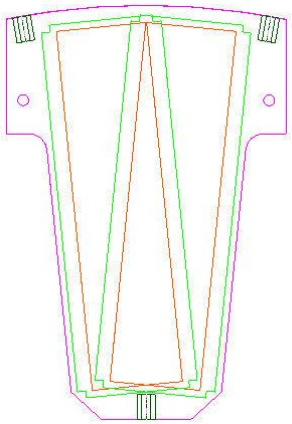
Inner & outer ring of blades

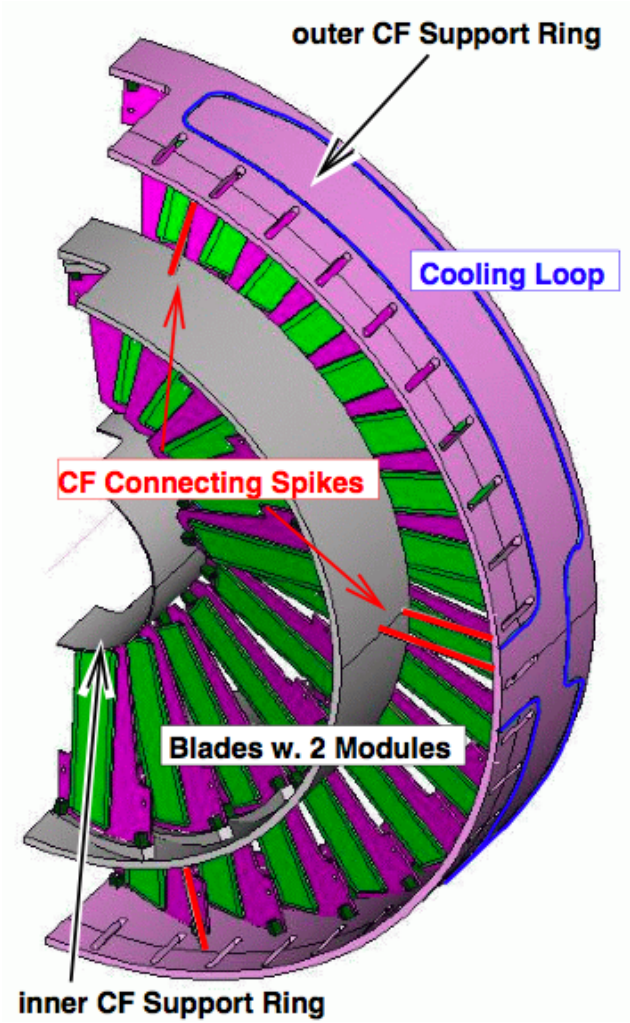
CO_2 tubes embedded in half disk support:

- support cylinder:
  - Carbon carbon
  - Grooves for cooling tube
  - Stainless steel tube:
  - 1.8mm OD, 100μm wall

Blades:

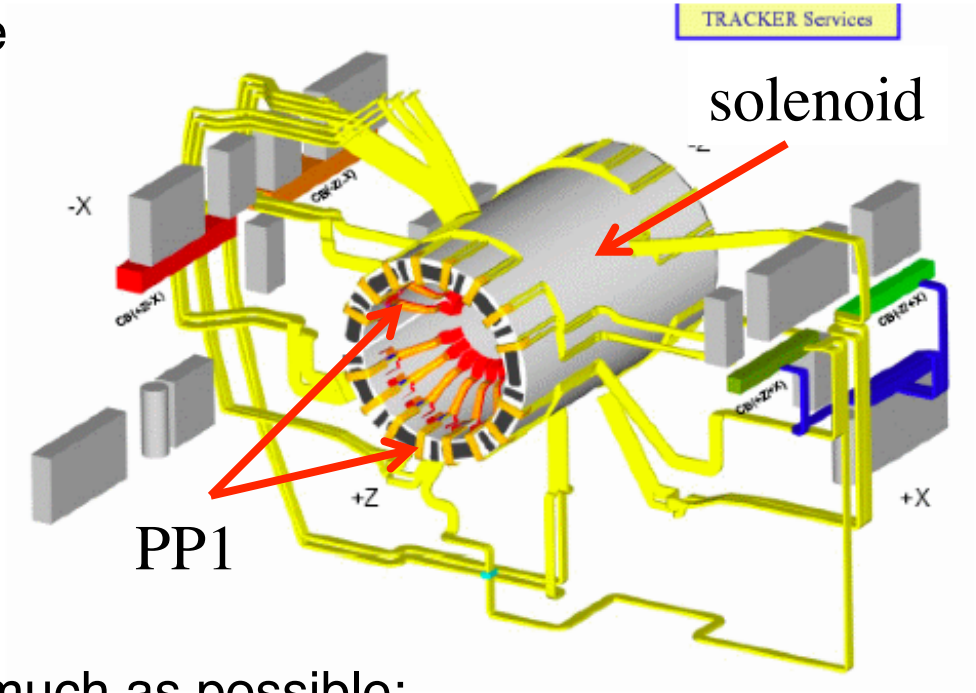
- all identical
- Rotated by 20^o radial
- Tilted by 12^o (inner ring)
- 2 modules per blade (ϕ overlap)
- individually replaceable





Constraints and Requirements

- Same mechanical envelope as present system
- Same services from PP1 outwards
  - → faster data links
  - →new powering scheme (DC/DC converter)

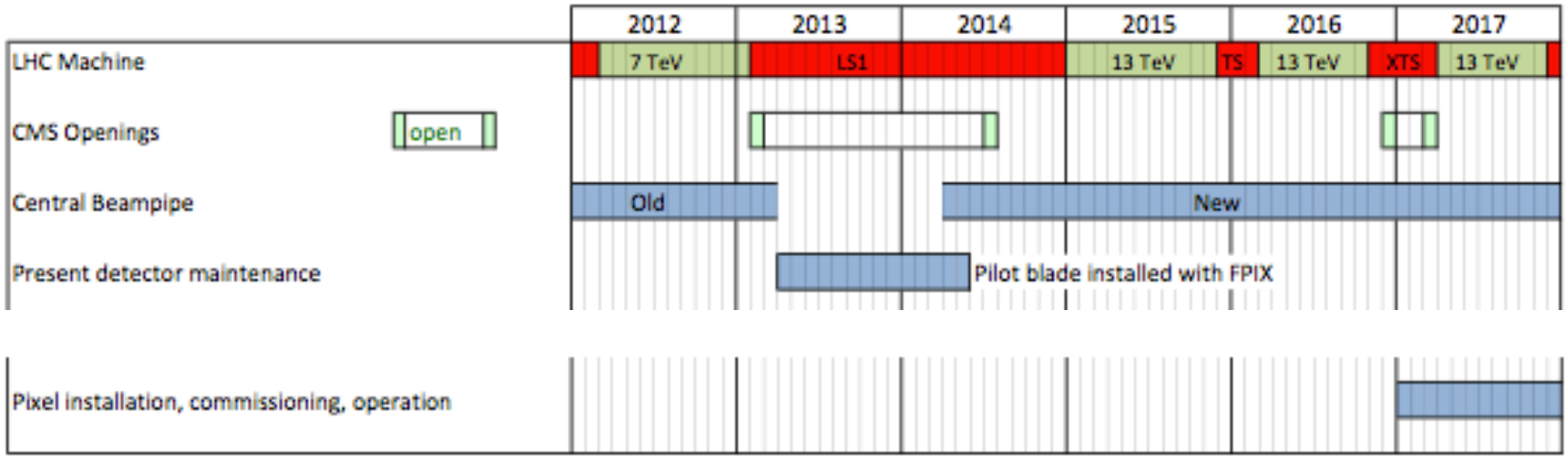


Leave system unchanged as much as possible:

- keep ROC core untouched. It works well and is well understood/debugged
- New system will be assembled and fully tested / calibrated at CERN

--> **minimise recovery time** in competetive physics situation

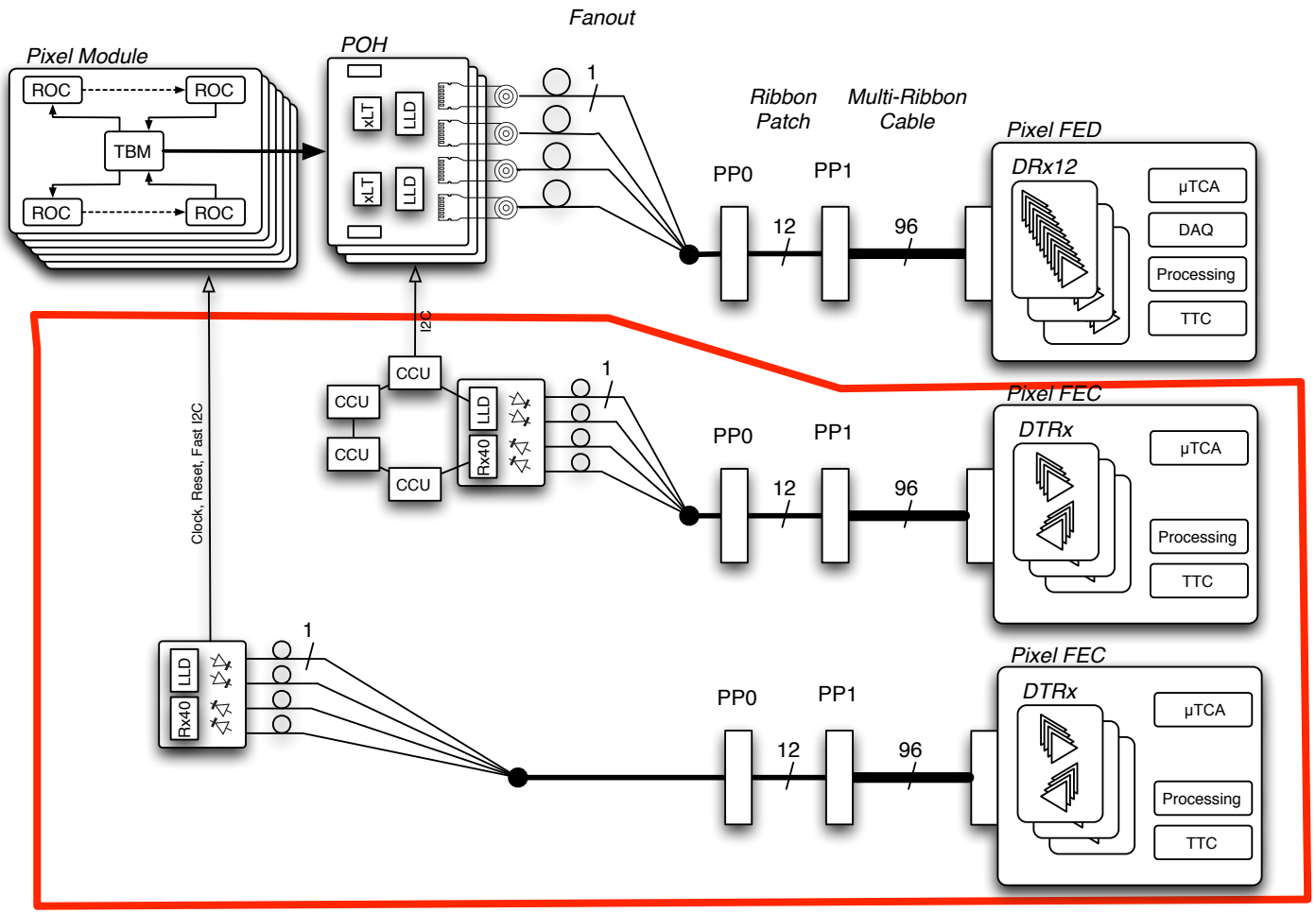
Schedule



- Install pilot system in long shutdown 2013/2014
  - Small scale system with all modifications added to present pixel system in FPIX region
  - Gain operational experience, head-on start
  - Develop firmware/software for smooth transition to full system
- Insertion of full system in extended technical stop 2016/2017

Front end electronics

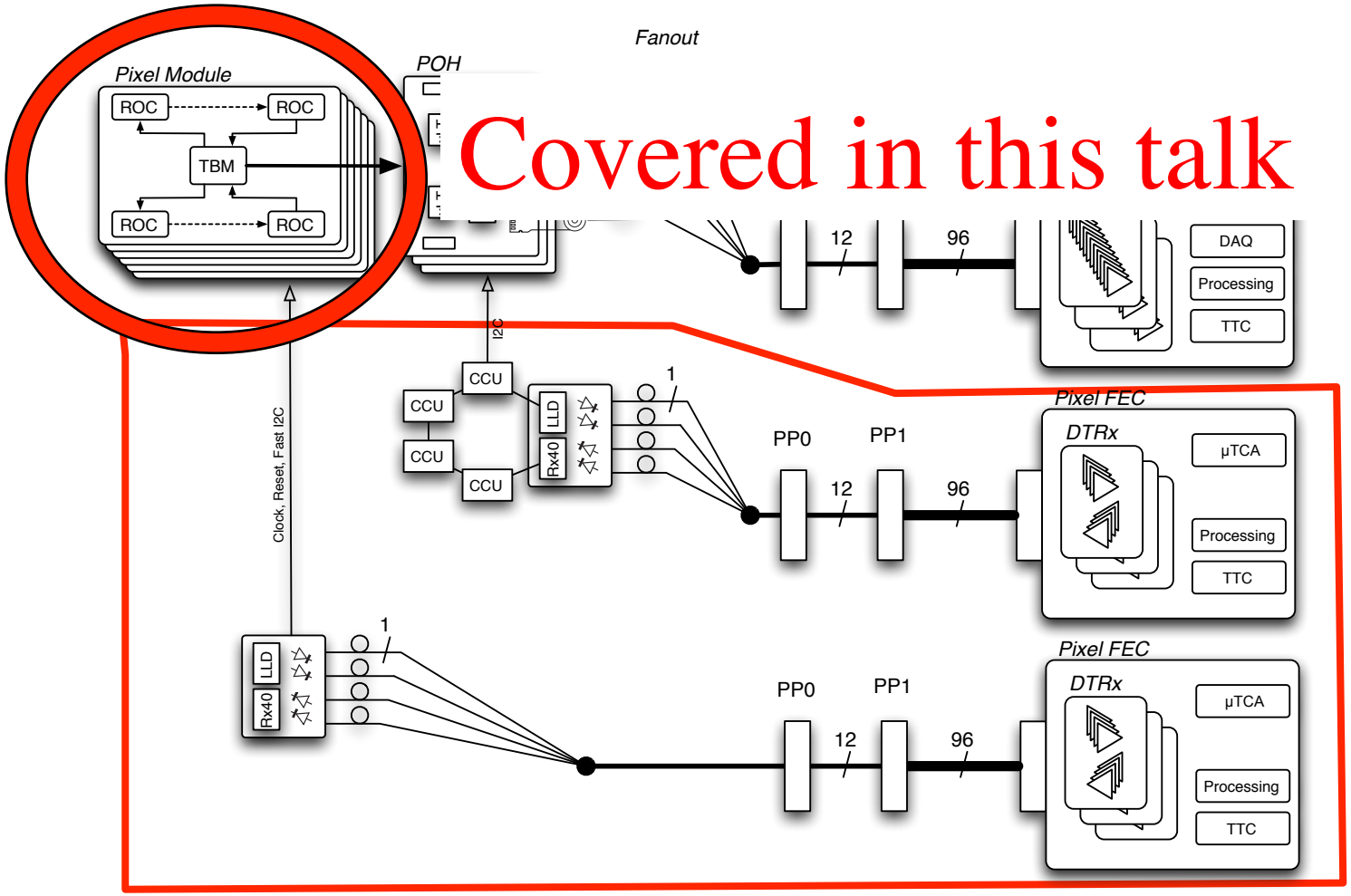
Control and Readout



All new except fibre plant

Module control protocol unchanged

Control and Readout



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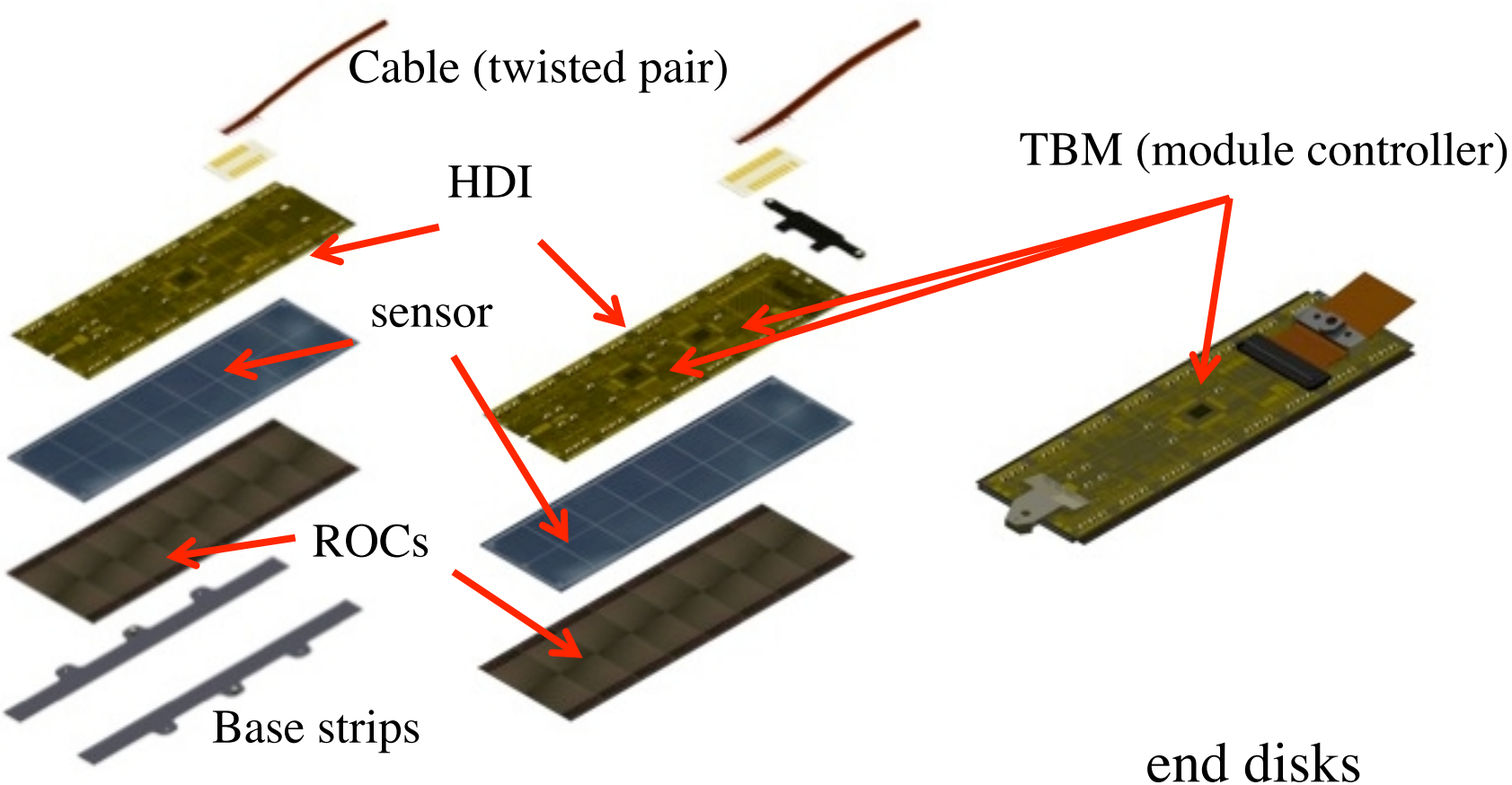
Modules

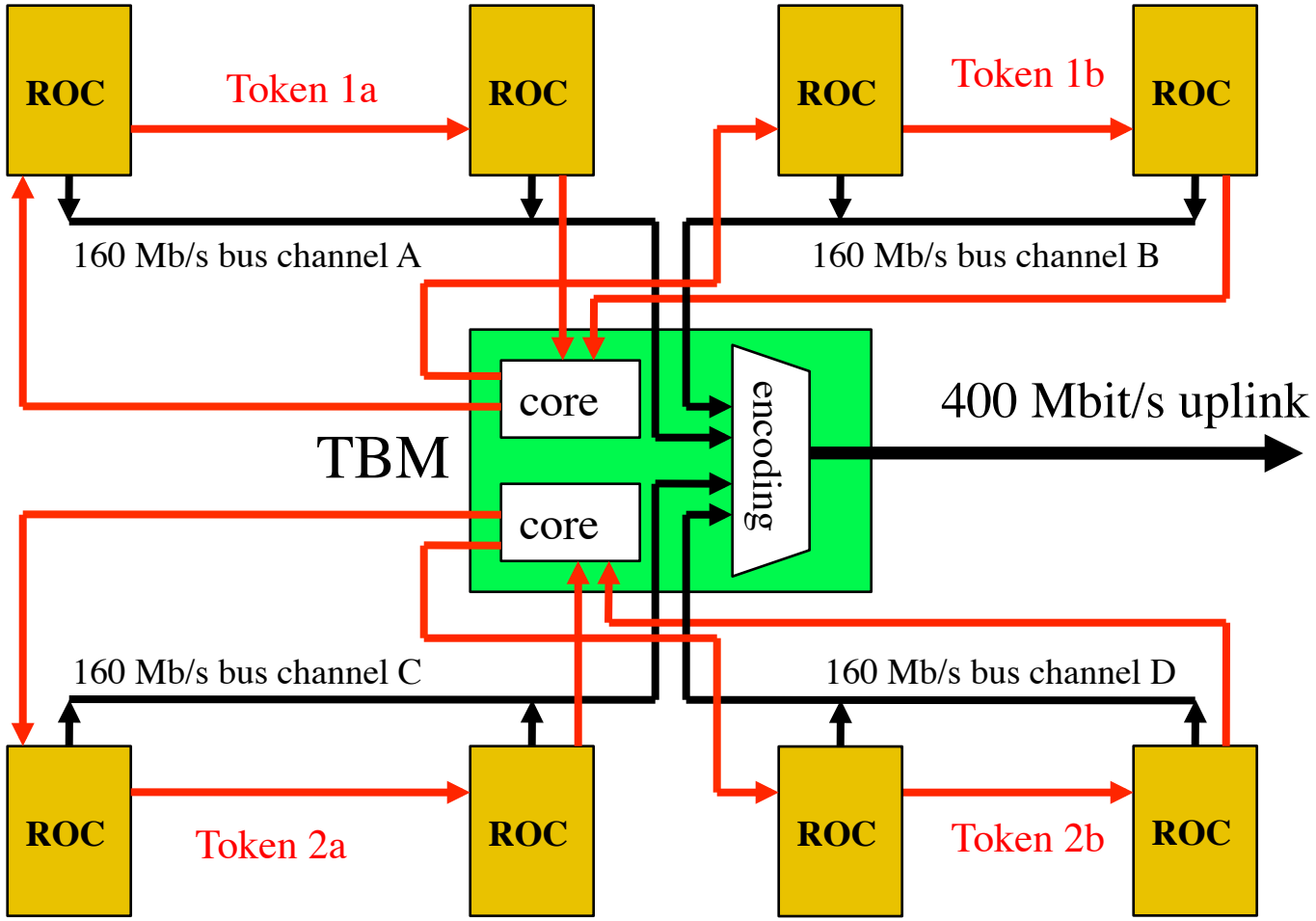


barrel layers 2-4

barrel layer 1
no base strips, thinner

end disks
different mounting/
cable

Basic Idea of digital module

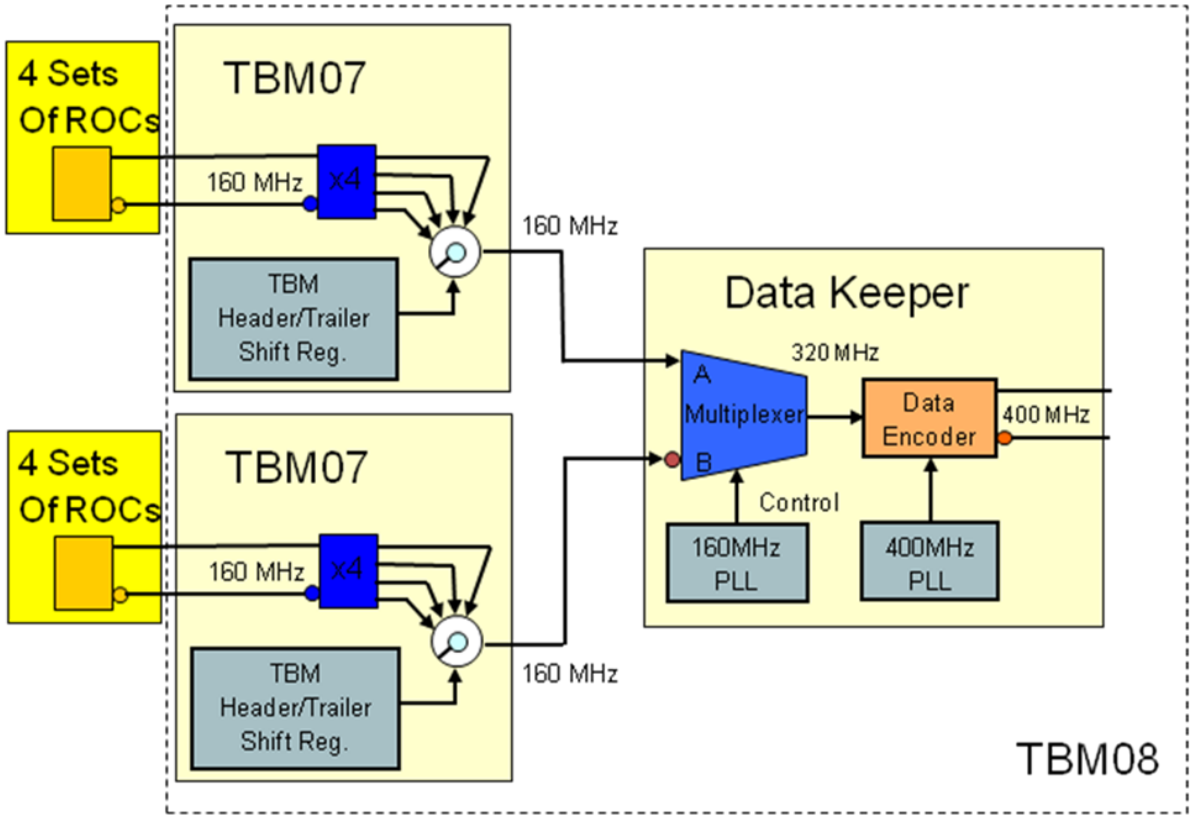


- 2 or 4 token rings
- 4 readout buses
- 4/5 bit encoding
- Up to 2 links of 400 Mb/s

TBMs

- The Token Bit Manager (TBM) controls the readout of a collection of ROC's and distributes clock, trigger and resets
- Must be modified, to accommodate new digital readout
- Since data load vary strongly it comes in 3 flavours
  1. TBM07: outer rings of end disks. One data link at 160Mb/s. Controls one side of a blade. Two outputs are combined to 400Mb/s by DataKeeper chip
  2. TBM08: Inner rings of end disks and outer two barrel modules. Combines functionality of 2 TBM07 plus DataKeeper in one piece of silicon. One encoded 400MB/s output link.
  3. TBM09: Inner two barrel layers. Two encoded 400Mb/s output links. Equivalent of two TBM07 plus two DataKeeper chips.

TBMs


4 Sets
Of ROCs
TBM07
160 MHz
X4
TBM
Header/Trailer
Shift Reg.
160 MHz
4 Sets
Of ROCs
TBM07
160 MHz
X4
TBM
Header/Trailer
Shift Reg.
160 MHz
Data Keeper
320 MHz
A
Multiplexer
B
Data
Encoder
400 MHz
Control
160MHz
PLL
400MHz
PLL
TBM08

Readout Chip for Phase I

Limitations of present ROC at Phase1:

1. Limited buffer sizes for data storage during trigger latency
   → **Increased data loss in double columns**
2. Long readouts. Long waiting time for readout token.
   → **Readout related data loss**
3. Much higher channel count / almost same number of fibres
   → **Faster data links.**
   → Present 40 MHz analog link will no longer be adequate and can hardly be adapted
4. Have to withstand higher than specified irradiation dose

Phase I ROC

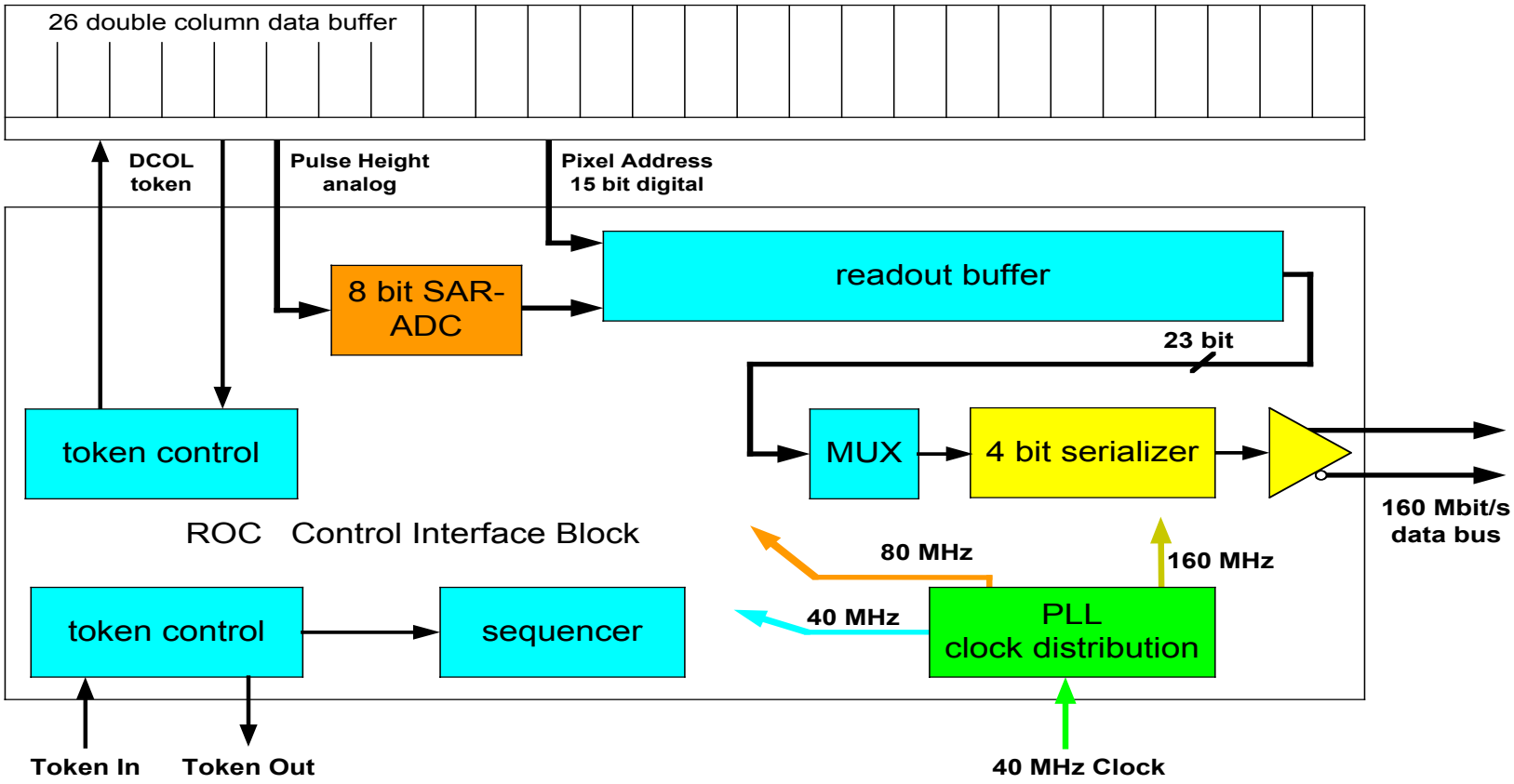
- Based on present ROC
  - IBM 250nm. Had to change to fab in Burlington, USA
  - Present ROC is well understood and debugged
  - Can be modified to cope with new requirements
  - Cheap and relatively ‚simple' technology (short development time)
- Staged development.
  - Barrel layer one ROC needs additional modifications in column drain, but few modules only→somewhat relaxed time schedule
  - Two ROCs will be pin compatible

PSI46dig design

Design changes with respect to present readout chip:

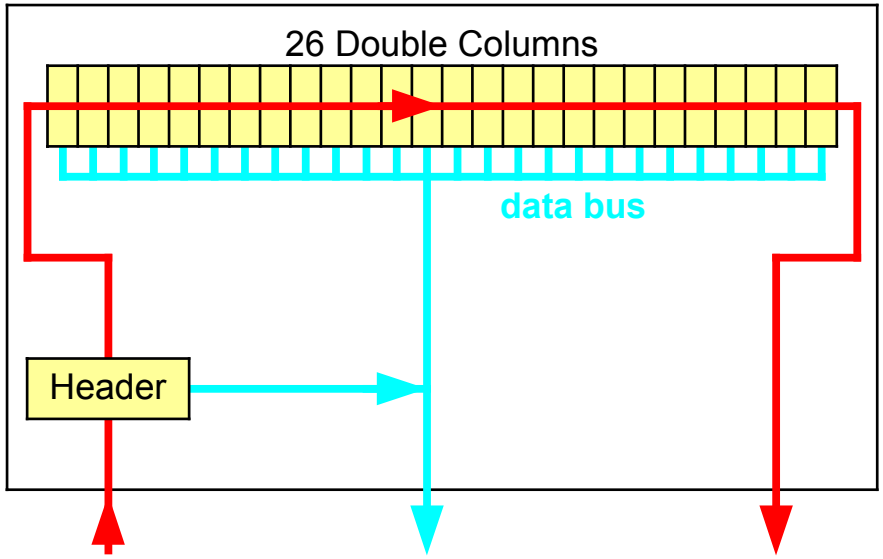
- Improved analog performance
  - New powering scheme: better uniformity, less X-talk → lower threshold
  - Optimized faster comparator → lower intime threshold, less x-talk
  - Lower threshold translates into longer detector lifetime
- Digital readout
  - Needs higher clock frequency on chip: PLL
  - Fast pulse height digitization: low power 8-bit ADC
- Enlarged data buffers. Had to redo layout due to space restrictions
- ROC readout buffer (FIFO)
  - Readout buffer FIFO on the ROC level.
  - New readout logic

ROC Periphery Upgrade to Digital Readout (core unchanged)



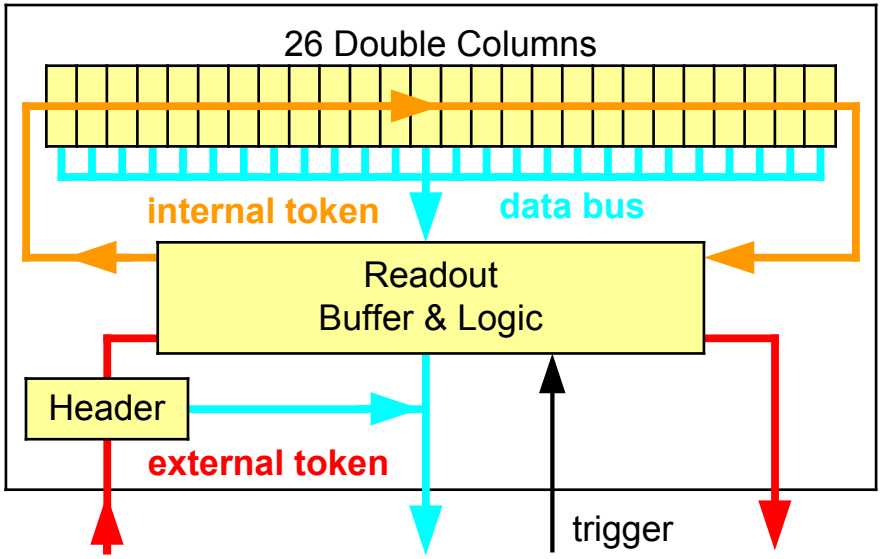
Buffered Readout

present ROC



- Double columns with verified data stops → no more events accepted
- Double columns have to wait for external token → long dead time
- Sequential readout of of 8/16 ROCs → high token delay

new ROC



- DCol readout parallel in all ROCs after trigger → reduced waiting time
- ROC readout buffer: read/write simultaneous; data with different time stamps
- Easy implementation in separate buffer on ROC → keep present DCol logic

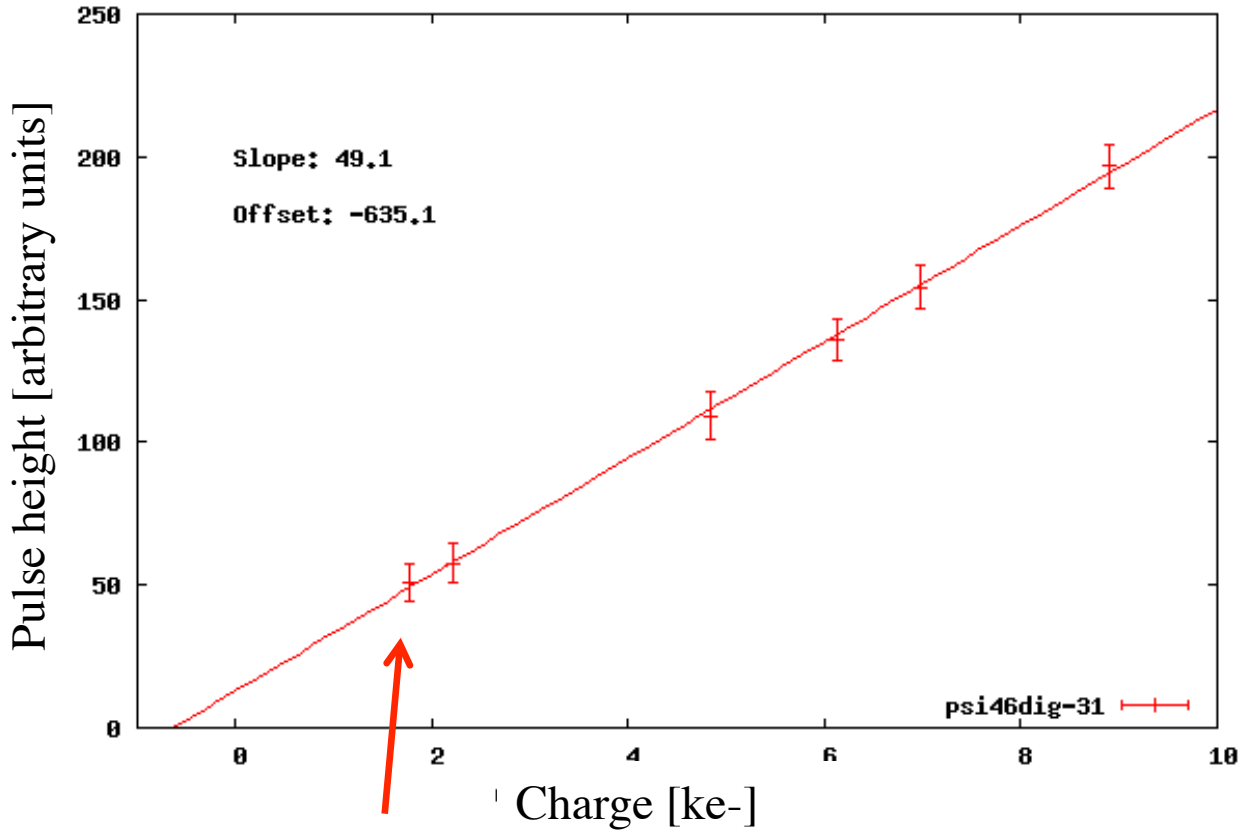
First results

First tests of ROC

- The first iteration of the digital ROC is currently unter test
- Results are **preliminary**
- Digital readout works well
  - ADC very linear (within last digit)
  - PLL has extremely wide locking range (15-70MHz)
  - Output buffer logic works flawlessly
- Analog performance looks encouraging
  - See next slides
- Slightly reduced power consumption wrt present ROC

Analog performance: threshold

Measurement in X-ray with fluorescence, random trigger



Absolute threshold as low as Fe fluoresence (1.8ke-)

Analog performance: Timewalk

	Present ROC	Digital ROC
Noise	~180e-	~180e-
Threshold dispersion	~90e-	~80e-
Minimal threshold	2.5 ke-	<1.8 ke-
In-time threshold	3.2 ke-	<1.8 ke-

Timewalk has two contributions:

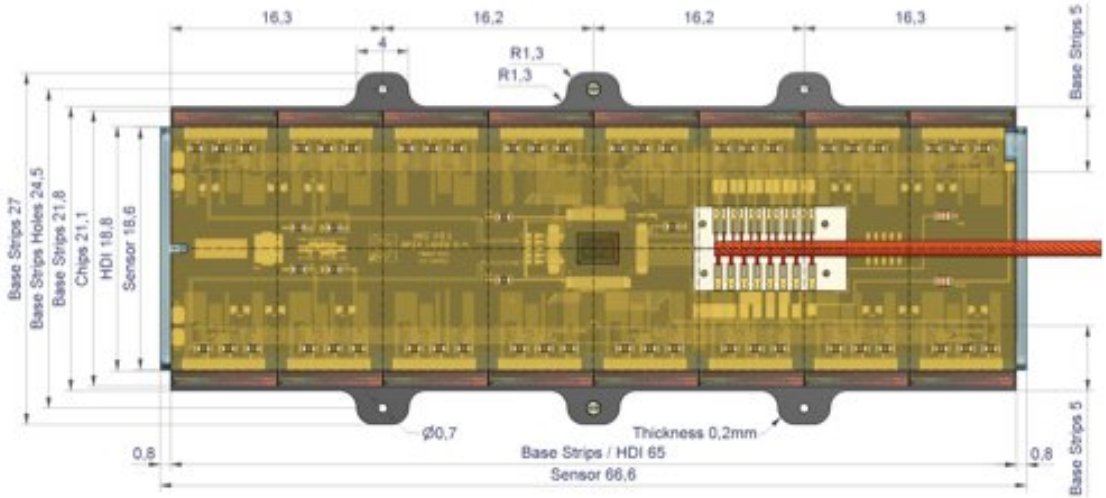
1. difference of preamp signal output
2. Comparator switching slower for low overdrive (close to threshold)

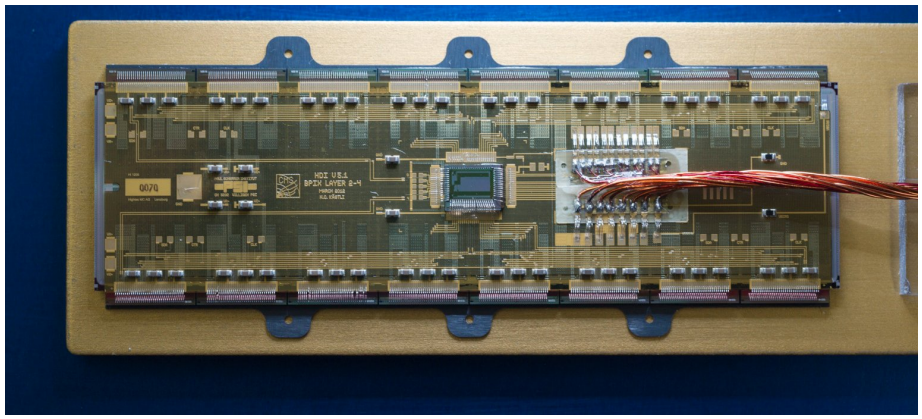
The later was dominating in the old ROC. For the improved comparator there is no measurable difference between absolute and in-time threshold. This gives a direct reduction in the operational threshold of 700 e-.

Issues / Questions

- Not everything went smooth...
  - Power-up circuit does not release reset. Couldn‘t really find reason. Presumably some kind of ‚soft‘ latch-up. Workaround exists.
  - There is a flaw in the trigger logic. Can send next trigger only after reading out previous hits
  - By making layout of trigger latency buffers denser introduced X-talk to analog pulse height
  - TBM has wrong polarity of readout-token-input→ does not send trailer.
- Open questions still to be addressed: operational margins after irradiation?
  - Configuration parameter (found difference to other foundary)
  - We will irradiate digital ROCs up to 10^{15} N_{eq}/cm^2 at PSI
- Next iteration will be submitted 12/2012

First prototype of barrel module





Just produced 1st prototype (last week). Works well with aforementioned limitations. Under study now.

Conclusions/remarks

- CMS will replace the entire pixel detector in the extended technical stop 2016/2017
- New system has 90% higher channel count
  - Need faster readout links → digital readout
  - Need lower data loss at up to 4 times the design data rates
  - New digital readout chip is based on present one. Same 250nm IBM process, however in different foundary (IBM France no longer available)
  - Improved analog performance
  - Few problems identified and solved. More testing needed
  - Resubmission end of this year
- Pilot system will be installed during long shutdown 2013/2014
- Barrel layer 1 will still need an improved version to cope with enormous data rate → change column drain mechanism to dynamic cluster finding. To come in 2013.

Thank you !