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Frontend Electronics development for the CMS pixel detector upgrade

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The performance of the LHC accelerator at CERN has been outstanding since its startup in 2010. It seems likely that the delivered instanteneous luminosity exceeds its design value of 10^{34} cm^{-2}sˆ{-1}$ soon after the recommissioning in 2014. Tracking in such a dense environment is challenging. This is especially true for the main tasks of the pixel detector such as b-tagging. In order to compensate for the expected decrease in performance due to the high number of simultaneous interactions, an upgrade of the pixel detector has been proposed. The innermost barrel layer moves closer to the interaction region and a forth barrel layer and a third endcap disk on each side have been added.\\
In order to cope with this substantial increase of data rates, an improved version of the front end electronics is needed. The new CMS pixel readout chip (ROC) is developed in two steps, based on the present ROC. In a first step, several measures have been taken to lower the inefficienies inside the ROC and to improve analog performance. The output data format has been changed to a digital scheme to increase data throughput. In a second step, the core of the so called Column Drain architecture needs substantial modifications to cope with the data rates expected in the innermost barrel layer.\\

We will present the overall concept of the front end electronics development and show results from measurements of the first step prototype chip.

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