

3D Integration for SOI Pixel Detector

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(T-Micro)

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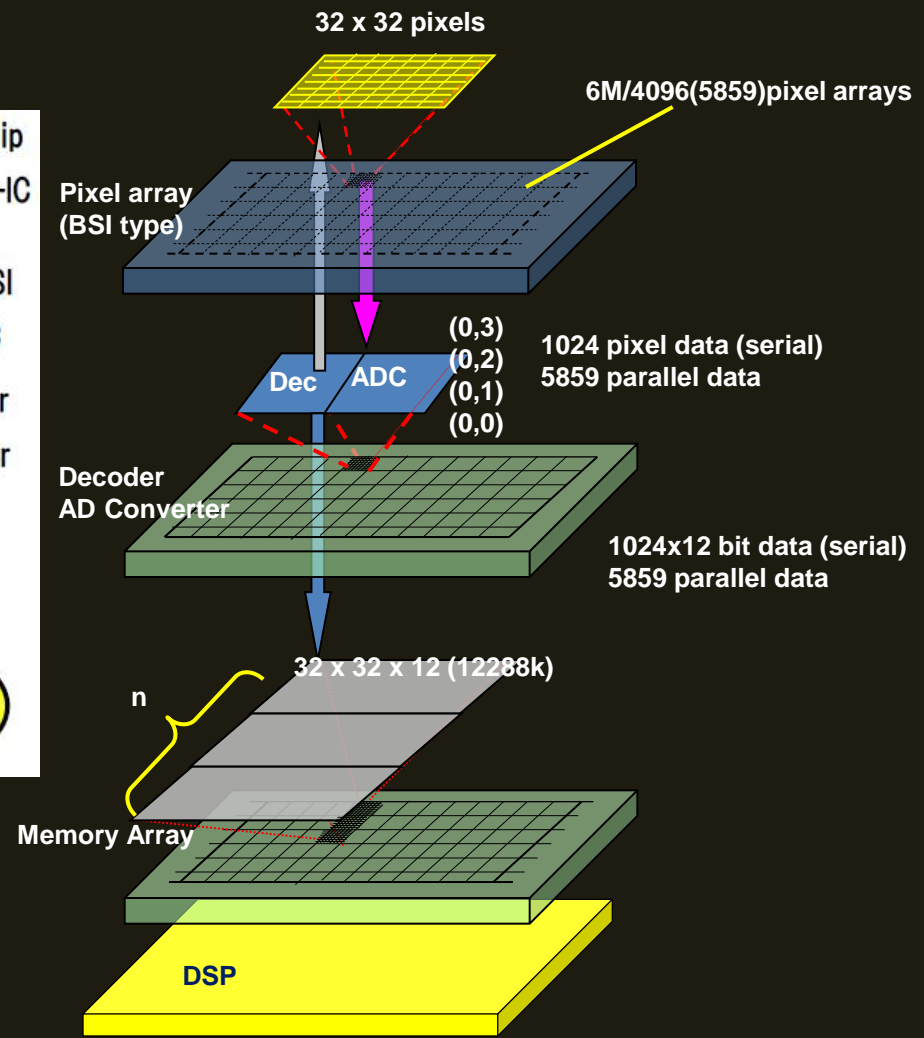
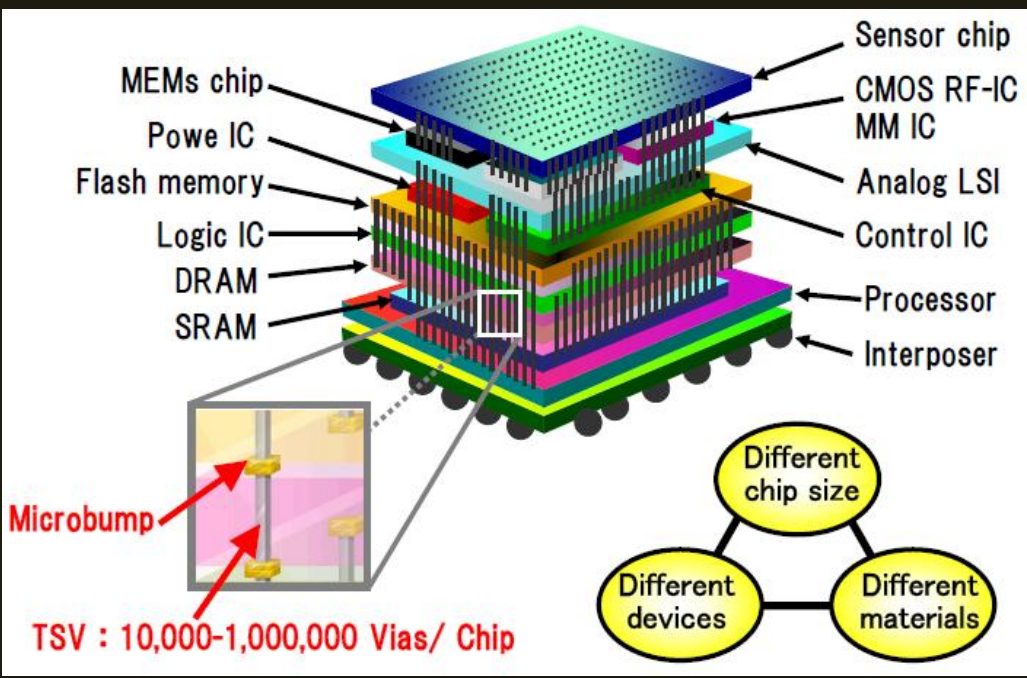
process issues and counter measurements

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Target of our 3D technology

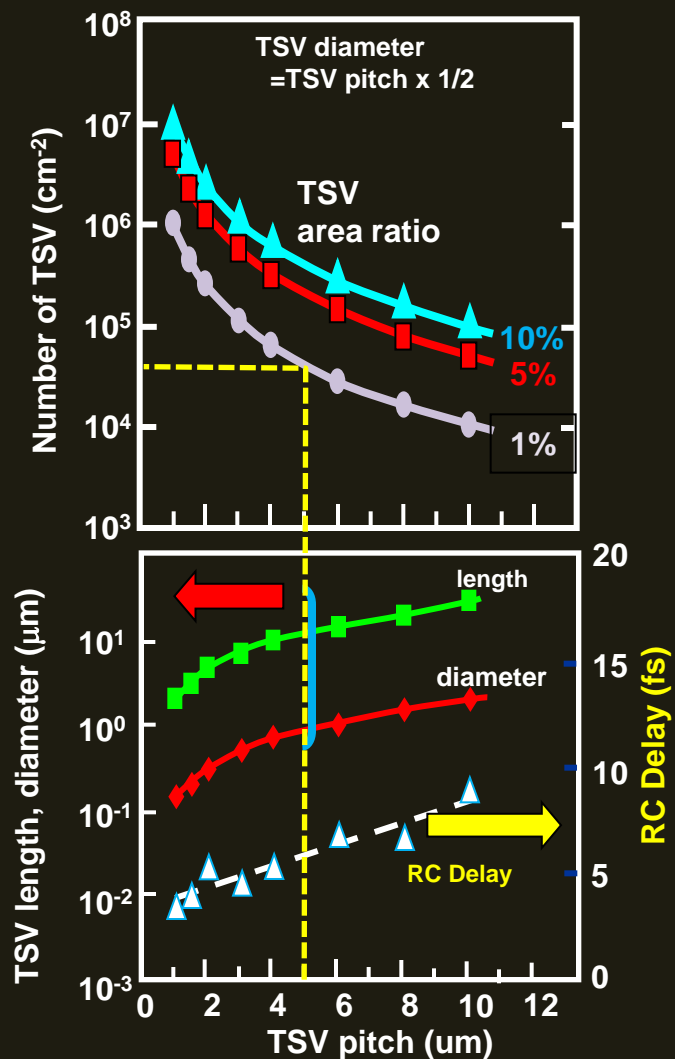
Realize High Speed Parallel Processing Pixel Sensor with Memory



Target 3D Technology

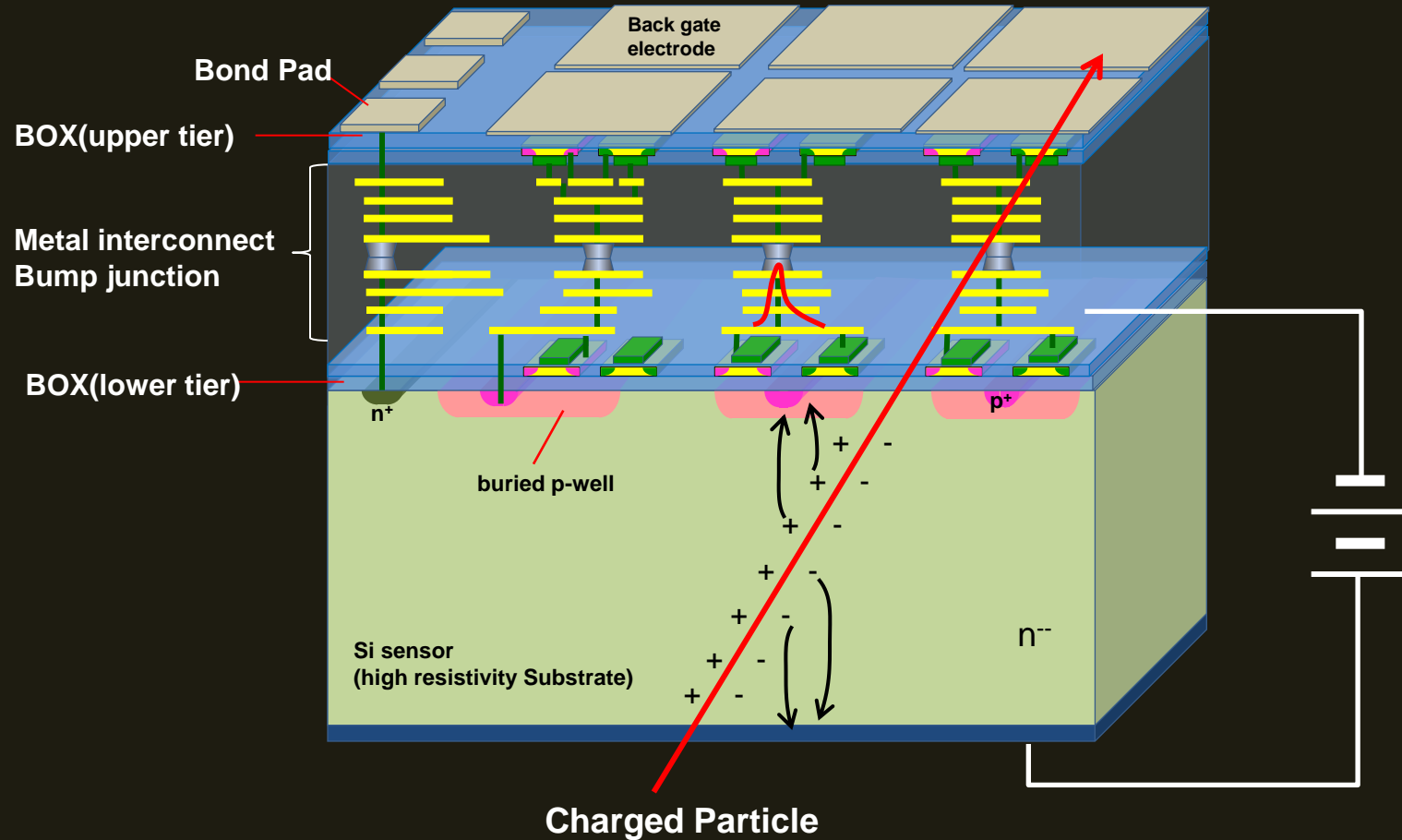
- Via last process
- Interconnect density $10^4 \sim 10^5 / \text{cm}^2$
- Area penalty $\leq 1\%$
- Good manufacturability (high yield, reliability)
- Low process temperature
- Low cost

TSV and μ -bump technology with the pitch less than $5\mu\text{m}$



M. Koyanagi et al.,
IEEE Trans. Electron Devices,
VOL.53, NO.11, pp.2799-2808, 2006

Stacked SOI Pixel detector



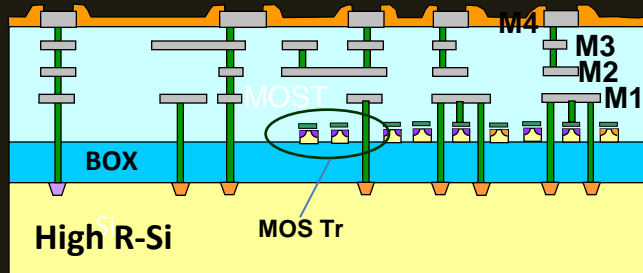
Process flow (1)

(a) Start with FD-SOI device wafer

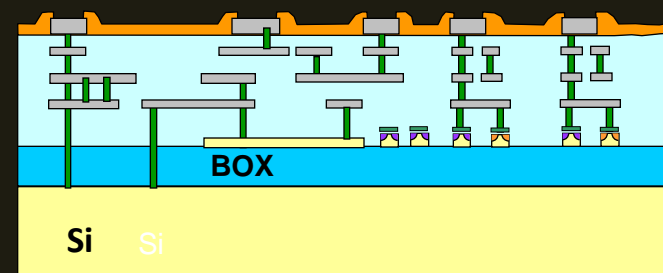
Active Si ~ 50 nm
BOX: 200 nm

*FD: Fully Depleted

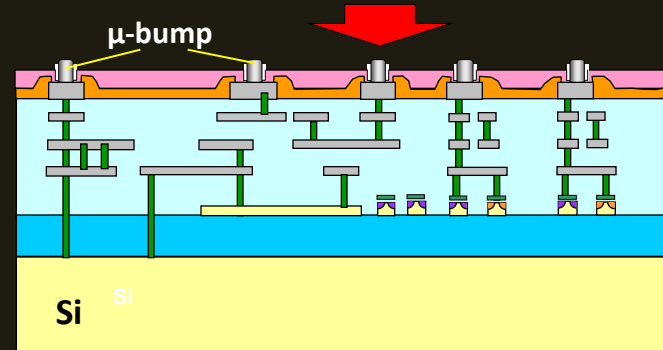
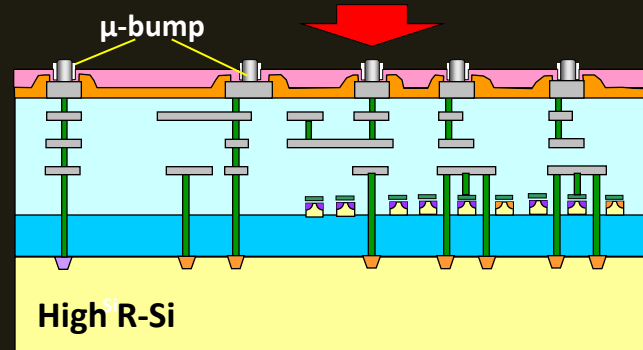
< Lower Tier >



< Upper Tier >

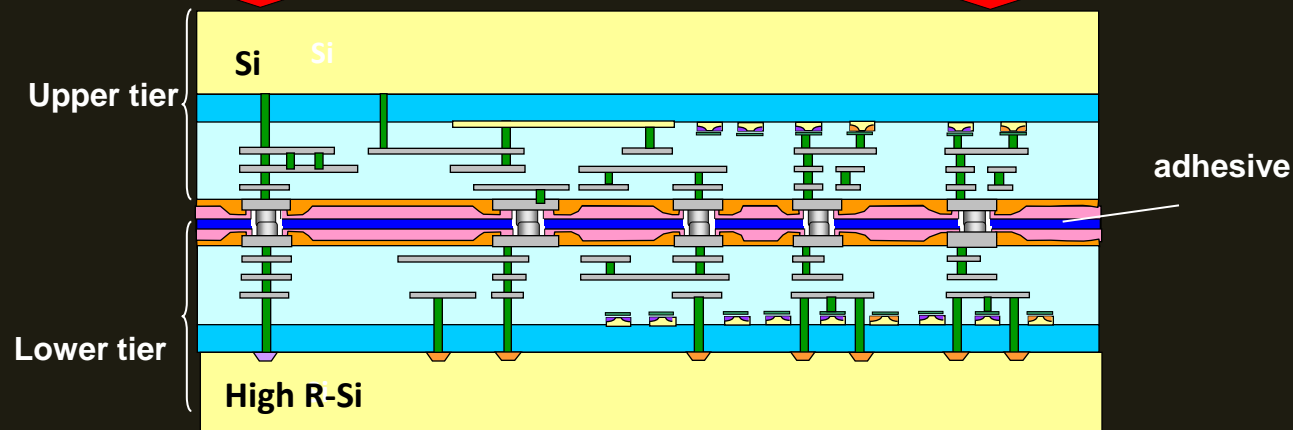


(b) μ -bump forming



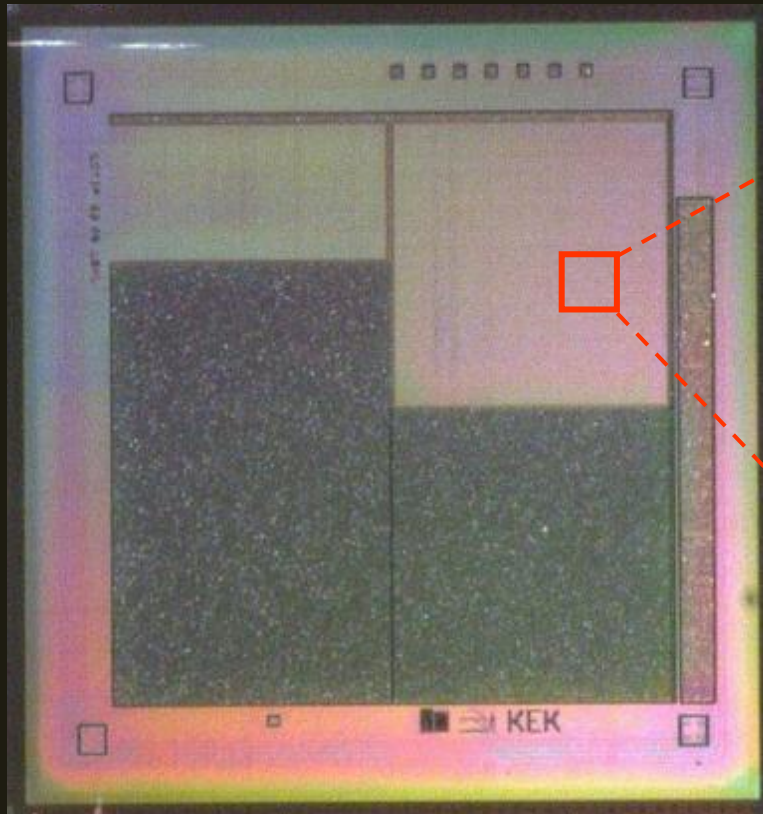
(c) Chip bonding

- face to face infrared alignment
- temporary bonding
- Adhesive injection
- permanent bonding (<200°C)

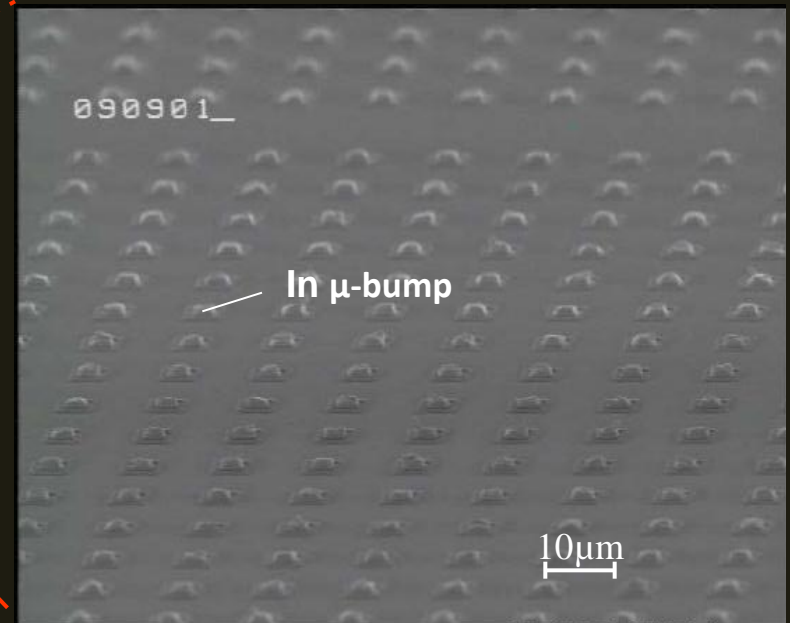


SOI pixel detector Chip

(After forming u-bump)

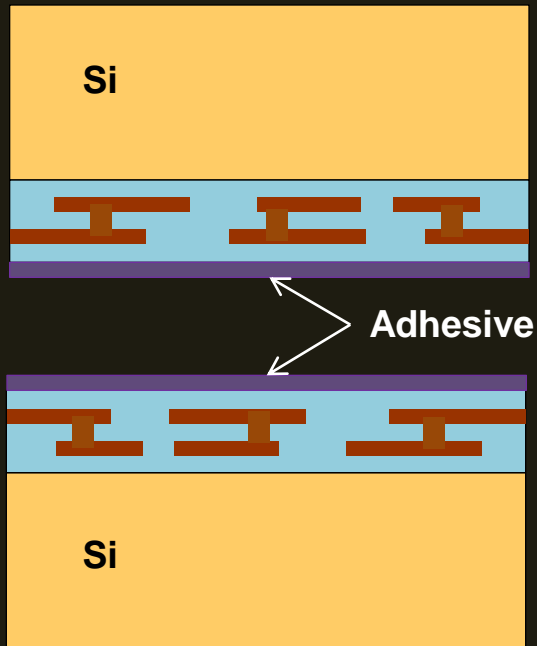


Upper tier

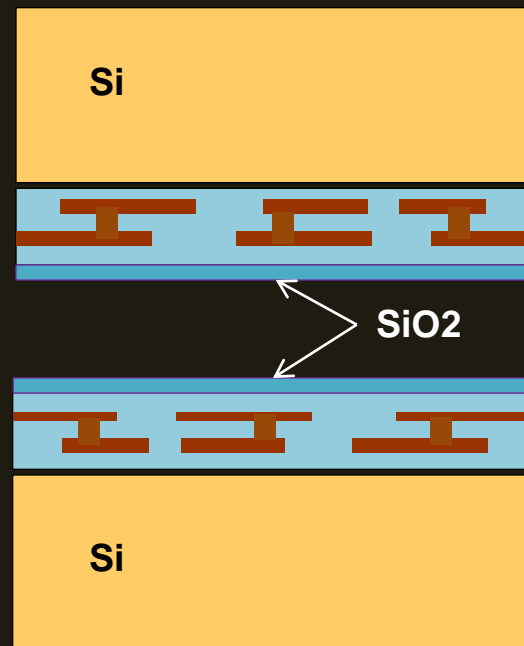


Detector Array

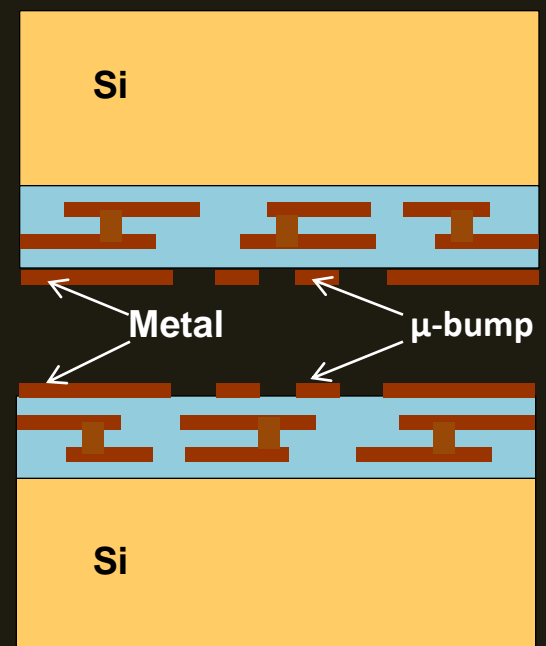
Selection of Wafer/Chip bonding technology



Polymer adhesive bonding

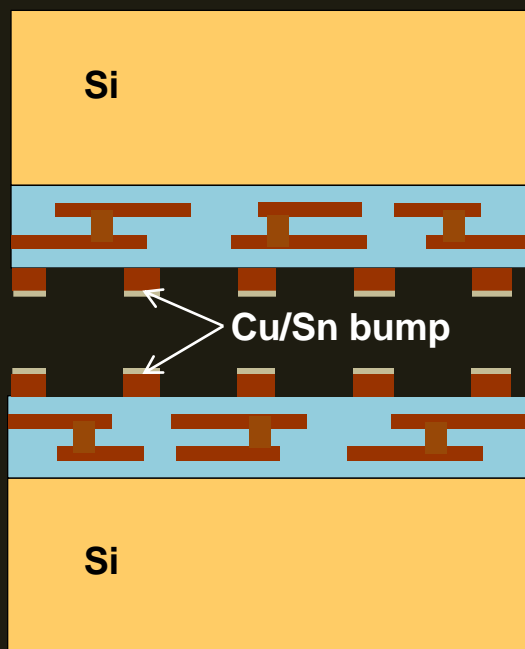


SiO₂ fusion bonding

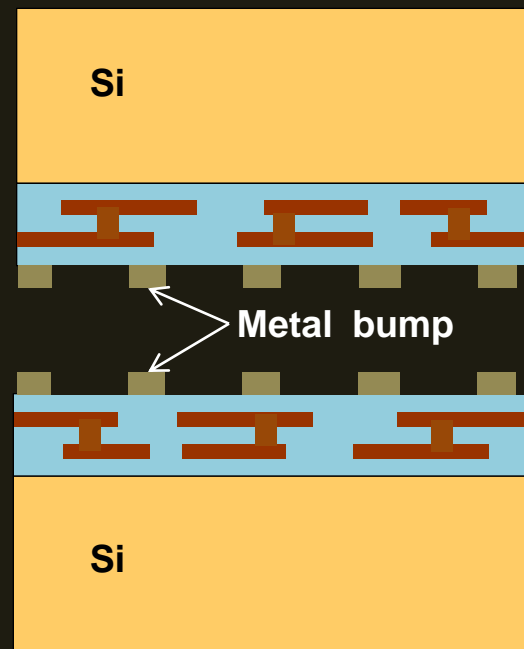


Metal fusion bonding

Selection of Wafer/Chip bonding technology (2)



Metal eutectic bonding



Bumping (Pb/Sn, Au, In)

Yield model

Yield Model of LSI

$$Y = Y_0 \cdot Y_1(D_0, A, \alpha)$$

Y_0 : Systematic yield

Y_1 : The fraction of chip sites without process related effects and circuit sensibility

A : Chip Area

D_0 : Density of defects

α : Distribution parameter of defects

Defect source

- **dusts or other particles in the environment, solution, process chamber in the production equipment**
- pattern defects due to ununiformity of material
- oxide defects caused by process damage
- statistical factor
- etc.

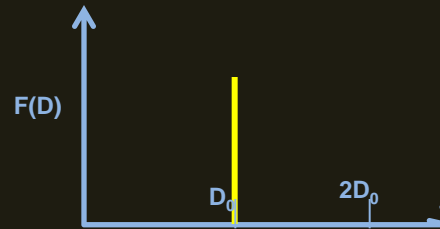
Yield model

Y_n : The fraction of chip sites without process related effects and circuit sensibility

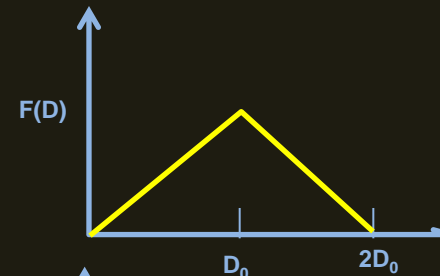
A : Chip area

D_0 : Density of defects

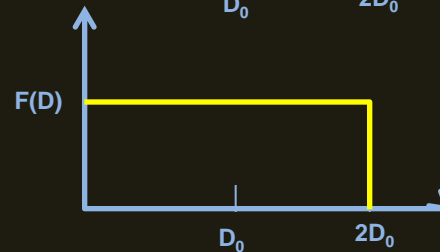
$$Y_1 = \exp(-D_0 A)$$



$$Y_2 = \left[\frac{1 - \exp(-D_0 A)}{D_0 A} \right]^2$$

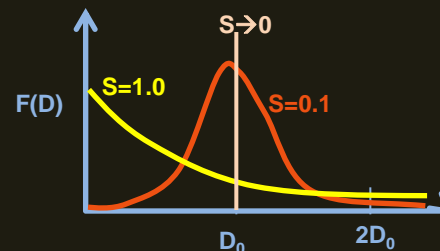


$$Y_3 = \frac{1 - \exp(-2D_0 A)}{2D_0 A}$$

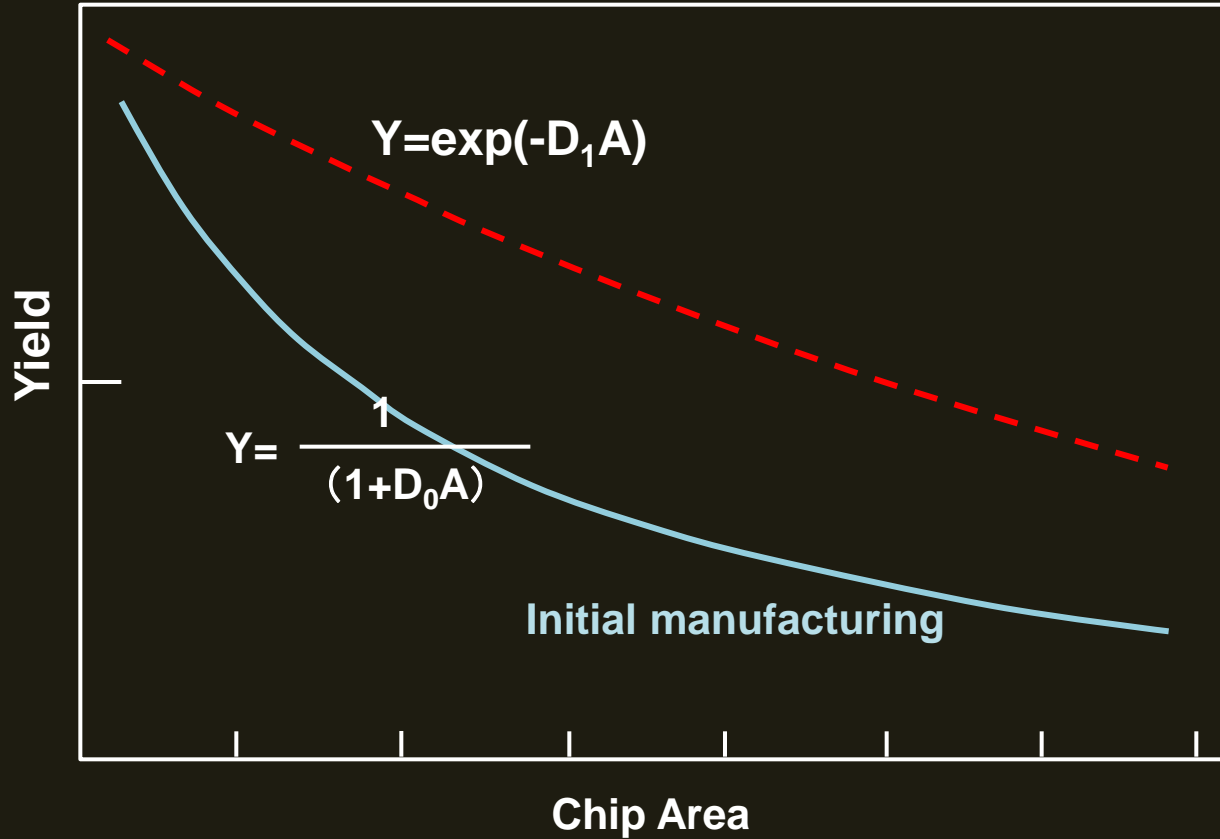


$$Y_4 = \frac{1}{(1 + S D_0 A)^{1/S}}$$

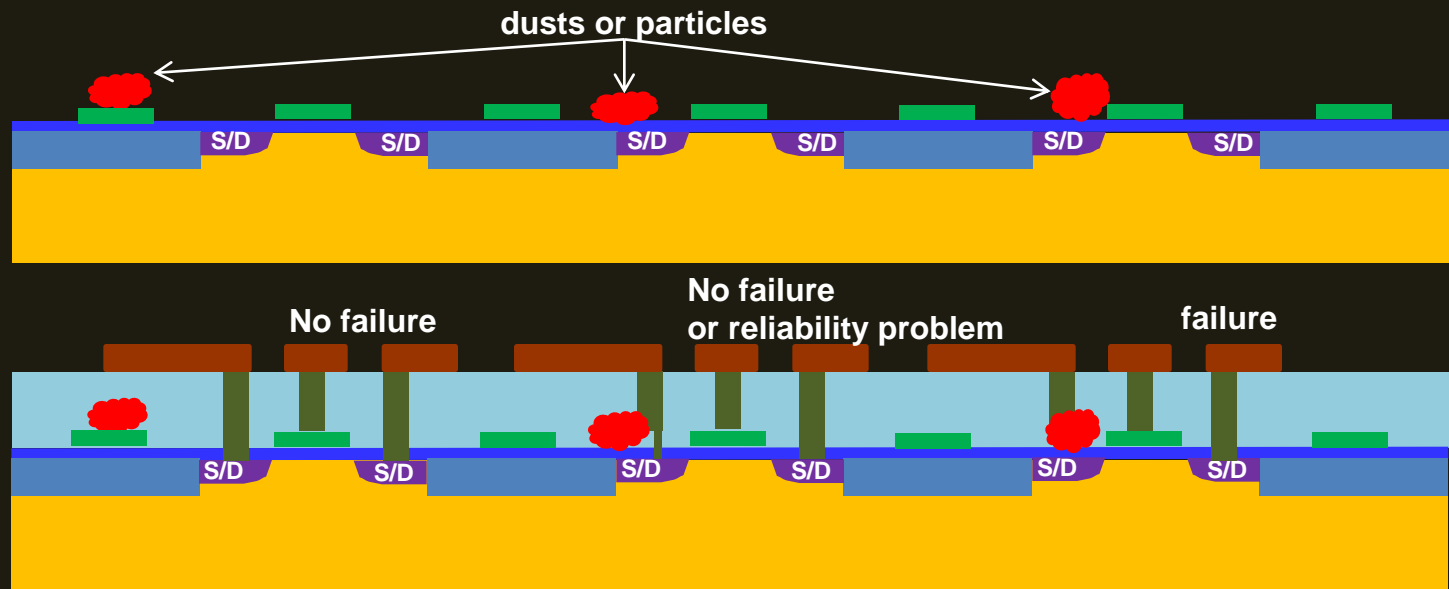
S : shape parameter



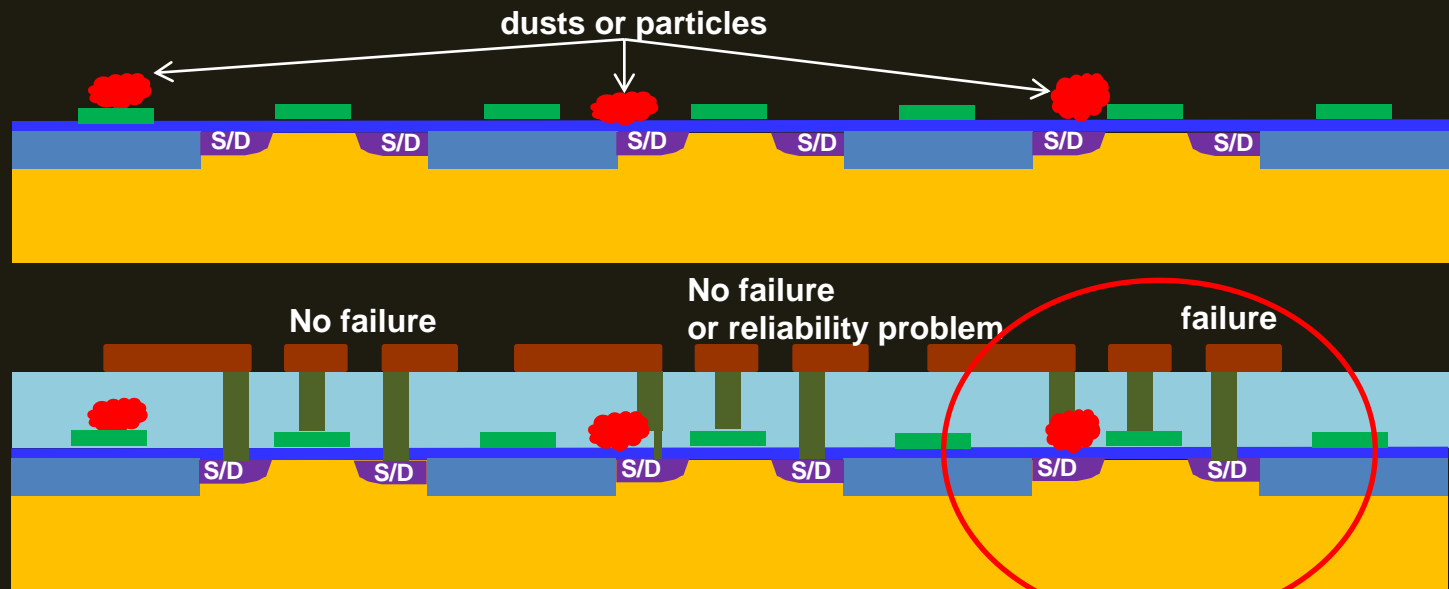
Yield Prediction



Yield and reliability

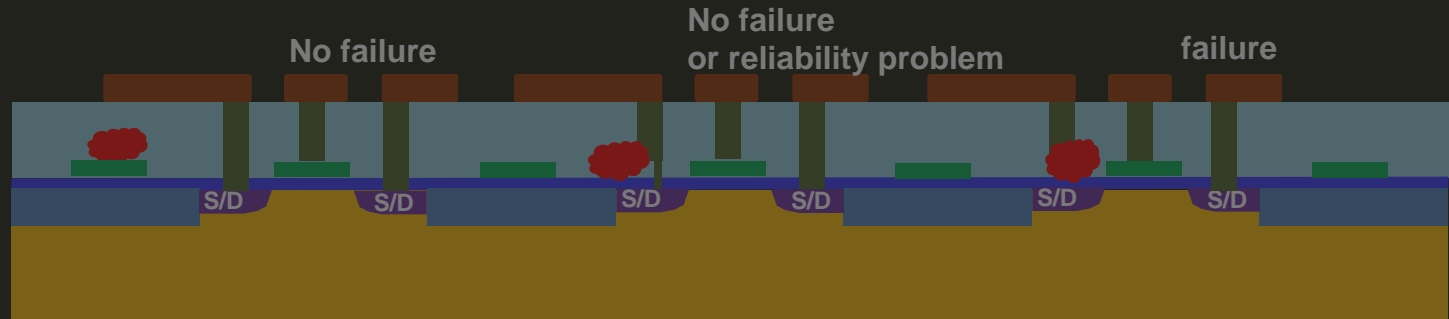
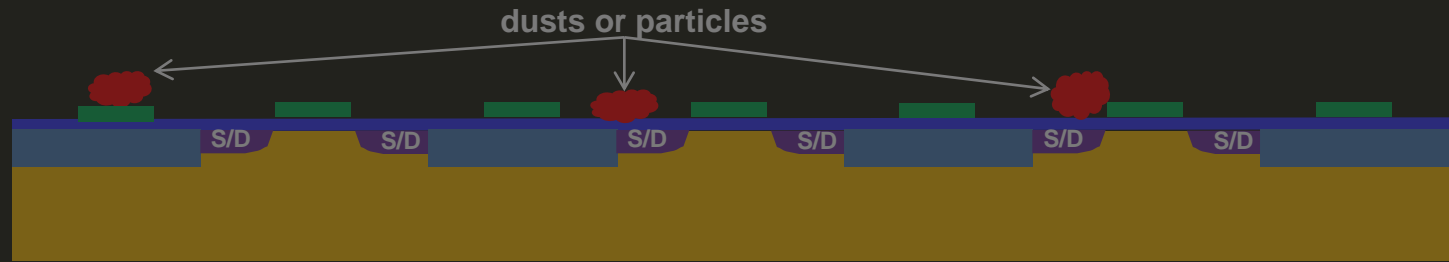


Yield and reliability



We can only detect this failure from electrical testing.

Yield and reliability



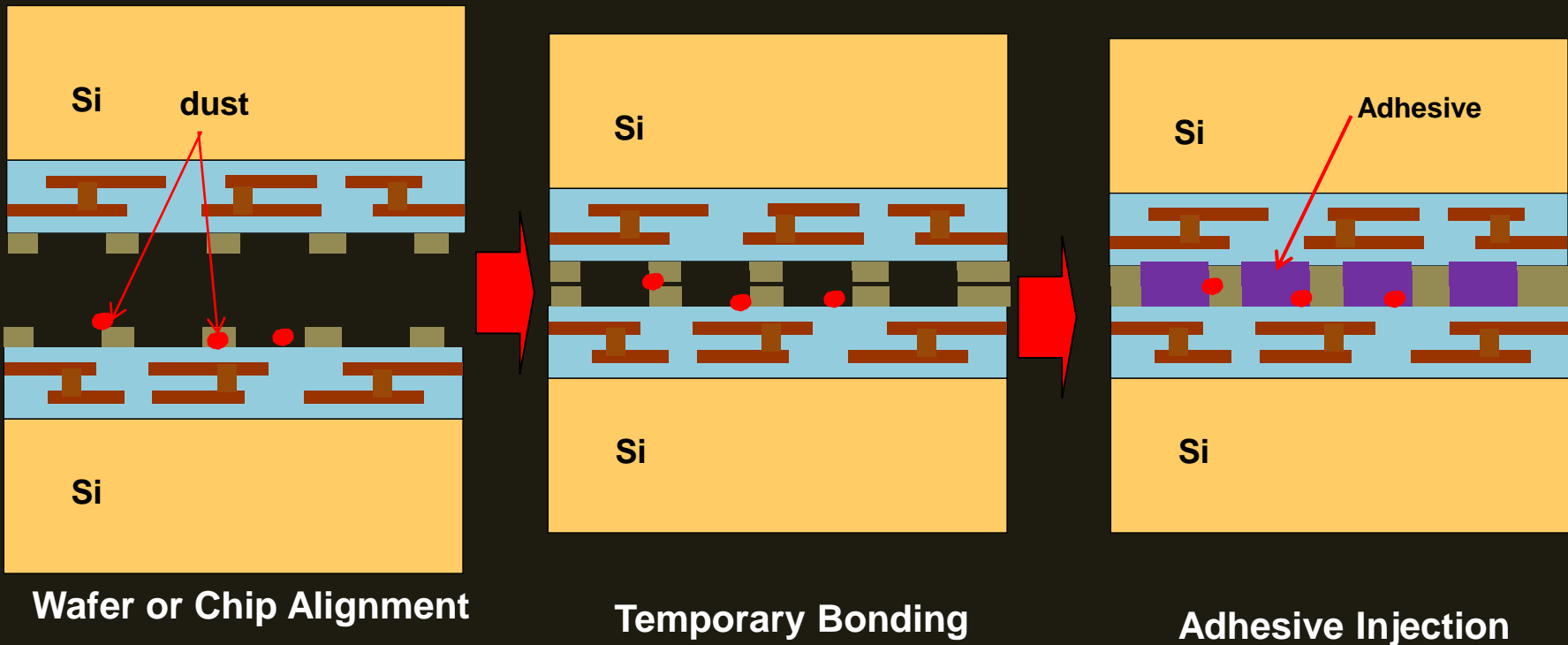
In case of bonding wafer/chip on wafer /chip surface with dust,



If the bonding method which needs microscopic smoothness and cleanliness, bonding yield will be affected by defect density of dusts and particles. So we have chosen the bump bonding with adhesive injection.

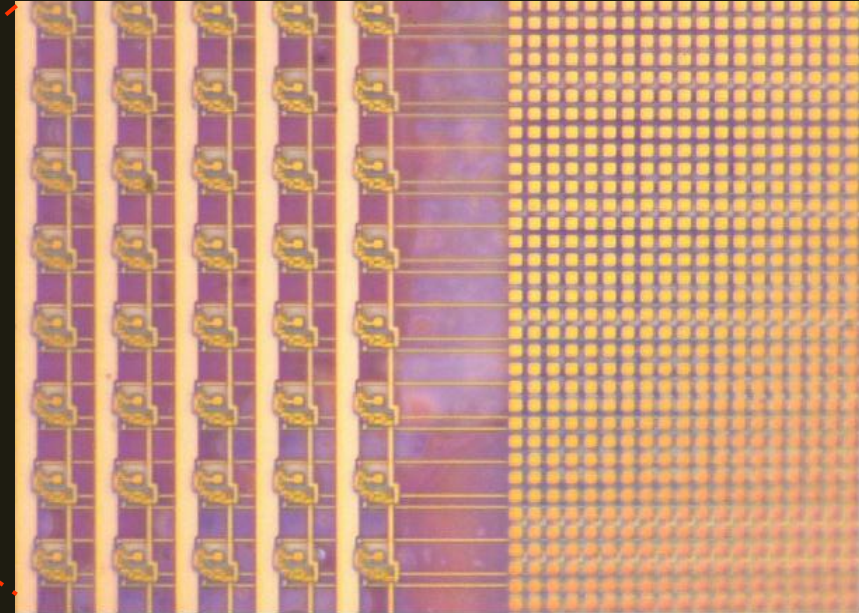
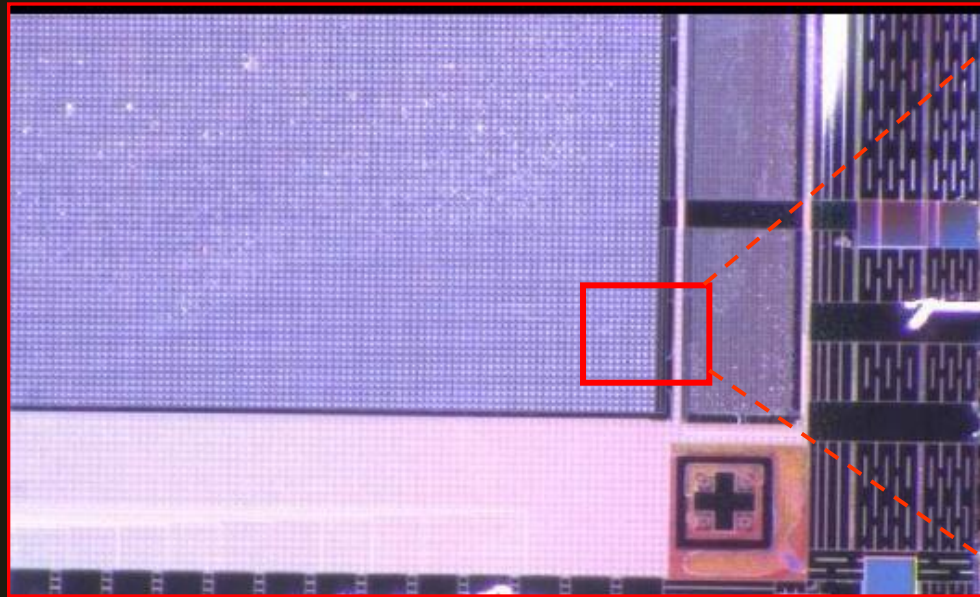
Wafer Bonding Method (Tohoku University/T-micro)

Bump size ($\sim\mu\text{m}$) \gg dust or particle size ($\leq 0.2\mu\text{m}$)



In μ -bumps do not have enough mechanical strength, so the combination use of adhesive is indispensable.

SOI pixel detector Chip After Si removal



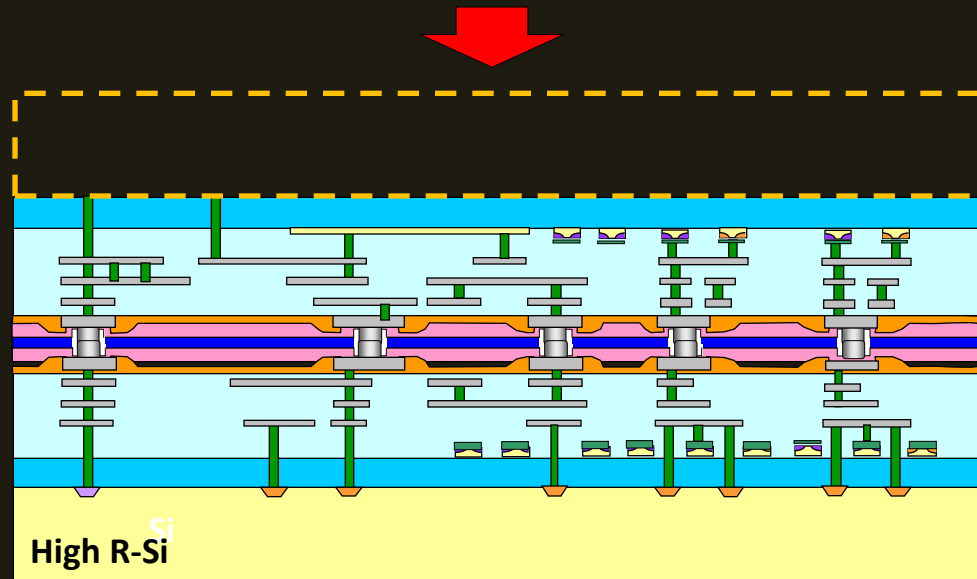
Detector Array /Peripheral Circuits



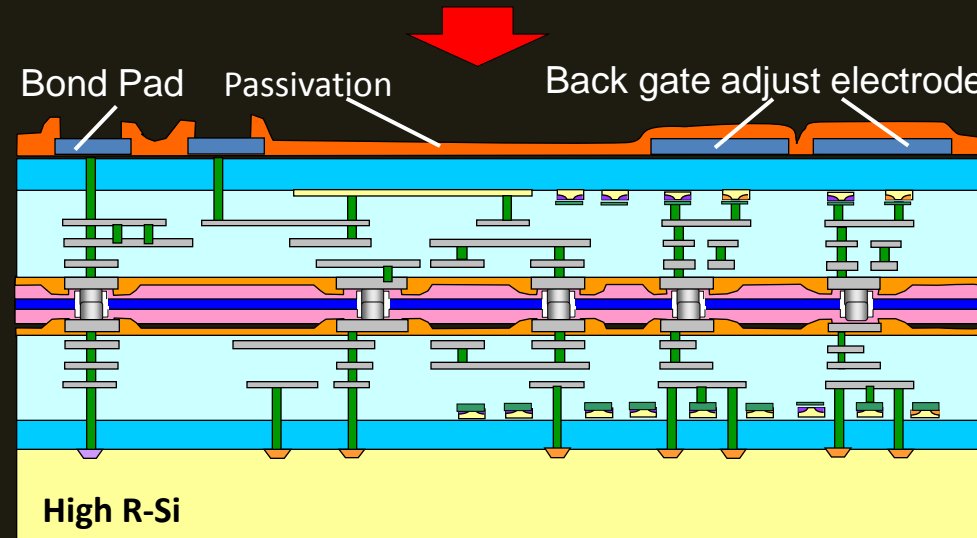
Voids

Process flow (2)

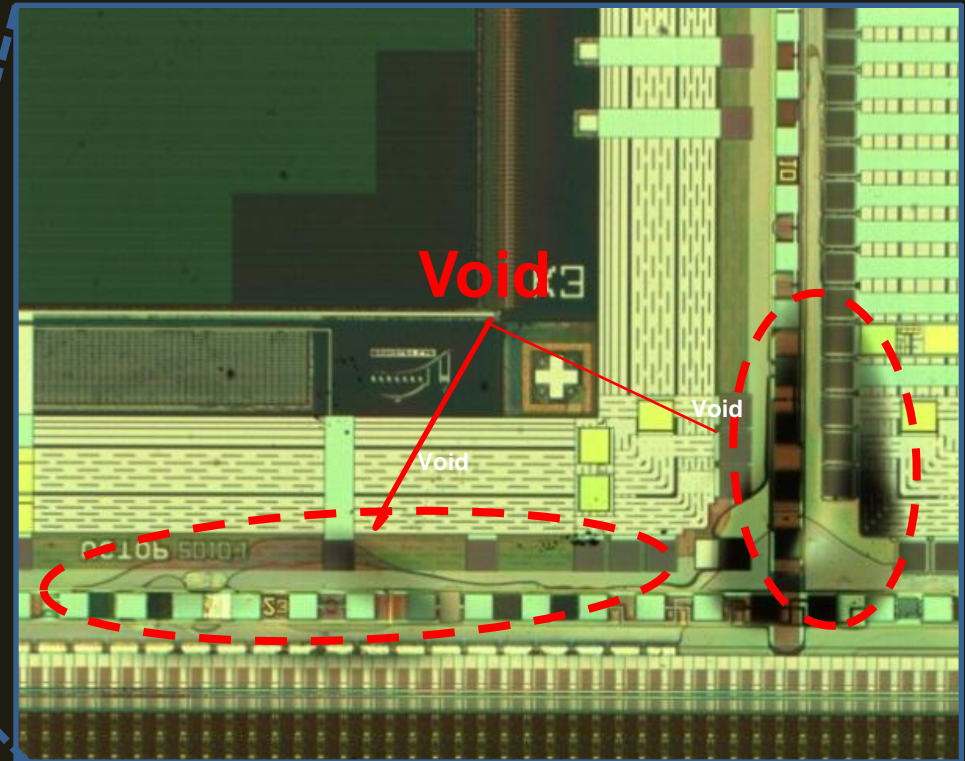
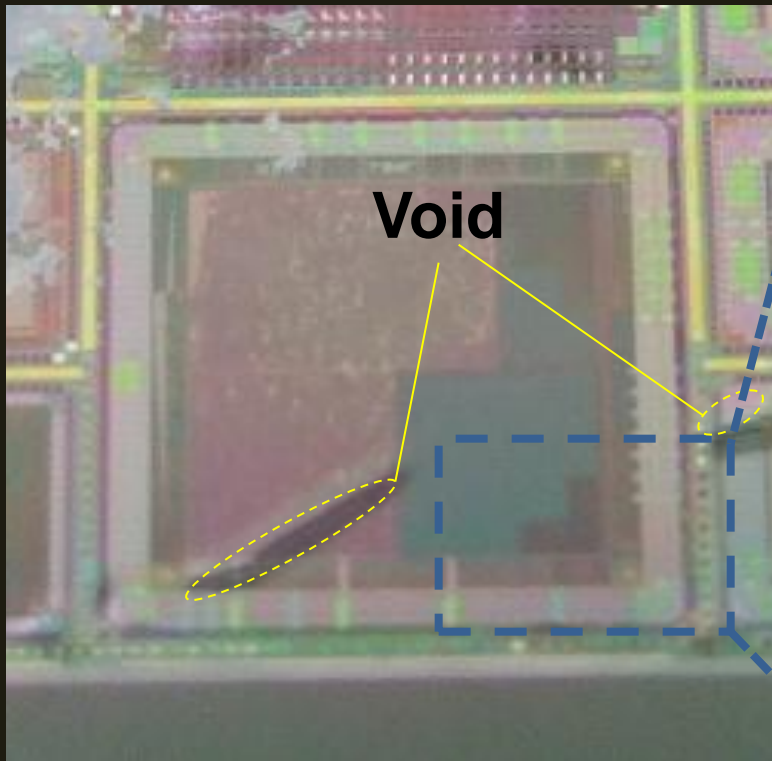
(d) Bulk-Si removal



(e) Pad patterning and passivation

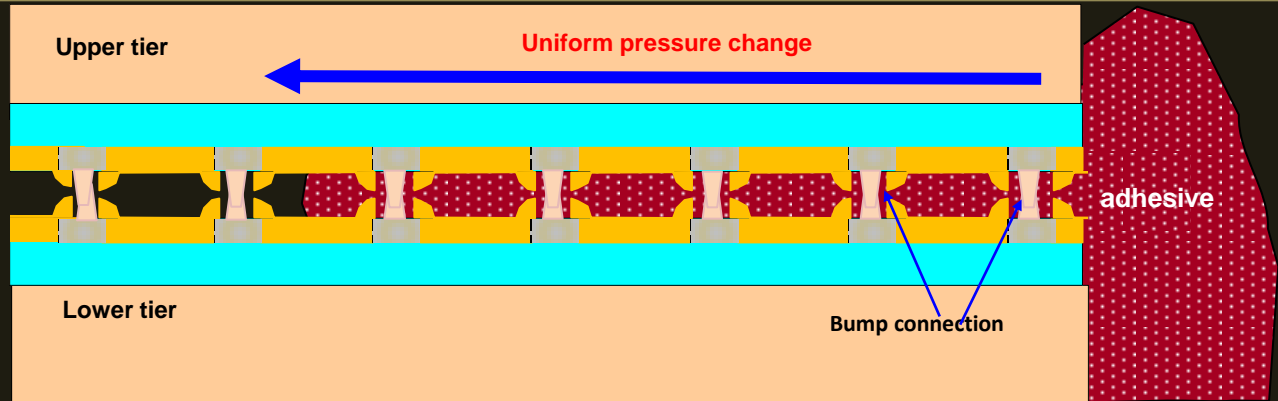


Void problem

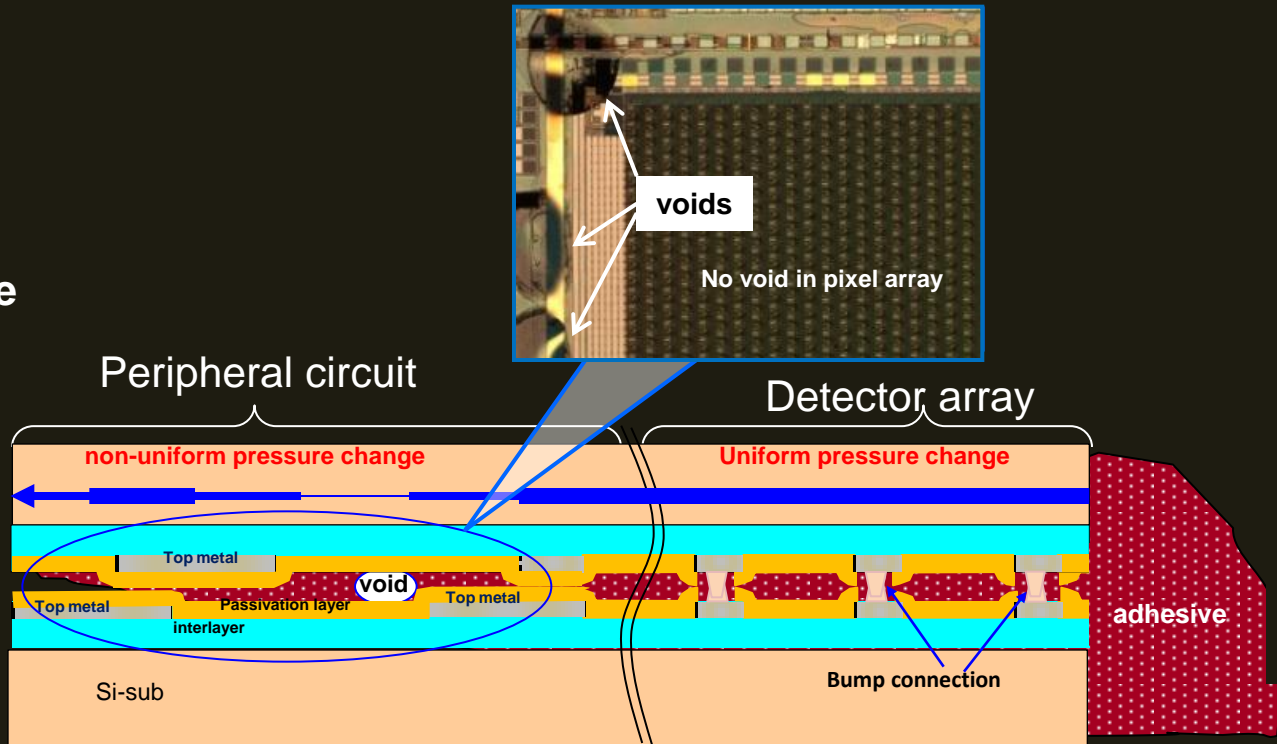


Mechanism of void formation (1)

(a) Simple test device



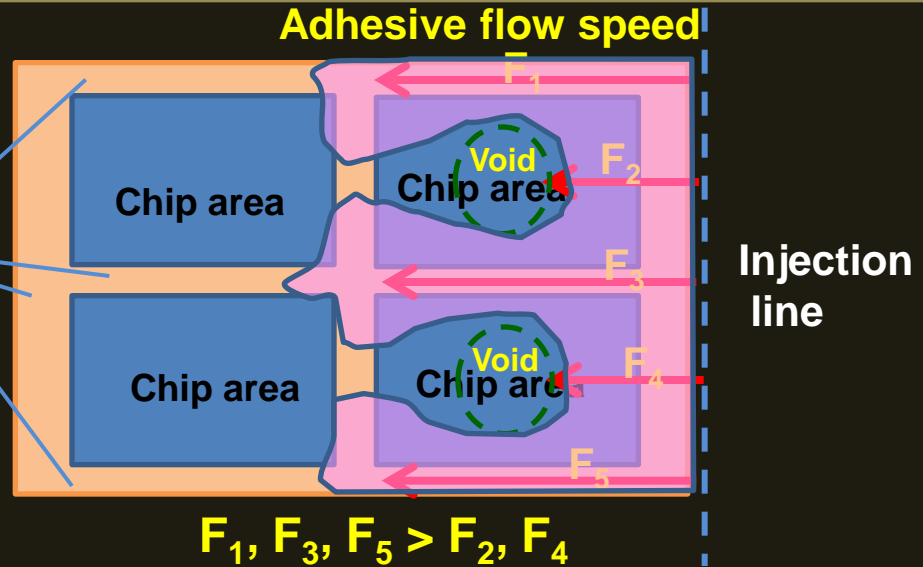
(b) Circuit test device



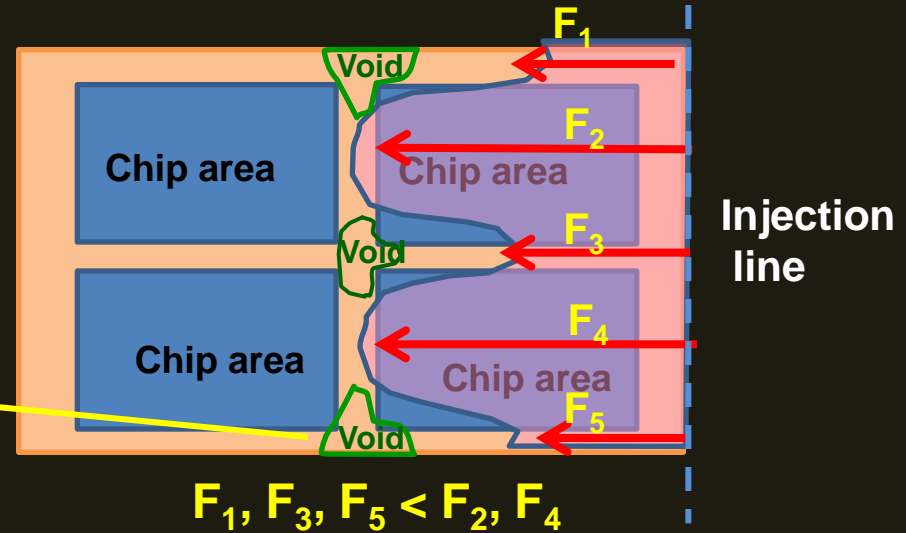
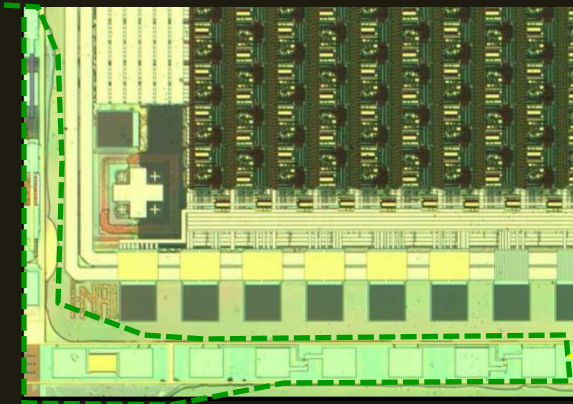
Mechanism of void formation (2)

Pumping action > capillary action

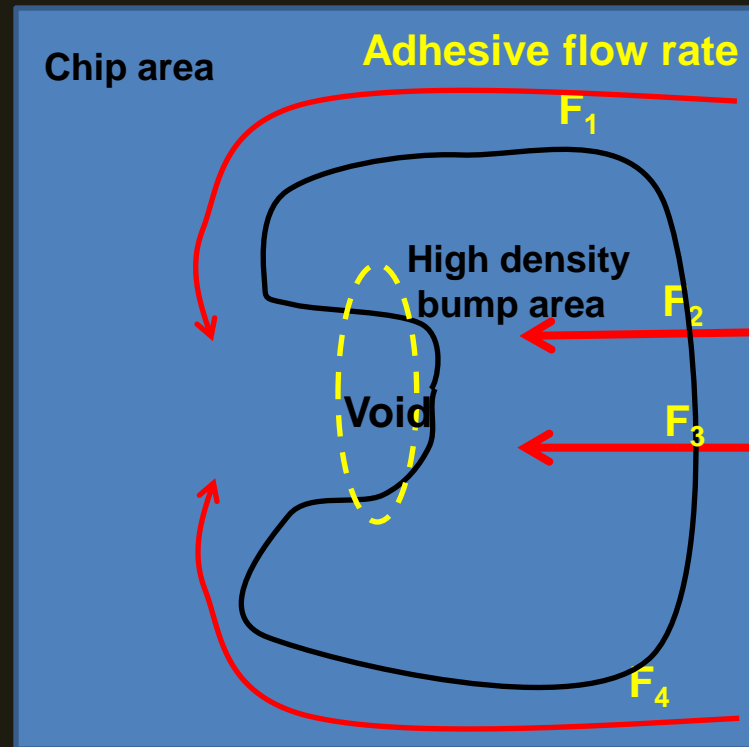
Scribe line



Pumping action < capillary action

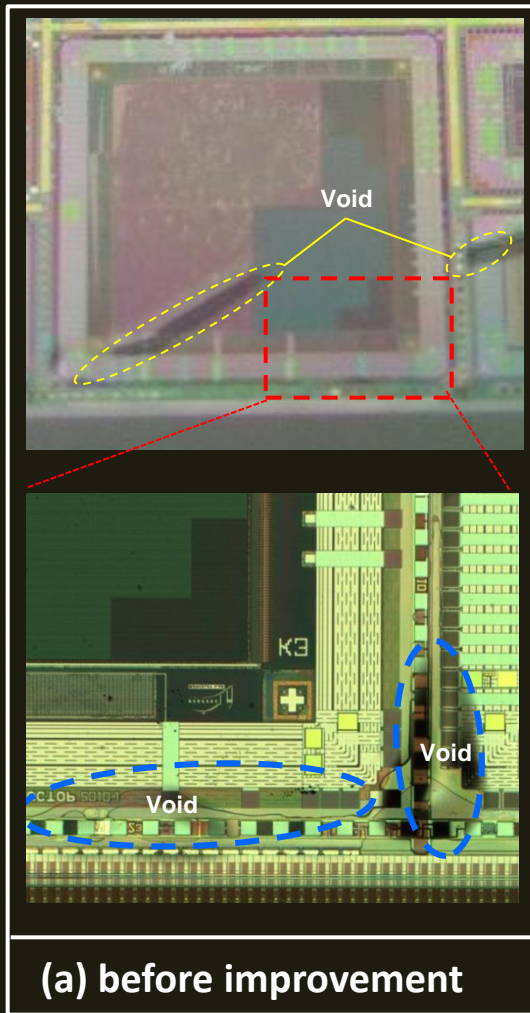


Mechanism of void formation (3)



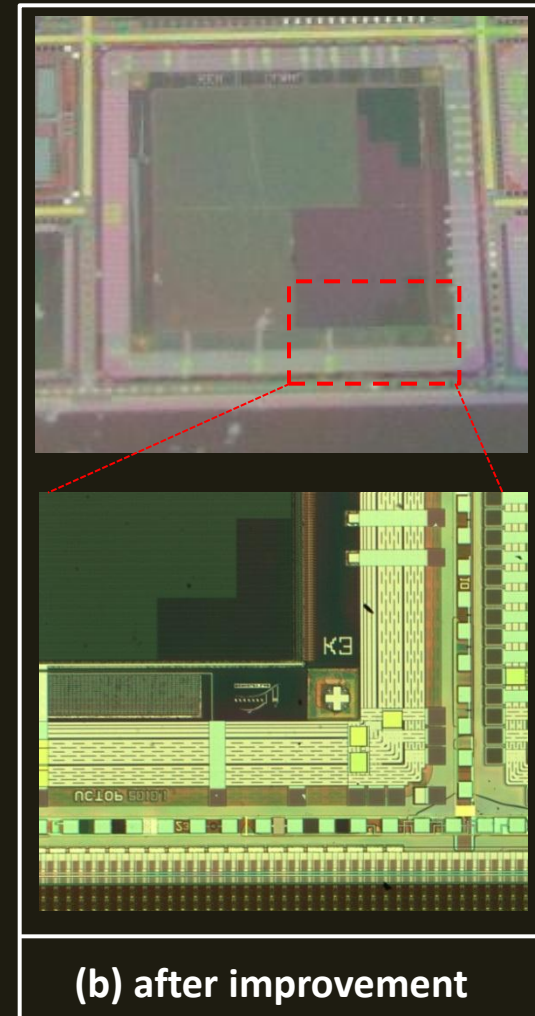
$$F_1, F_4 > F_2, F_3$$

Pixel detector chip after Si removal

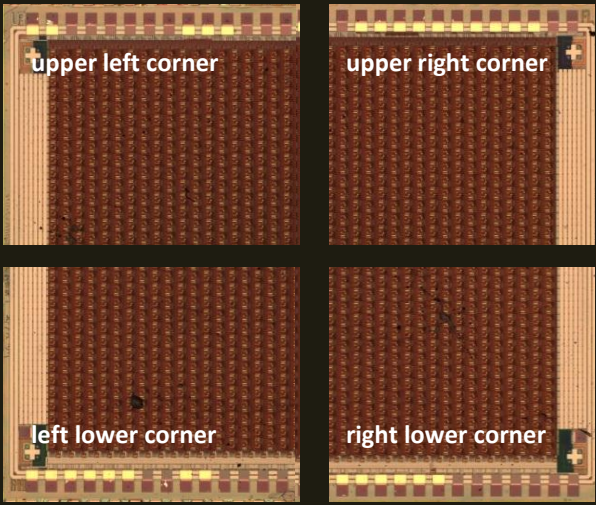
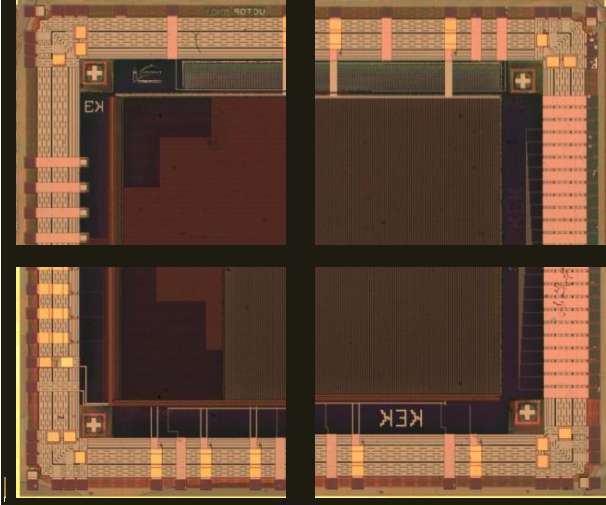

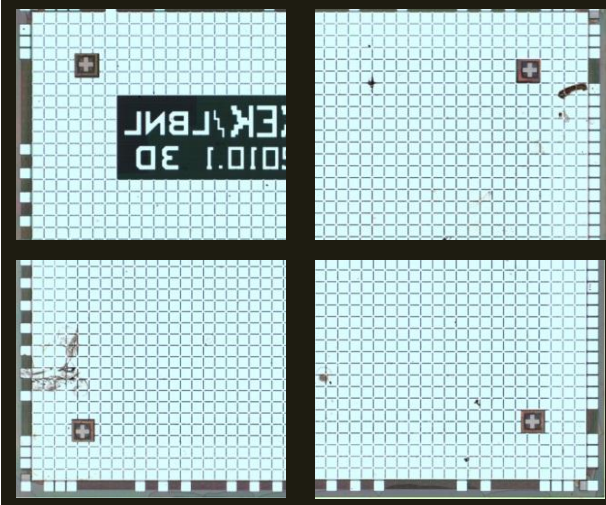


Optimize

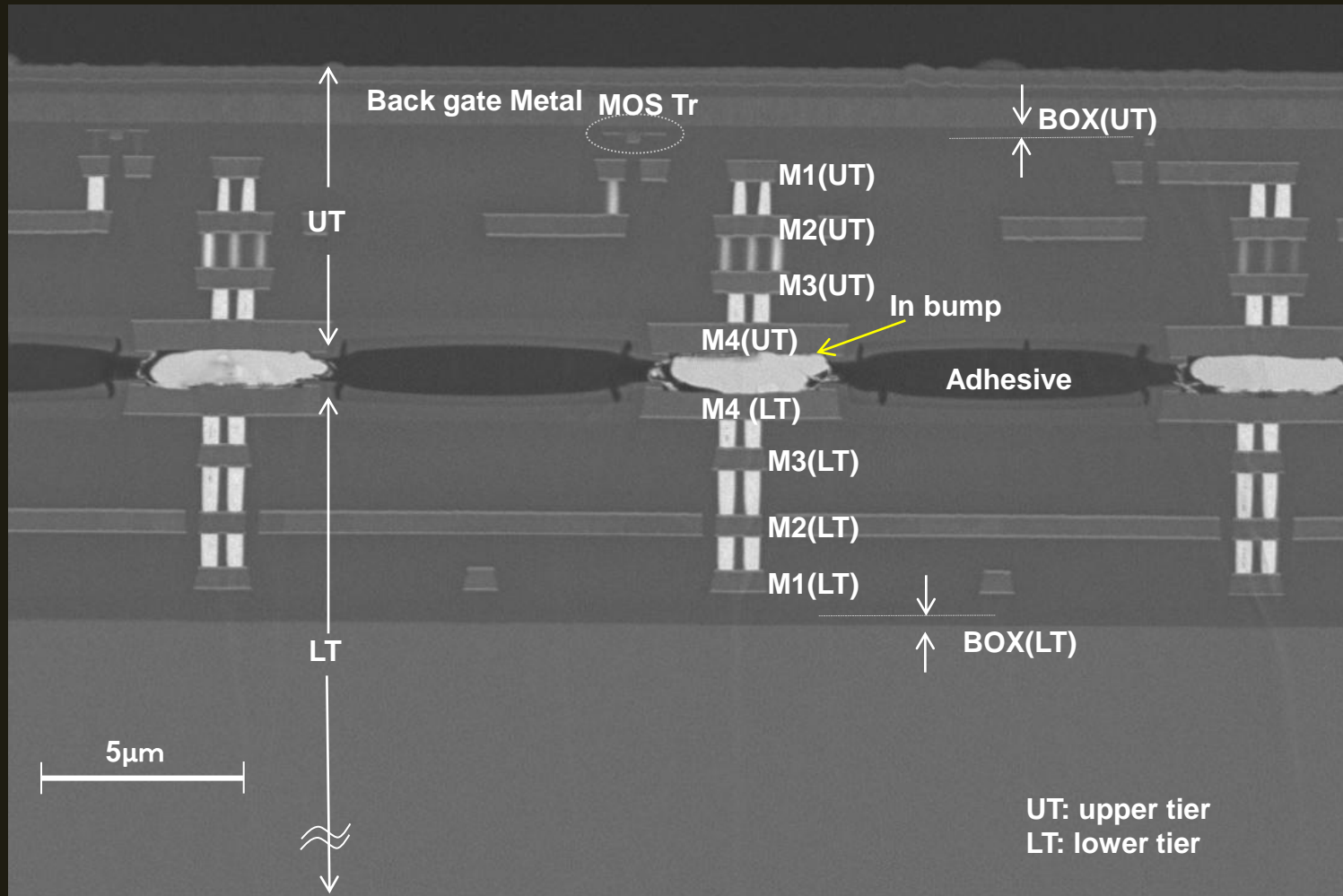
- bump layout
- differential pressure of adhesive injection
- process temperature (control the viscosity of adhesive)
- wettability of adhesive

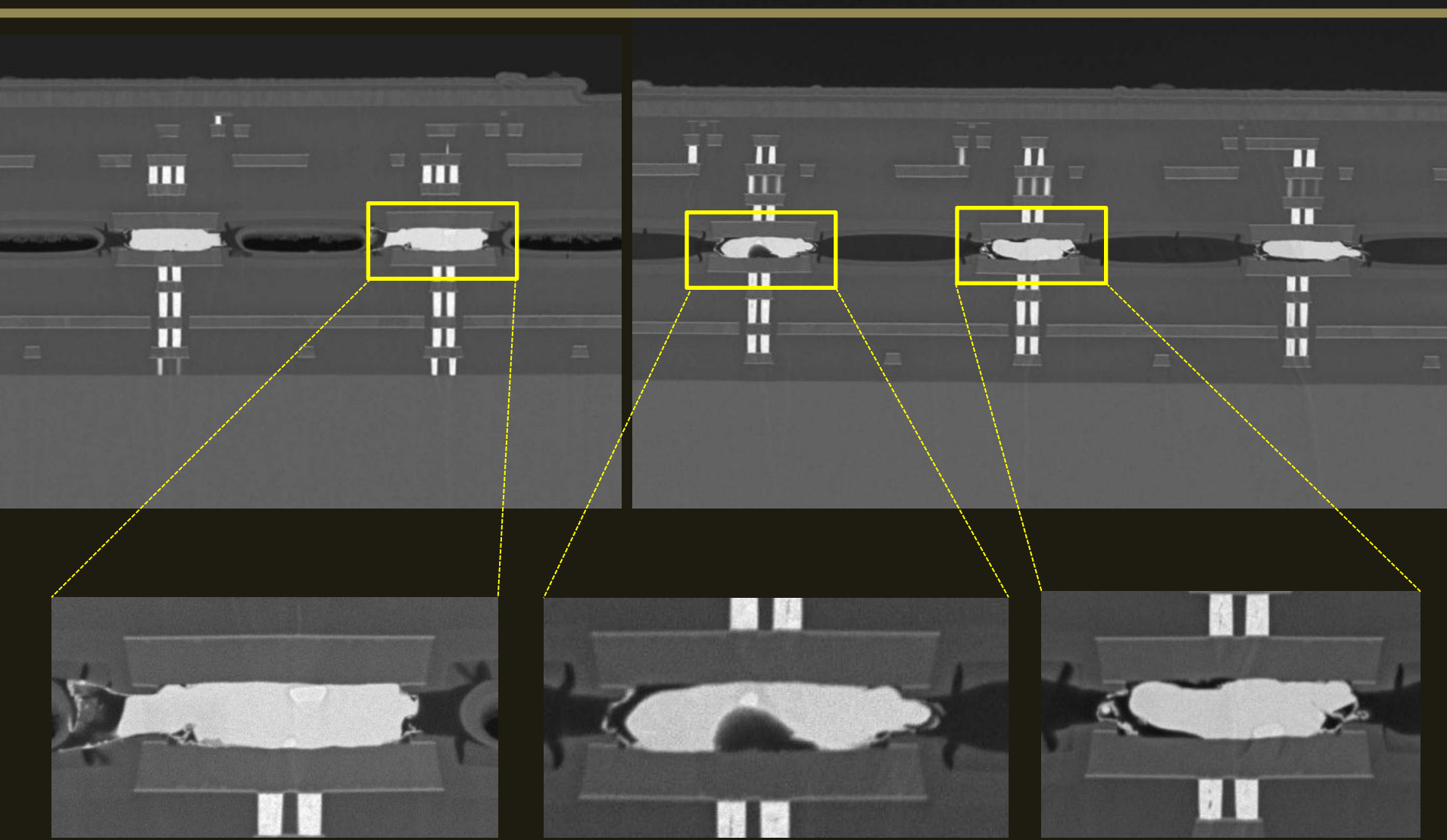


Two types of pixel detector chip

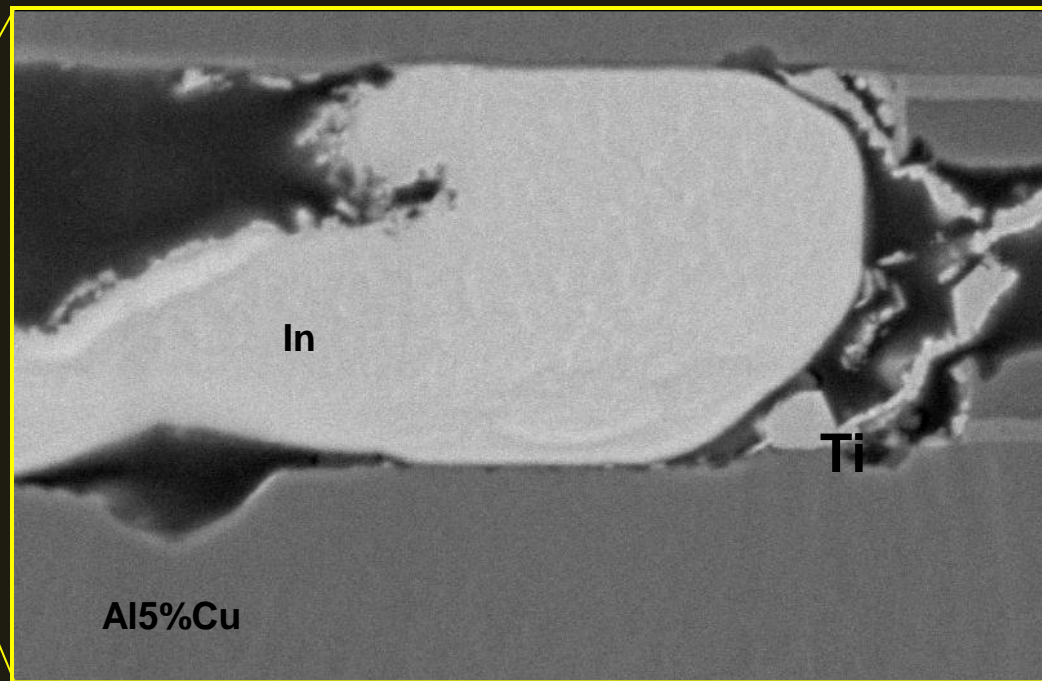
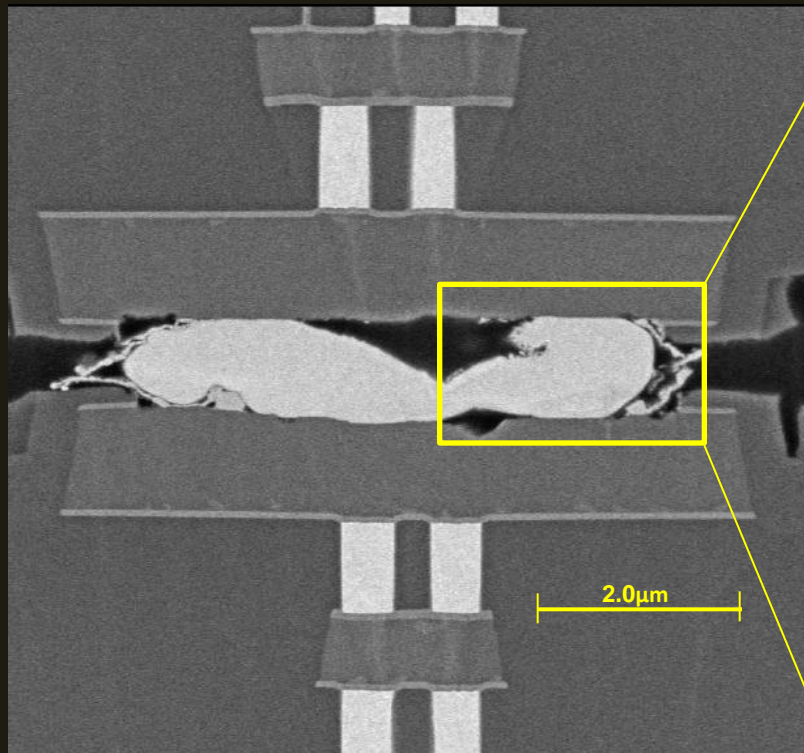
	A pattern (5mm x 5mm)	B pattern (5mm x 5mm)
after Si removal		
Finished Chip		

Cross sectional SEM image of pixel array

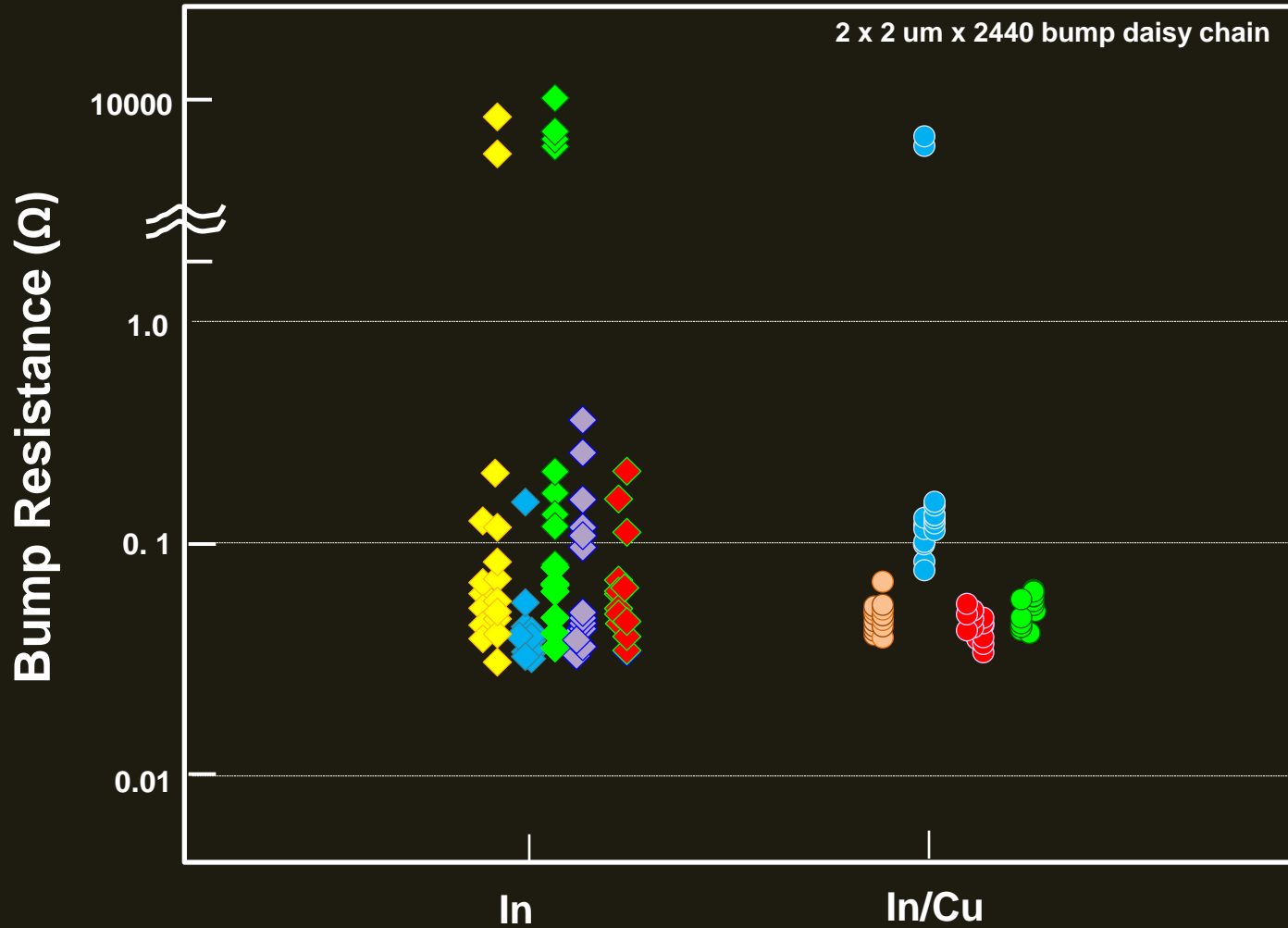




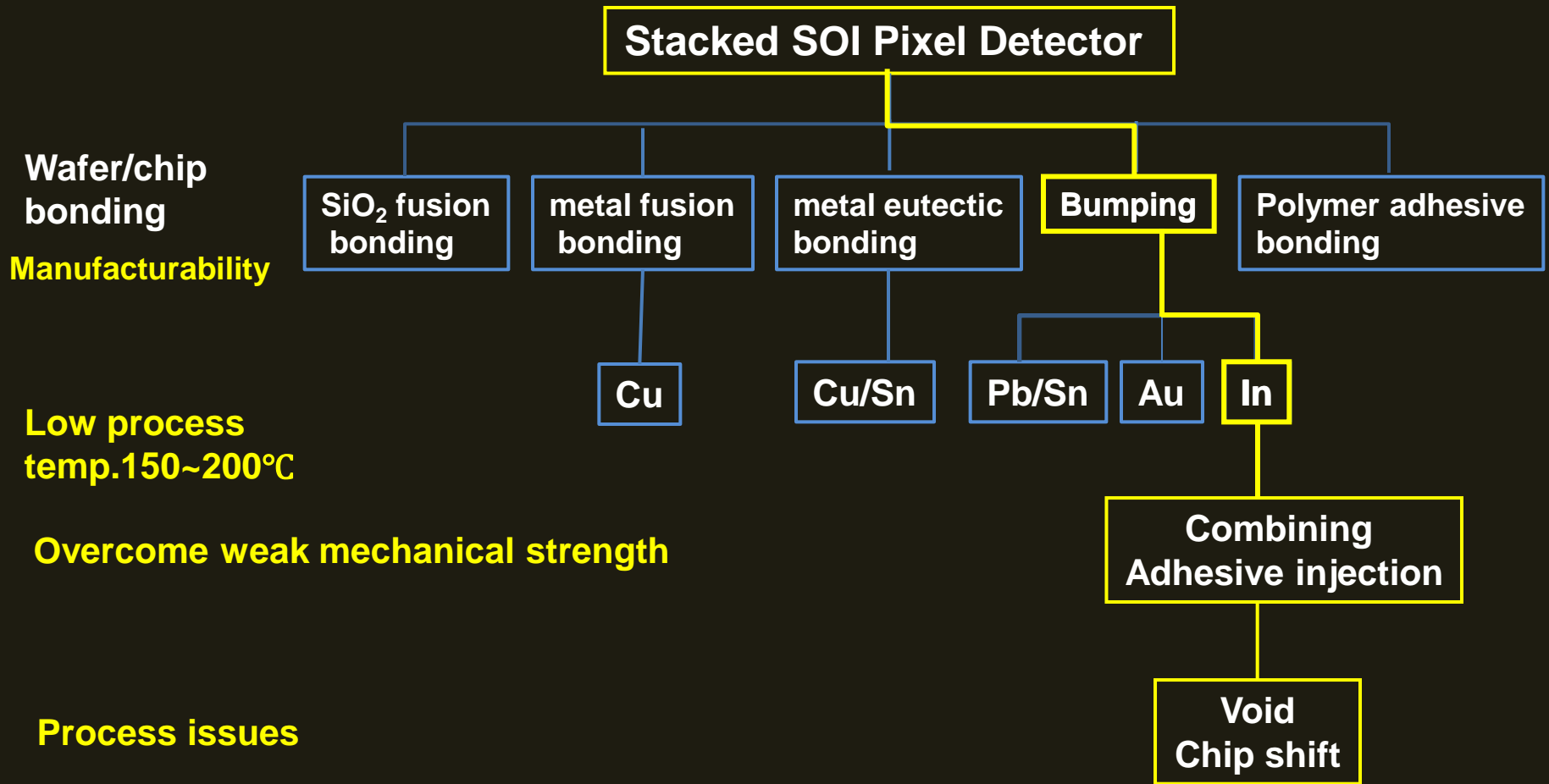
Poor wettability



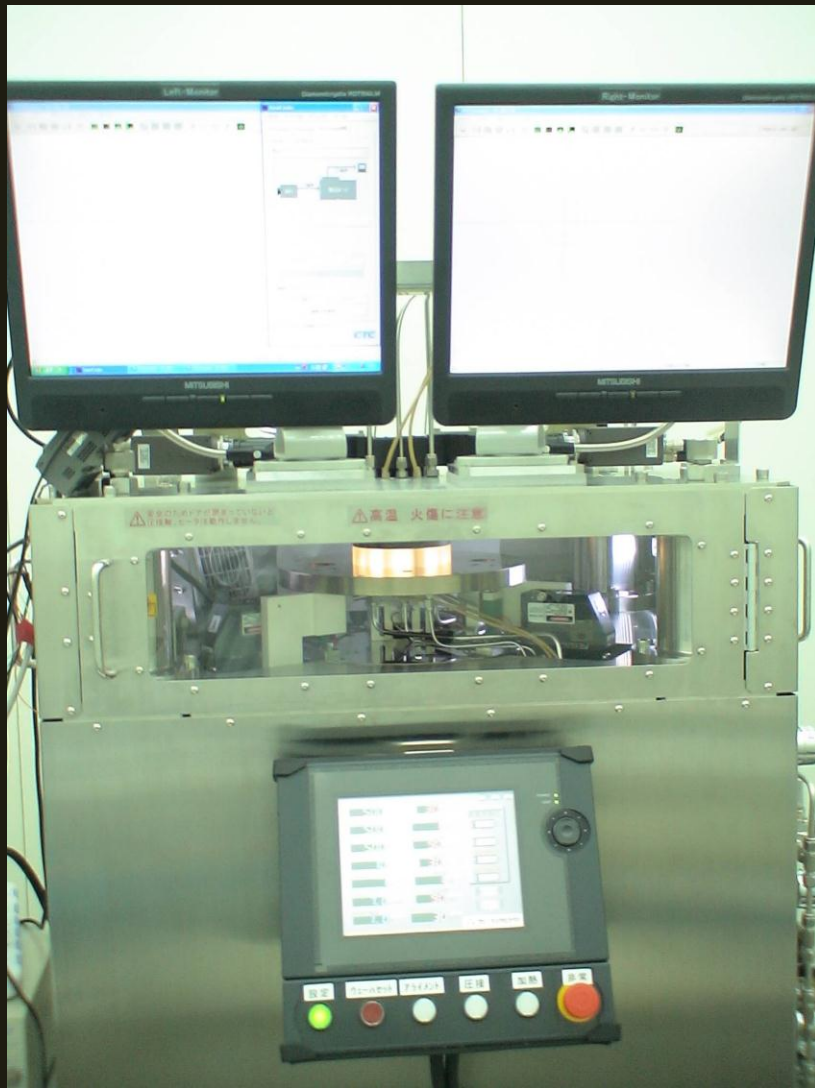
In bump vs In/Cu bump



Summary-Technology selection chart



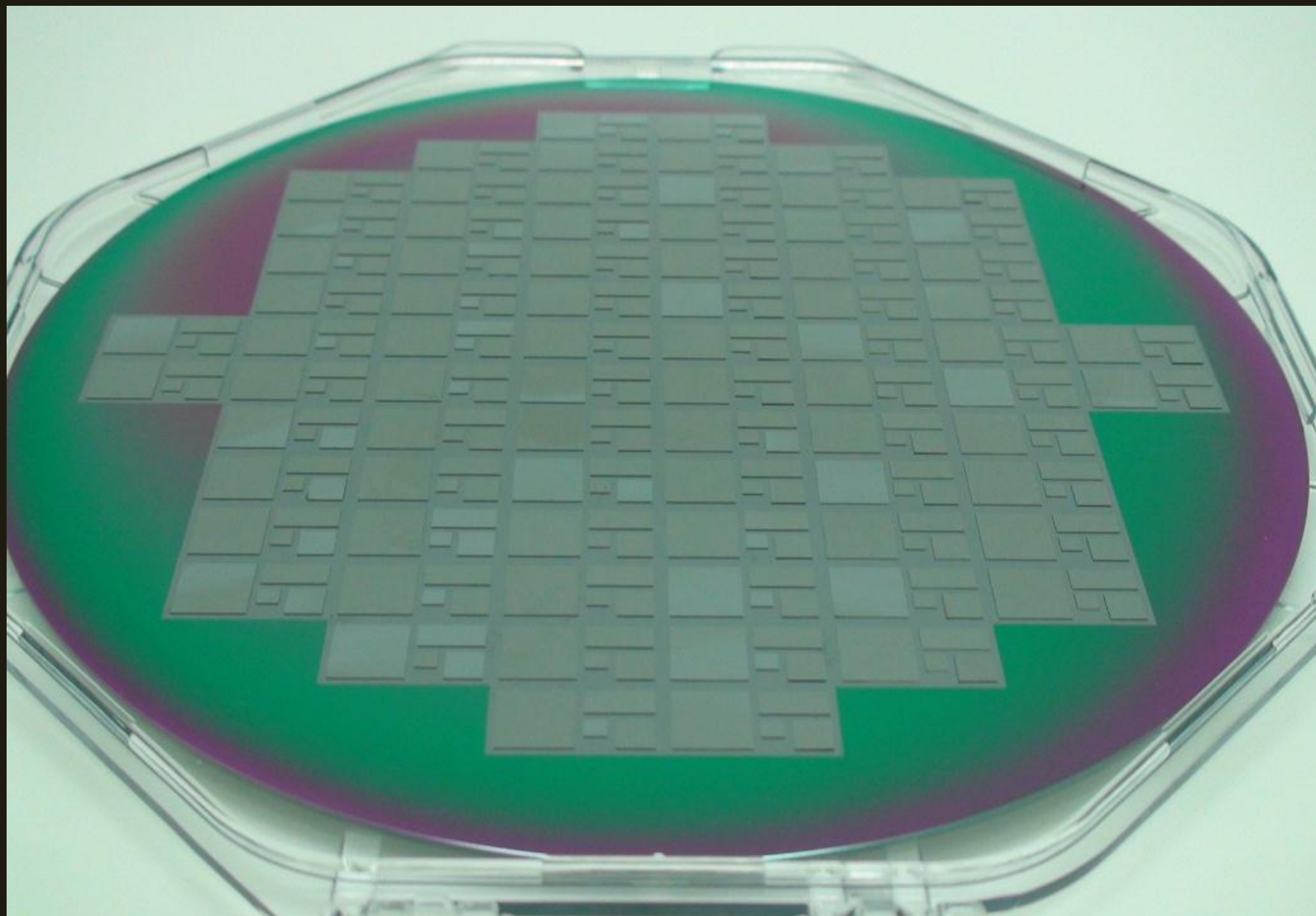
Prototype of 8" Self-Assembled Chip Bonder



Self-Assembly Process with 8-inch Wafer



Alignment accuracy: ~ 400 nm



200 mm

図4 試作製造装置で多数のチップを仮接着したウェーハの全体写真

Conclusion

- **3D LSI Integration technology using minimum 5 μ m pitch bump is verified using SOI stacked pixel detector as circuit level test device.**
- **In this technology, adhesive injection is found the key technology. Optimizing layout, process parameter and adhesive injection method, this process have completed without void.**
- **The dispersion of bump resistance is still high, the following optimization are still ongoing.**
 - Improvement of wettability between bump and pad**
 - Introducing the new Cu/In IMC bonding**
- **In further development of wafer /chip bonding with few μ m pitch bump , it might be necessary to optimize the gap between tiers and volume of bump metal.**