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3D Integration for SOI Pixel Detector

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Abstract
Large-scale integration (LSI) technology in two dimensions has been the norm over the past three decades. However, the industry is now rapidly moving into the era of sub-20-nm nodes, and continuation of the present scaling trend will require the introduction of new transistors with three-dimensional (3D) structures and new materials and processes. This is expected to dramatically increase the development and manufacturing costs for systems-on-a-chip. 3D-LSI is one solution that can mitigate cost increases without degrading device performance. Consequently, many methods to realize 3D-LSI devices have been developed by focusing on the unit processes of 3D-LSI technology: (1) through-silicon via (TSV) formation, (2) bump formation, (3) wafer thinning, (4) chip/wafer alignment, and (5) chip/wafer bonding. However, these unit processes are incompatible in terms of various device and process requirements such as process temperature, device structure, TSV and bump dimensions, yield, reliability, and supply chain. For example, the simplest 3D pixel detectors are two-tile face-to-face stacking devices with fine-pitch μ-bump bonding, which requires bump formation, wafer thinning, accurate chip/wafer alignment, and chip/wafer stacking. For bump connection, several reported methods are available, such as Cu–Cu bonding, intermetallic-compound bonding with Cu/Sn bumps, and Au bump bonding. Cu–Cu direct bonding can provide a good and robust connection, but needs completely clean and flat surfaces. This would necessitate a dust-free environment, which is difficult to realize in practice for wafer/chip stacking with bump bonding. Therefore, although theoretically there might be many combinations of these five unit processes, the combinations do not a device structure with good yield, reliability, and cost. This study investigated the optimal combination of unit processes for manufacturing the SOI stacked pixel detector chip that has been designed by KEK. Stacking was accomplished with 2.5 μm × 2.5 μm In bump connections and adhesive injection at low temperature (less than 200℃). It was found that the stacking process is affected by the layout of each tier, that adhesive injection is the key technology, and that these effects could be minimized by optimizing the layout, process parameters, and device structure. Another concern in manufacturing the pixel detector is suppressing metal contamination. Some metals such as Au, Fe, and Pt form intermediate energy level between the conduction and valence bands of Si and act as life-time killer. Cu is used as a wiring material and bump material in 3D devices. However, Cu diffuses into Si crystals and SiO2 even at room temperature, increasing the leak current of pn junctions and deteriorating the oxide quality of MOS transistors. In our 3D integration using In bumps, Au is used to protect In from oxidation. Hence, optimizing the UBM (under bump metallization) layer is important. Therefore, we also studied the device characteristics with different UBM materials.

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