VERTEX DETECTORS FOR FUTURE LINEAR COLLIDERS

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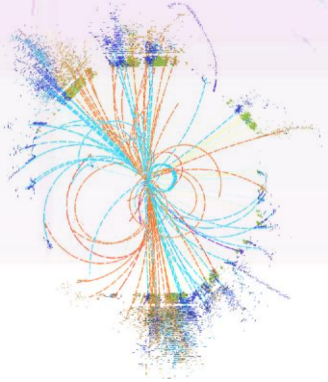


Outline

- The future linear collider projects
  - The Compact Linear Collider (CLIC)
  - The International Linear Collider (ILC)
- Vertex detector requirements in linear colliders
  - Physics requirements
  - Impact on vertex detector design
- The detector concepts
- Sensor technologies
- CLIC R&D for vertex detector instrumentation

Future linear collider projects

Future linear colliders are e+ e- colliders aiming at performing precision measurements of Standard model (SM) and beyond SM parameters

Beam Parameters	CLIC	ILC
Technology	2-Beam acceleration scheme	Superconducting RF cavities
Beam energy	Few hundred GeV to 3 TeV	Few hundred GeV to 1 TeV
Train rate (Hz)	50	5
Train length (us)	0.156	910
Bunches per train	312	1300
Bunch separation (ns)	0.5	700
Train separation (ms)	20	200
Duty Cycle (%)	0.00078	0.45

Vertex detector requirements in linear colliders

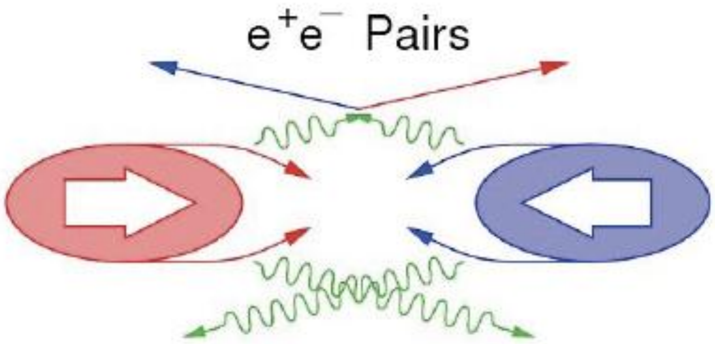
- **Single-Point Resolution** (σ_{sp}=3-5 um) requirements for vertexing and charged particle impulsion measurements
  - ➢ Very low sensor thicknesses (~0.1% per layer, ~100 um of Silicon) to reduce multiple scattering
  - ➢ Pixel size ~O (20x20 um)
  - ➢ Air cooling to reduce inactive material

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3 \theta)}$$

$$a \approx 5\mu m \quad b \approx 15\mu m$$

Single Point Resolution **Multiple Scattering term**

- **Timing** of single hits with a resolution of ~10 ns (CLIC) for reduction of beam background-induced hits



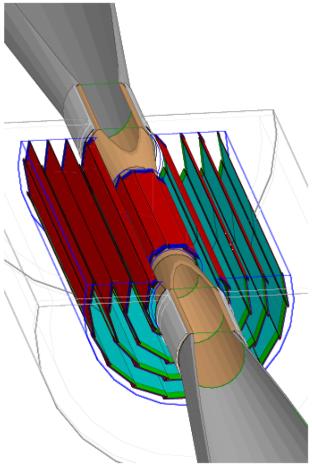
Beam-induced Background

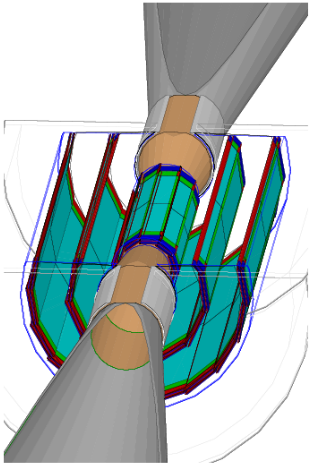
- **High Granularity** to reduce occupancy and reduce probability of double hits
  - Low power electronics (~ 2uW/channel)

The ILD and SiD Detector Concepts

International Large Detector (ILD)

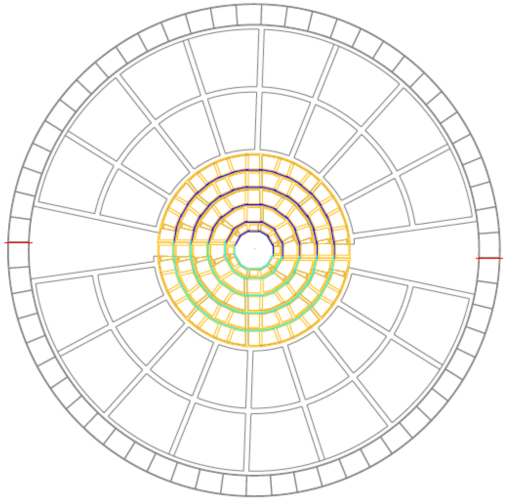
- 4T Magnetic Field
- TPC-based tracking in the outer tracking region
- Two vertex detector concepts VTX-SL and VTX-SL
- Annual dose in excess of 1kGy and fluence of 10^{11} 1-MeV n_{eq}/cm^2





Silicon Detector (SiD)

- 5T Magnetic field
- All-Silicon vertexing and tracking
- Silicon only in the IP region with vertex supported only at extremities

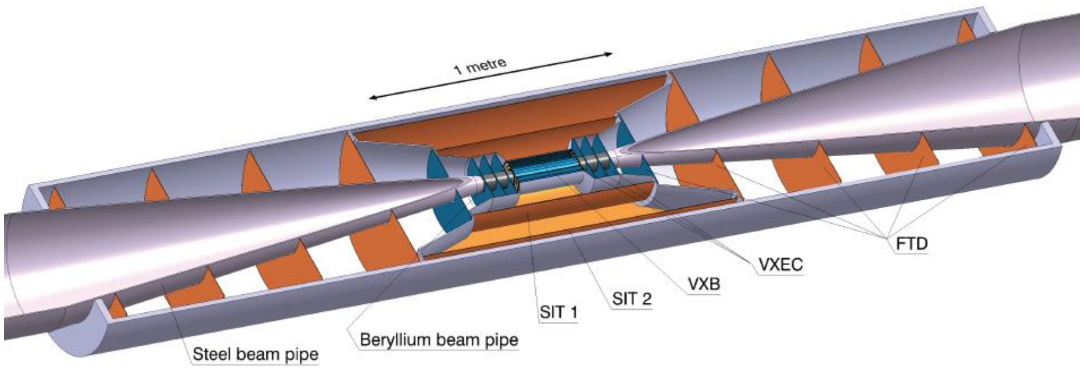


CLIC_SiD and CLIC_ILD

The CLIC versions of SiD and ILD detectors are modified to take into account the different bunch train structure:

- Beam pipe pushed at outer radius to avoid high occupancy from beam background
- Power consumption must be reduced by means of Power-Pulsing to take advantage of the small duty cycle associated to the beam train structure
- 200 Gy/year, 5×10^{10} 1-MeV n_{eq}/cm^2/year

	CLIC_ILD	CLIC_SiD
Central beam pipe	Beryllium	
	$R_i = 29.4$ mm $d = 0.6$ mm	$R_i = 24.5$ mm $d = 0.5$ mm
Barrel region	3 double layers $\lvert z\rvert < 130$ mm $R_i = 31,\ 44,\ 58$ mm	5 single layers $\lvert z\rvert < 98.5$ mm $R_i = 27,\ 38,\ 51,\ 64,\ 77$ mm
Forward region	3 double layers $z = 160, 207, 255$ mm	7 single layers $z = 120, 160, 200, 240, 280, 500, 830$ mm
Sensors	$20\ \mu m \times 20\ \mu m$, $\sigma_{sp} \approx 3\ \mu m$	
	$X/X_0 = 0.18\%$ per double layer	$X/X_0 = 0.11\%$ per single layer
Surface area	$0.736\ m^2$	$1.103\ m^2$
Number of channels	1.84×10^9	2.76×10^9



Sensor technologies for futures linear colliders

- The sensor technologies foreseen for ILC and CLIC declines in 3 flavours

Monolithic sensors	3D/Hybrid type CMOS sensors	Hybrid pixel sensors
DEPFET, FPCCD, MAPS • Low material budget (50 um thickness)acheivable with current technology • Fine granularity (down to 5um pixel acheivable) • Coarse timing only (integrating sensor) • Suitable for ILC vertex detector • Partially depleted sensors • **See Session 2, 6**	**Chronopix, PLUME (MAPS), SOI pixel sensors** • Low material budget (50 um thickness)acheivable with current technology • Fine granularity (down to 5um pixel acheivable) • Coarse timing only (integrating sensor) • Suitable for ILC vertex detector • Partially depleted sensors • **See session 4 . 6**	**Timepix3/SmallPix/CLICPix** • Low material budget to be demonstrated • Coarser pixel pitch (~25 um pixel size acheivable) • Fully depleted : Time slicing (~ 10 ns) for background reduction • Make use of widely available commercial technology (130nm, 65nm CMOS) • Fast sparsified read-out • Suitable for CLIC • **See session 7, 8**

CLIC R&D for vertex detector instrumentation

- **Requirements**
  - **~ 20x20 µm2 pixel sizes : need small feature sizes !**
  - **Time-stamping ~10 ns : need high-resistivity sensor !**
  - **~0.2% X_o material/layer : corresponds to ~200 µm silicon (incl. support + cables) !**
  - **156 ns bunch train every 20 ms : trigger-less readout, power pulsing !**
  - **Magnetic field 4-5T : Lorentz angle !**

- The CERN LCD group R&D focuses on these main aspects of the CLIC vertex detector:
  - **Ultra-Thin Hybrid Planar Pixel Detector R&D**
  - **R&D on mechanics and cooling of the detector**
  - **R&D on power delivery and power pulsing**

Sensor Simulation and Digitization

Thin sensors (~50 um) deplete a very low voltage (1-10 V)

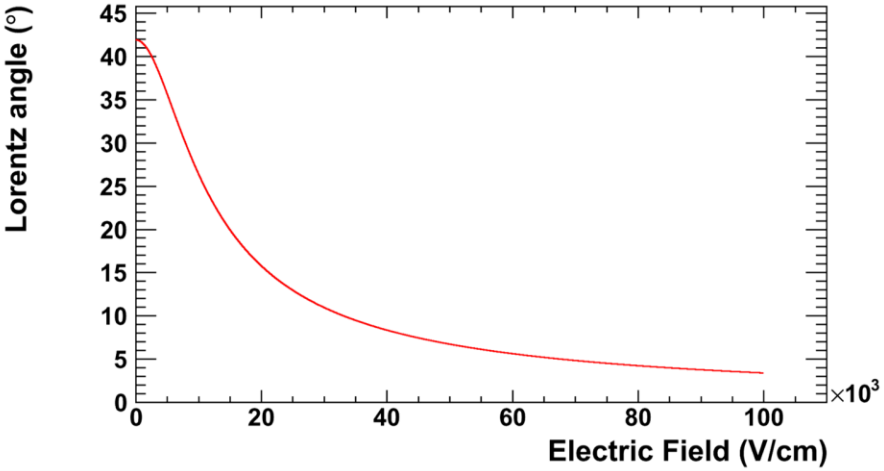
- Larger Lorentz angle in the drift of carriers

A set of simulation was performed to study these effects in pixel sensors

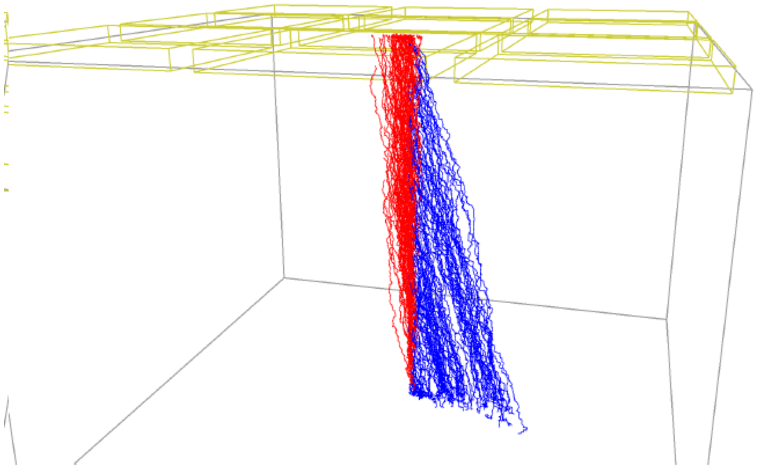
- **Geant4 simulation and Digitization model** (Fast, needs to be calibrated to readout chip and sensors)
- **TCAD simulation of thin pixel sensors.** Slow approach but allow to solve the full system of equation, useful for tuning of simpler models
- **Monte-Carlo Charge Transport coupled to Static TCAD simulation.** Allow for larger statistics, can be coupled to GEANT4

TestBeam campaign in CERN SPS with 180 GeV/c pions and Timepix-based hybrid planar pixel sensors

- Power Pulsing characterization
- Digitization and Simulation tuning



Lorentz angle dependence on Electric field in p-in-n sensor

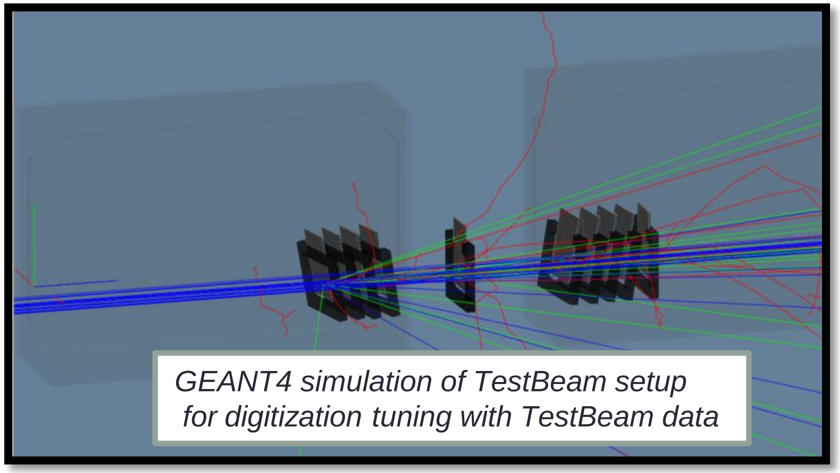


Carrier drift in a 50 um thick fully depleted sensor

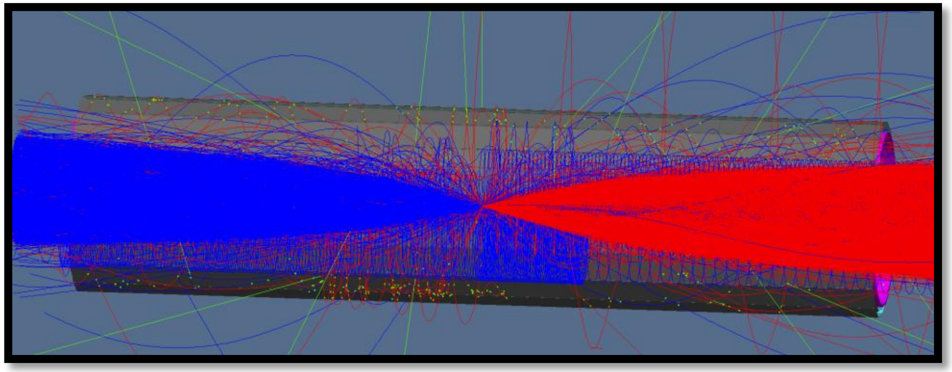
Sensor Simulation and Digitization

- TestBeam data will be compared to GEANT4 simulation (MC and Simple model based Digitizer) of the telescope setup

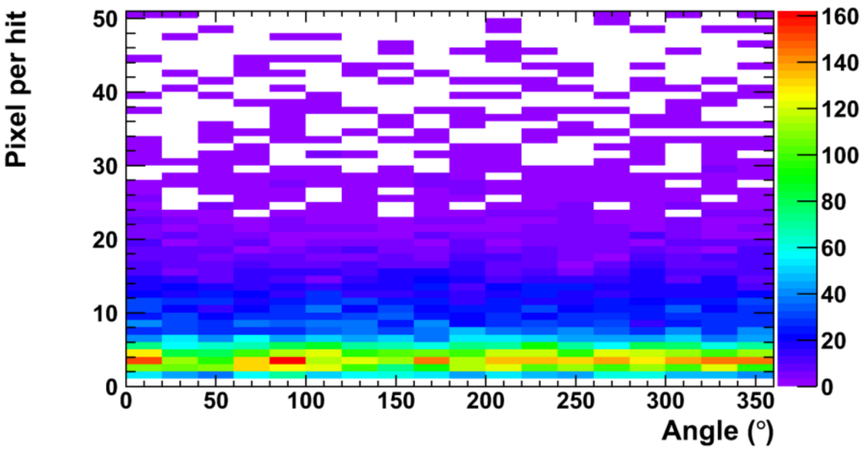
- The Simple Digitizer can be used to predict occupancy in the vertex layout



GEANT4 simulation of TestBeam setup for digitization tuning with TestBeam data

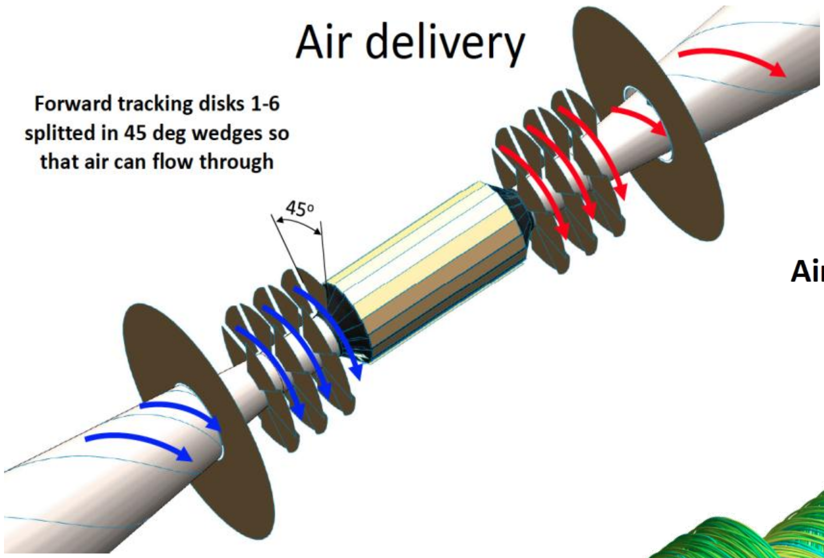


GEANT4 simulation Beam Background in CLIC vertex detector using our tuned digitizer

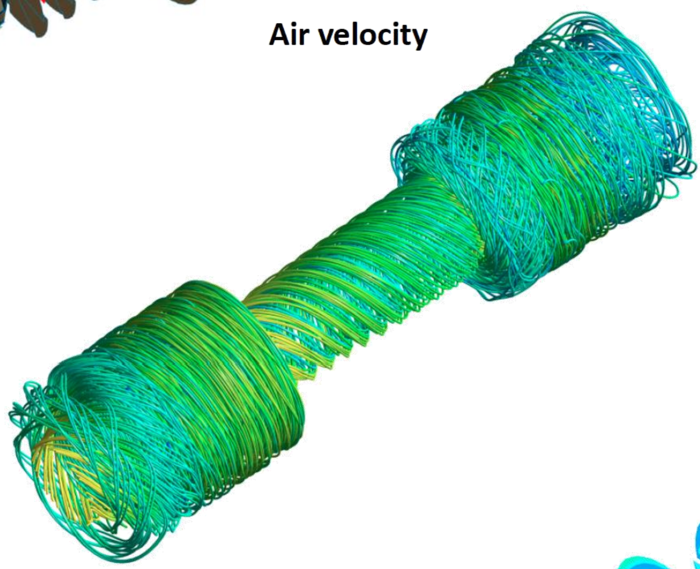


Hit multiplicity in CLIC vertex detector using our tuned digitizer

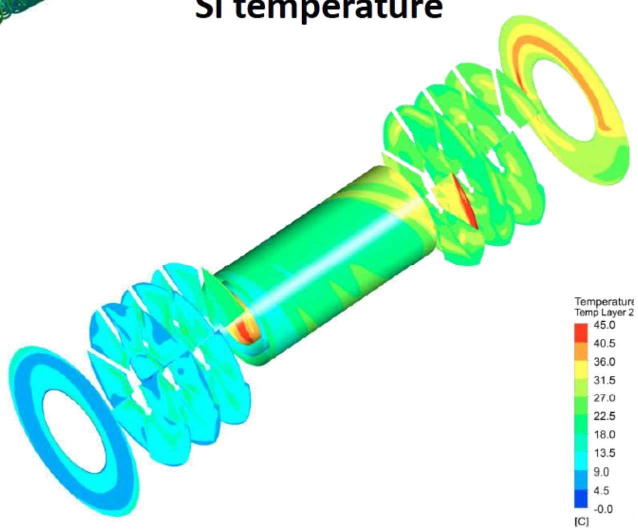
CLIC Mechanics Integration and cooling



Mass Flow:20.1g/s
Avg.velocity@Inlet:11.0m/s
Avg.velocity@Z=0:5.2m/s
Avg.velocity@outlet:6.3m/s

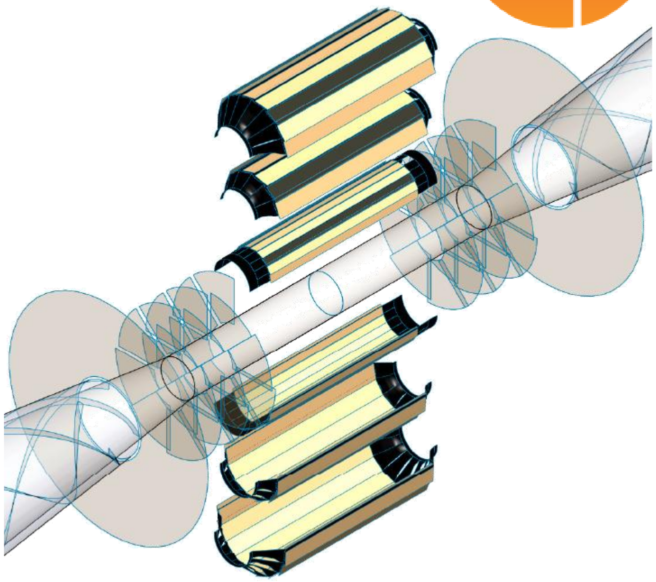


Temperature below 30C
Except for Barrel layer 2 (40C)
Conduction not taken into account



F. Duarte Ramos, CERN

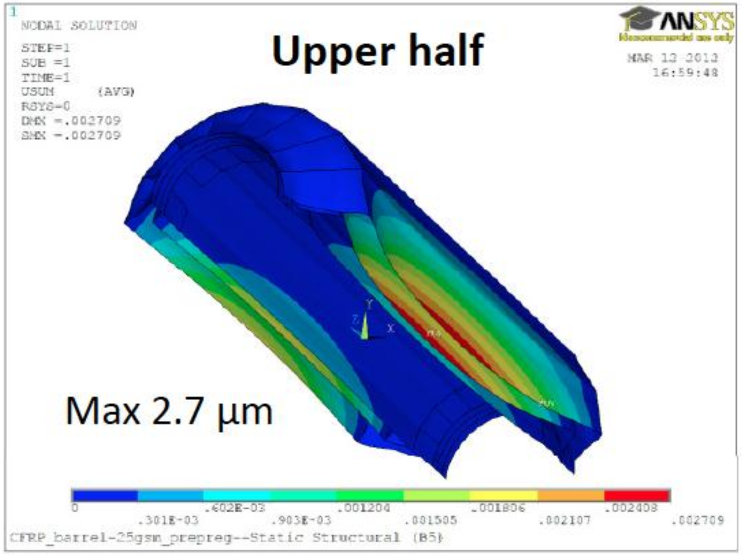
CLIC Mechanics Integration and cooling



Ongoing work on the design of the disk and barrel support **to minimize material budget and allow air cooling** to be efficient.

- Low mass carbon fiber shell (180um CFRP)
- Spiraling petal design

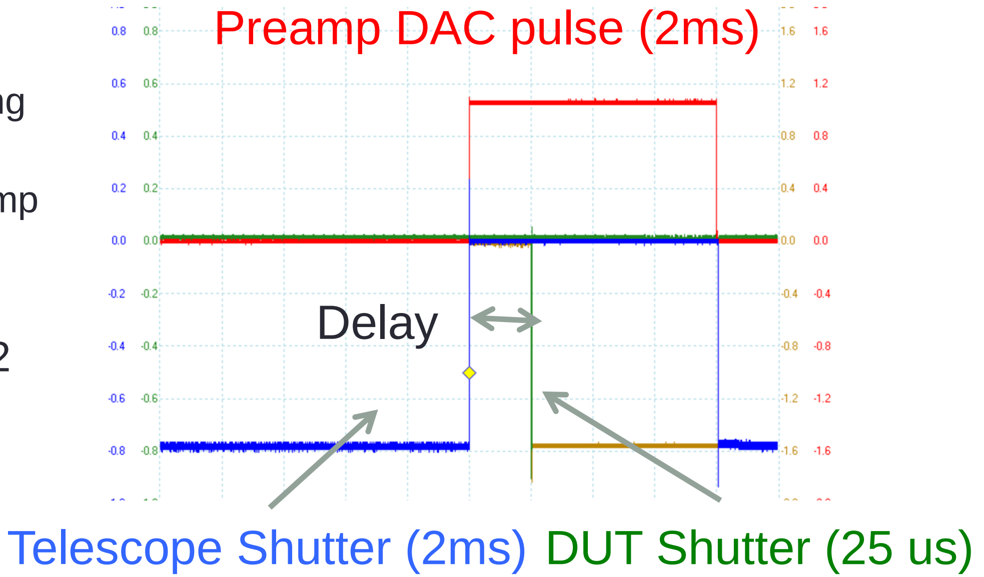
Vibration and **deformation** analysis are being performed to evaluate the efficiency of cooling and vibration present in the barrel and disk structures



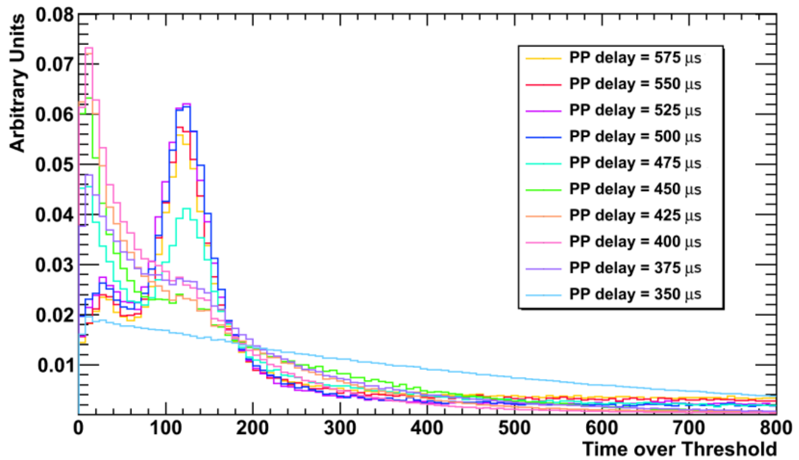
F. Duarte Ramos, CERN

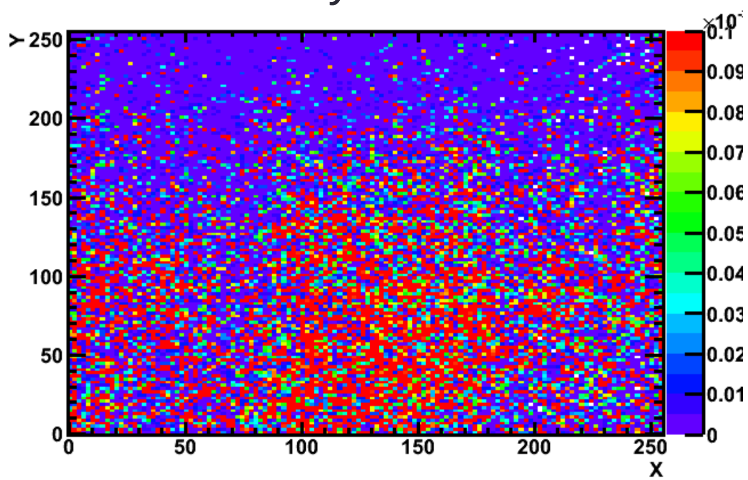
CLIC: Power delivery and Power Pusling

- Power Pulsing with the Timepix chip
  - Not design for pulsing, large capacitance coming from single bias line for all pixel row
  - Possible to nevertheless power-pulse the preamp of the chip through its bias DAC
- CERN SPS testbeam campaign in June2012
  - Power pulsing of the Chip and operation in synchronisation with a Tracking telescope (LHCb/Timepix Telescope)
  - Results are promising, showing full detection efficiency within 600 us



Delay = 350 us





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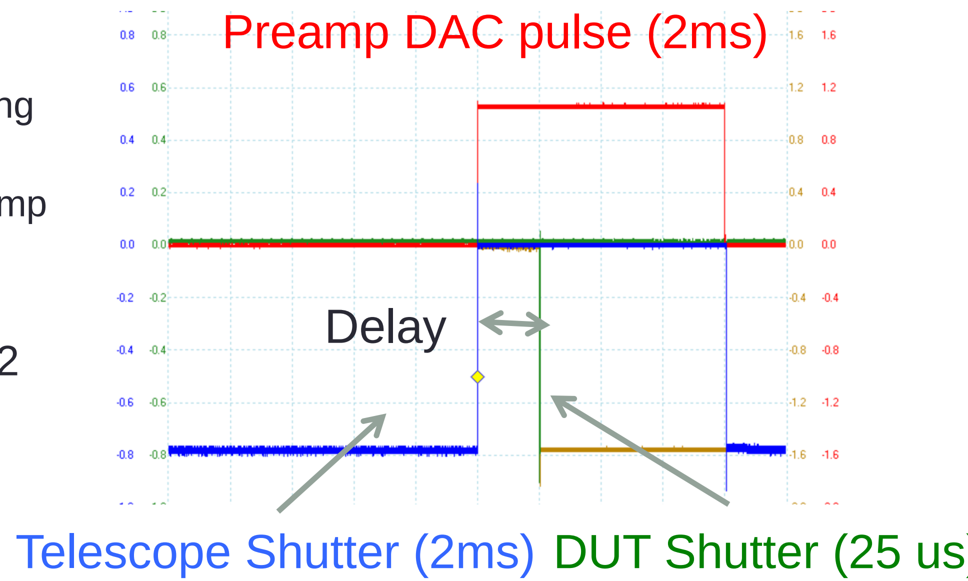
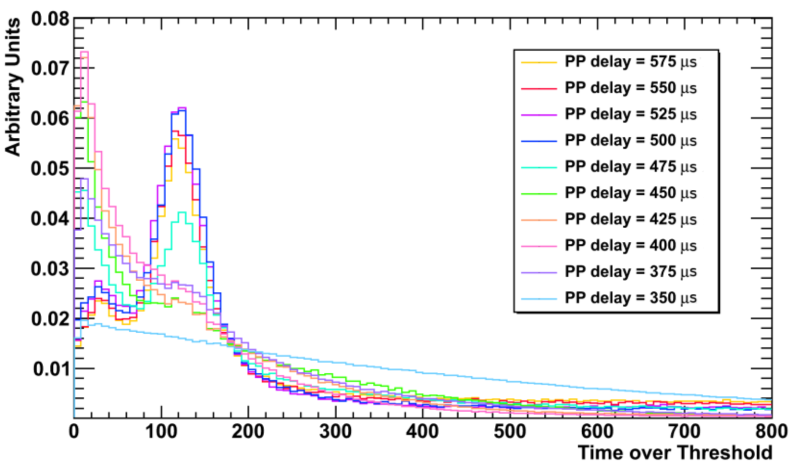
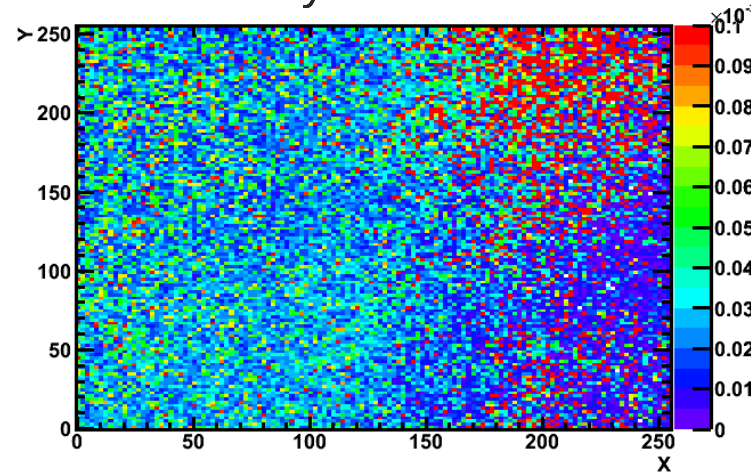




Delay = 400 us



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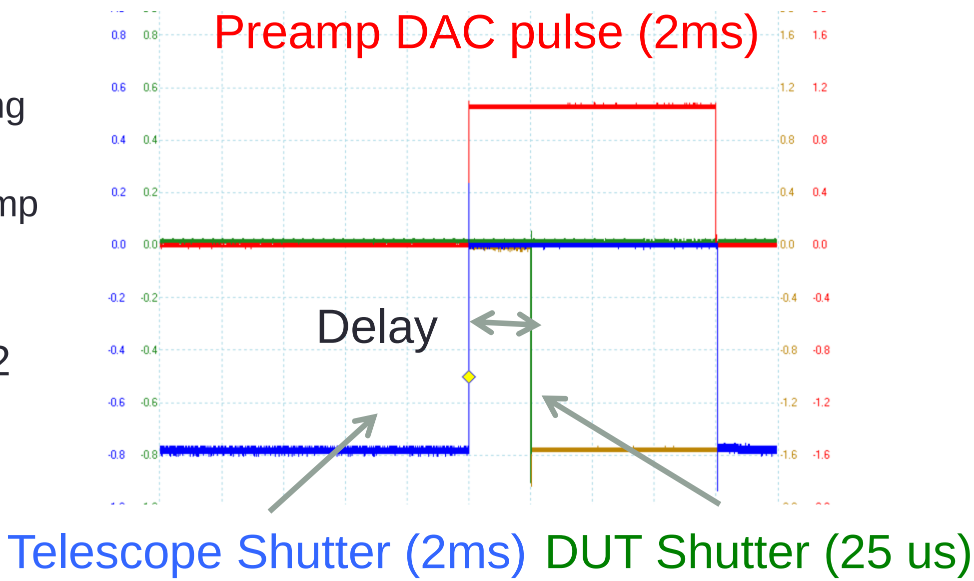
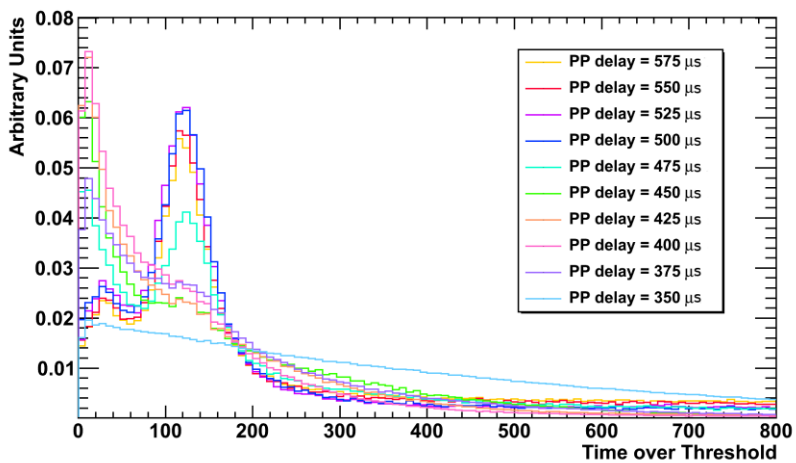
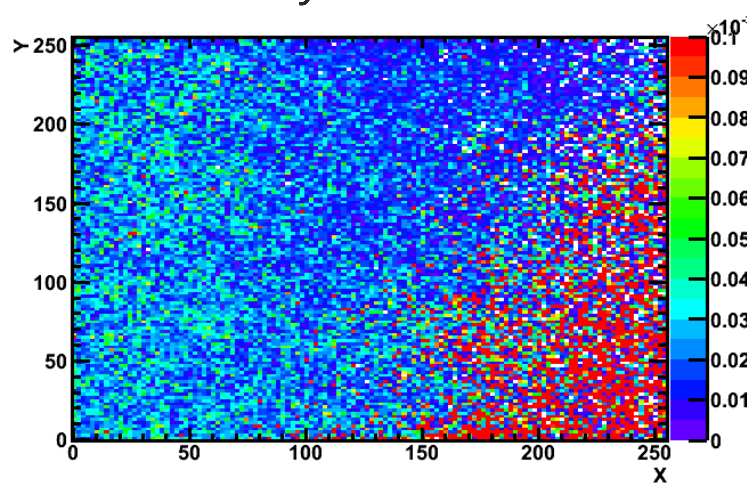


Delay = 450 us





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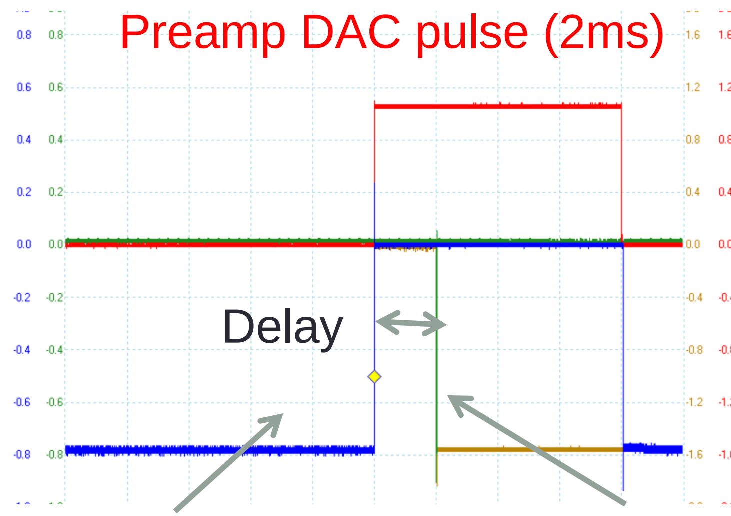
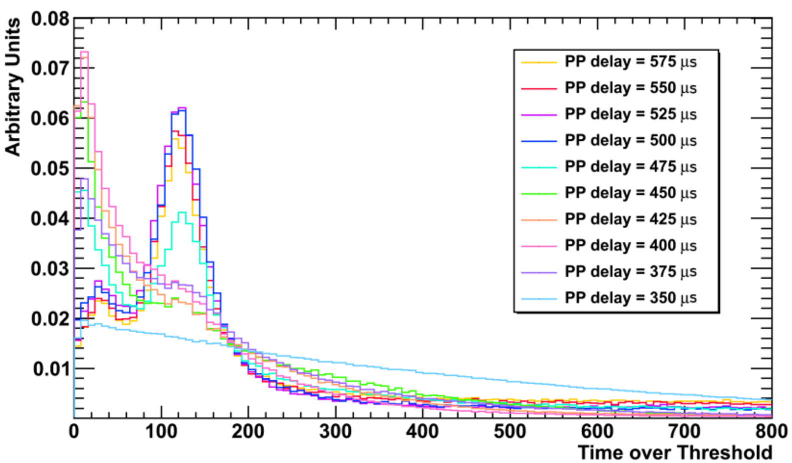
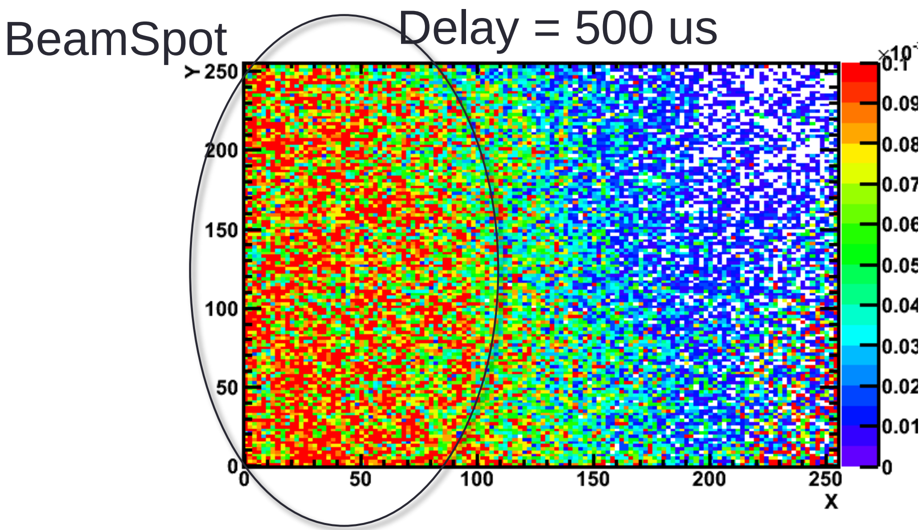


Telescope Shutter (2ms) DUT Shutter (25 us)





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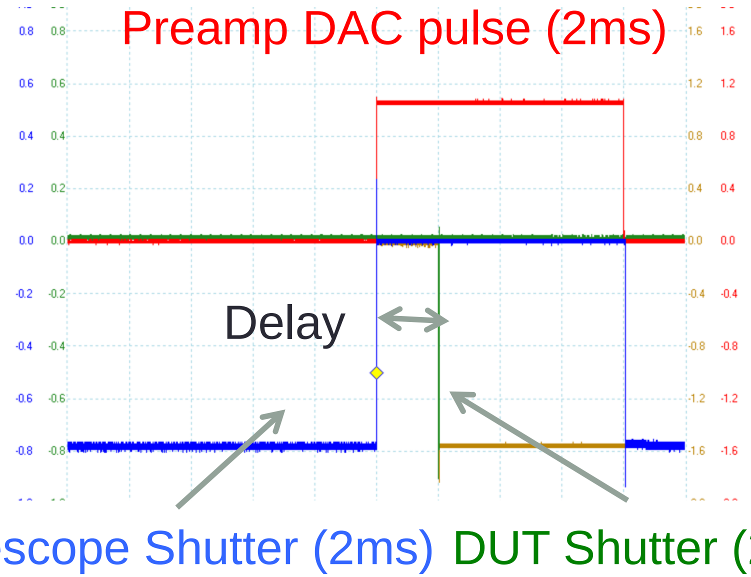
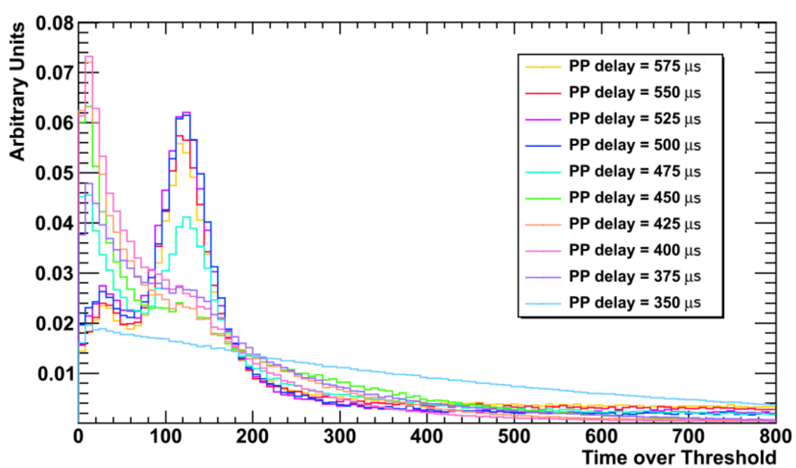
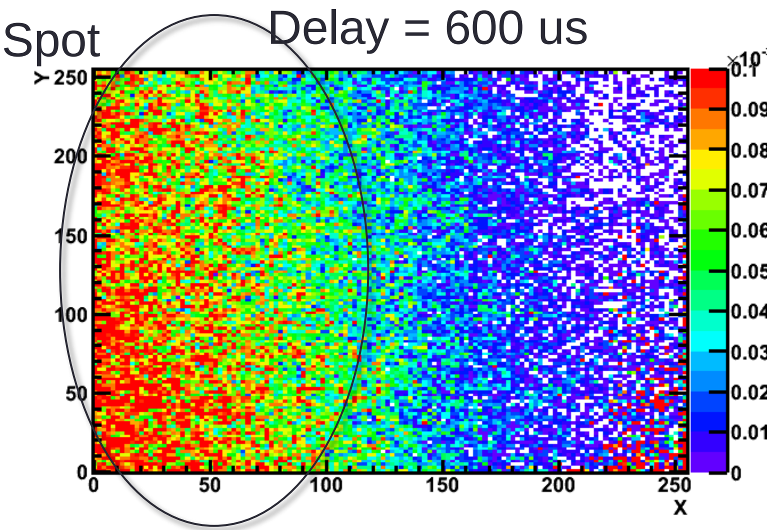


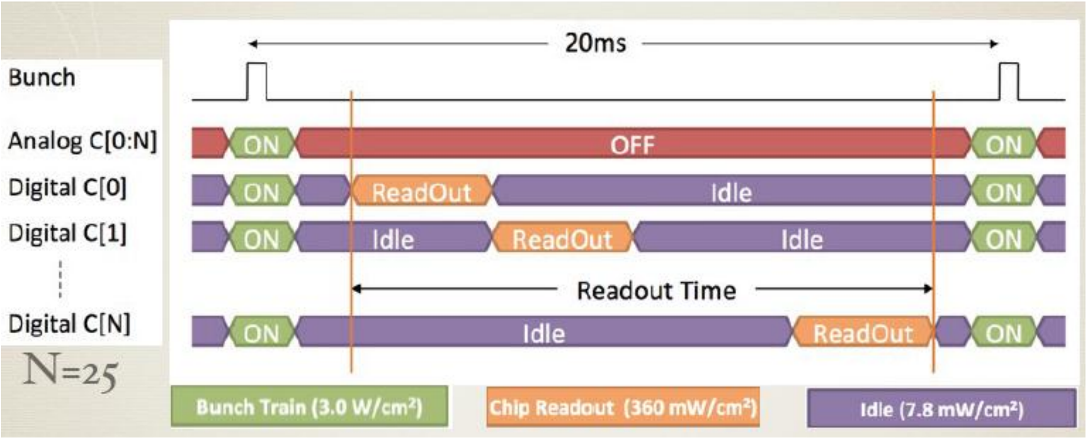


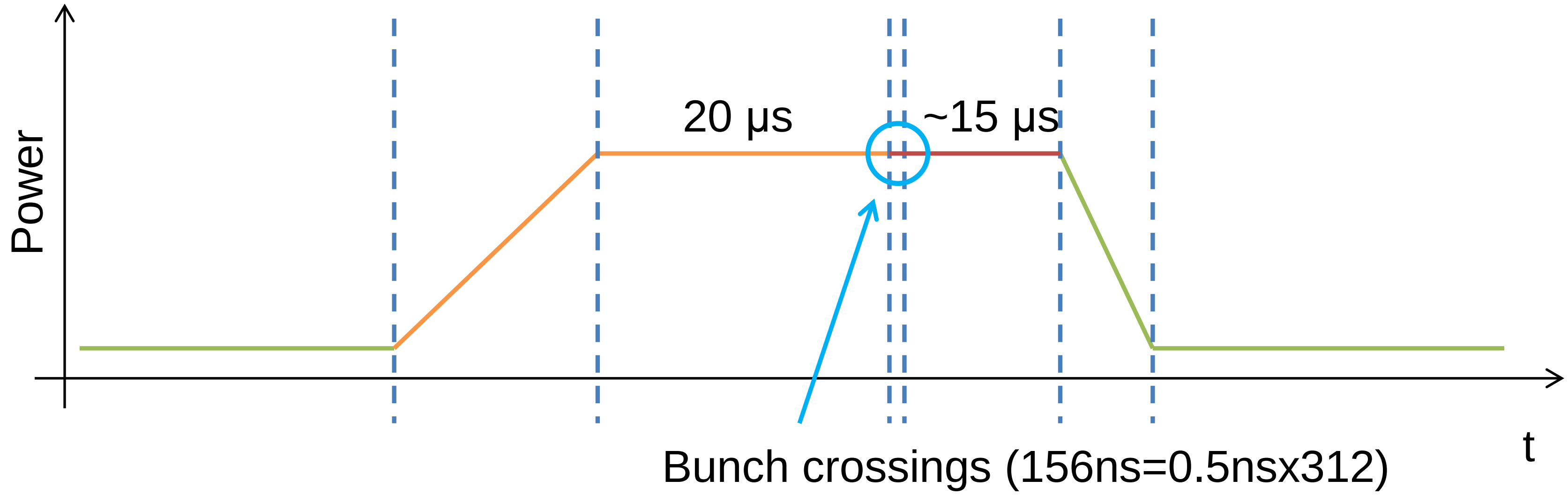


CLIC: Power delivery and Power Pusling

C. Fuentes, CERN

- Power delivery in low Material budget Flex Cable represent a great challenge : 20A / half-ladder during acquisition!



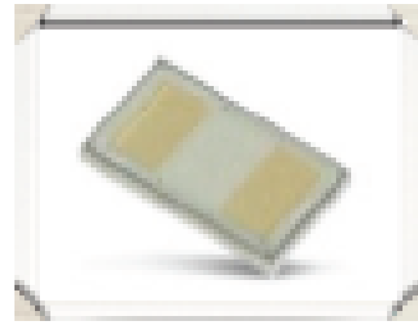


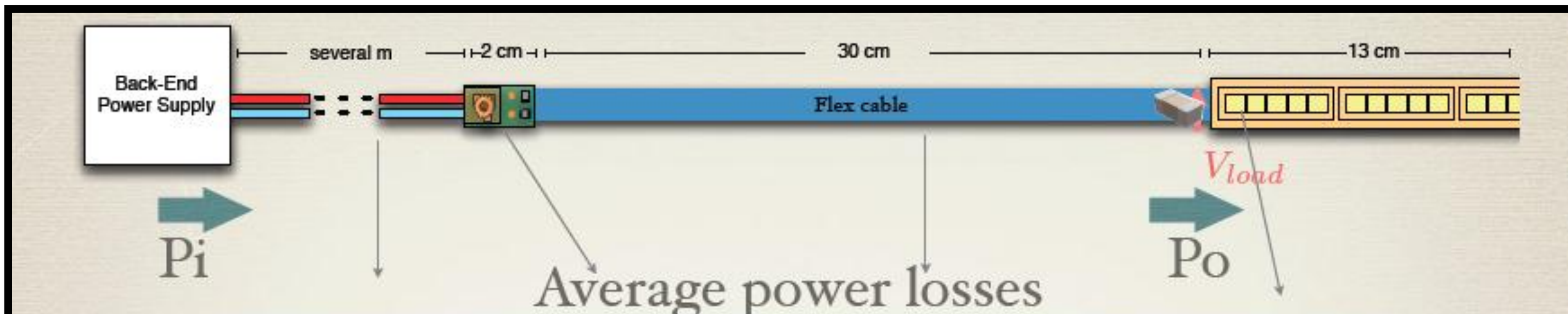
CLIC: Power delivery and Power Pusling

C. Fuentes, CERN

DCDC Conversion and use of **large value capacitor** to store the power close to the detector and recharge between trains

- High power DC-DC conversion
- Low material budget Storage capacitor (Silicon capacitor, 50um thickness, 100uF per piece)



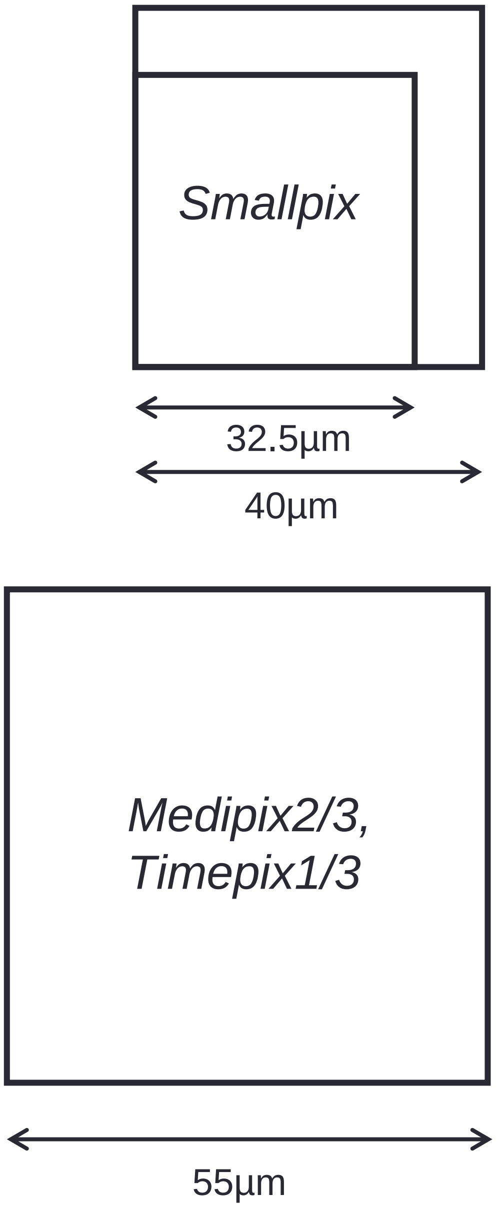


	Cable in	DCDC	Flex	1st chip Load	1st LDO
Vin=5V	13mW	45mW	3mW	26mW	12mW

SmallPix: general features

Technology: 130nm CMOS

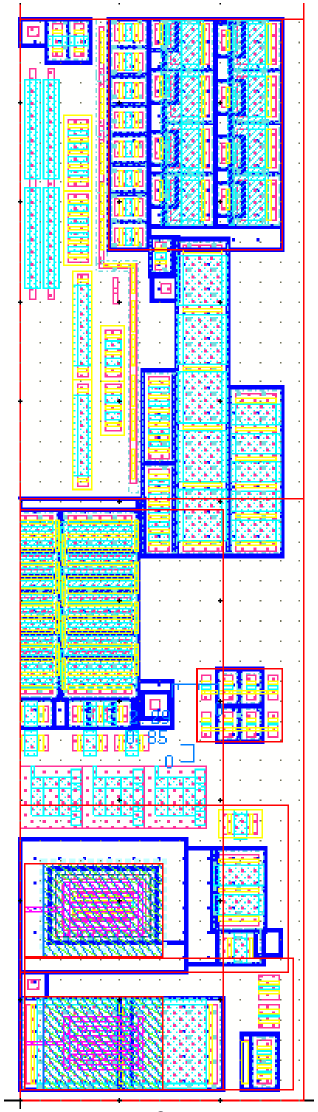
- **Goal:** decrease pixel size compared to previous Medipix/TimePix chips (55x55um^2 pixel)
- **Features:**
  - **130 nm Technology**
  - ≈19x20mm^2 chip size, 250kpixel
  - Two ≈14bit counters allow simultaneous Integral Time-Over-Threshold (TOT) and Time Of Arrival (TOA) or simultaneous TOT and Photon Counting; Increase resolution (counters' depths) using 2x2 SuperPixels
  - Zero suppression in the pixel to compress data and speed up the readout
  - Zero suppression per column
  - Re-use High Density library from MediPix3
  - Power Pulsing Logic on Chip



R. Ballabriga, M. De Gaspari, CERN

SmallPix: analog specifications, area & power estimate

- **Analog Design**
  - Analog front-end in synergy with TimePix3 development
  - Based on a Krummenacher feedback preamplifier and a single-threshold discriminator
  - Small feedback capacitor => high gain => the system works in saturation for charges bigger than 12ke$^-$
  - Analog noise ≈80e$^-$@C_{det}=25fF, allowing thresholds as low as 500e$^-$
  - Leakage current compensation: -10nA (e$^-$), +20nA (h$^+$)
  - Peaking time <25-50ns
- **Digital Design**
  - Timewalk <25ns for Q_{in}=1500e$^-$
  - TOT monotonicity for big positive charges up to >300kh$^+$
  - TOA resolution 1.5ns
- **Footprint**
  - Analog area: 630-780um^2 with 3-4bit pixel equalization DAC
  - Digital area: 575um^2 for 10bit, 644um^2 for 12bit, 705um^2 for 14bit
  - Equivalent to a Pixel size ≈40x40um^2 with 14bit TOT/TOA counters
- **Power Consumption**
  - Analog consumption: 7.4uA/pixel (3uA single-ended preamplifier, 4uA discriminator);
  - Assuming 0.5uA/pixel digital@1.5V => 740mW/cm^2, before power pulsing



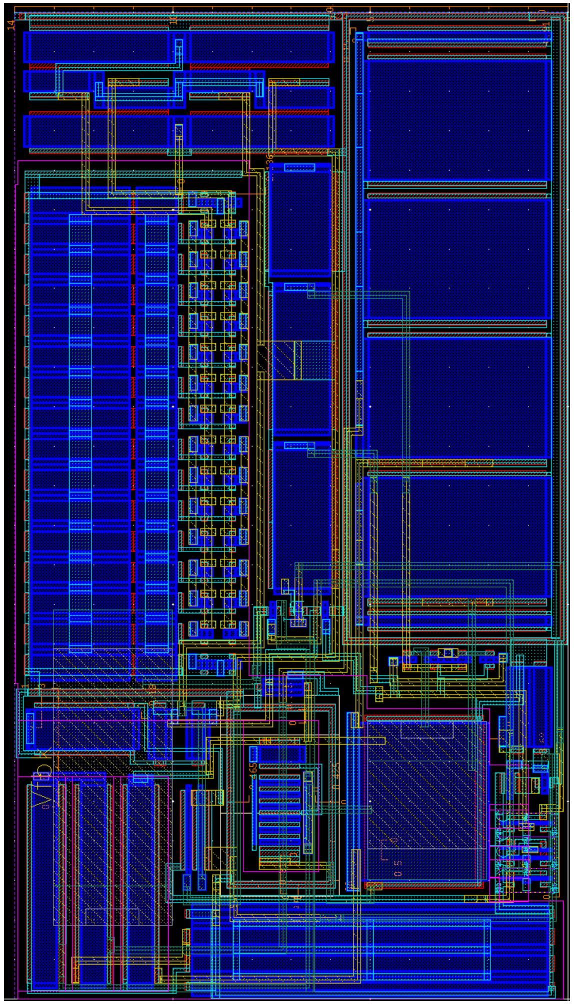
780um^2 draft for TimePix3

- Submission target: Q1/Q2 2013.

R Ballabriga, M De Gaspari, CERN

CLICPix: General Features

- CLICPix is a pixel detector ASIC under development at CERN, implemented in **65 nm CMOS**, driven by the requirements of CLIC vertex detectors
- The main feature is the **small pixel pitch (25 μm)**,
- Each pixel includes simultaneous **4-bit TOA and TOT measurements**
- Photon Counting Mode for threshold equalization purposes
- Front-end **time slicing aims to be less than 10 ns** (timewalk can be corrected using the TOT measurement)
- A (selectable) compression logic allows skipping pixels which were not hit during the acquisition. A **cluster-based and column-based compression is also being implemented**. Full chip in less than 800 μs (for a 10% occupancy) using a 320 MHz read-out clock
- A **power pulsing scheme has been implemented** allowing for the reduction of the average power consumption to be less than 50 mW/cm^2 (allowing the use of air cooling)
- The main contribution to the power consumption is the analog front-end, which would use ~2W/cm^2 if run continuously
- The demonstrator will have a **fully functional 64 by 64 pixel matrix**



- The submission for **November 2012** with a Multi-Project Wafer (MPW)

P Valerio, CERN

Conclusion

- Future linear collider vertex detectors present a new kind of challenges compared to LHC
  - Less radiation damage but …
  - Higher precision (timing ~10ns, SPR ~5 um)
  - Less power (2uW/channel, 50mW/cm2)
  - Lower Material budget (50-100 um of silicon, minimalist support structures)
- R&D Converge toward a set of solution fullfilling the requirement for CLIC and ILC

- CLIC Conceptual Design Report Volume 2 and Volume 3 are published
- ILC Detector Baseline Document (DBD) in preparation, to be released end of 2012

Thanks for your attention ! ありがとう。

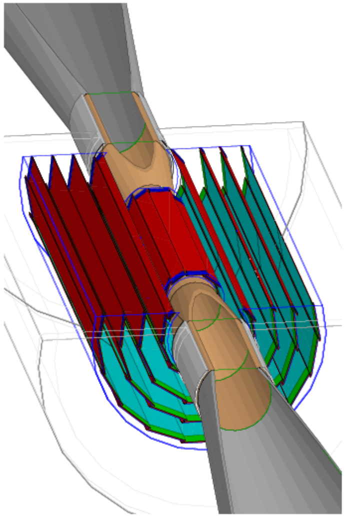
BACKUP

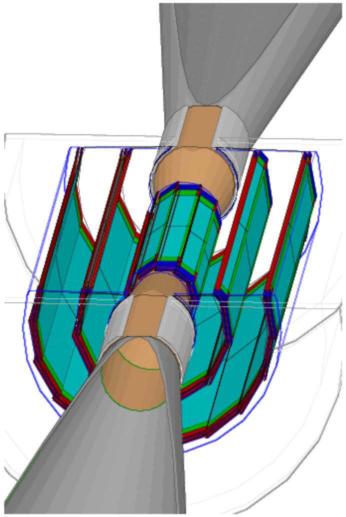
The ILD vertex detector concept

- **Material Budget**
  - 0.11, 0.16 % X_o for VTX-SL/DL at normal incidence
  - 500 um overlap between sensitive regions of ladders

- **Physics Requirements**
  - SPR : < 3um
  - Double hit separation : < 40um
  - Sensor thickness: ~ 50 um
  - 4T magnetic field

- **Foreseen Technology**
  - CMOS, DEPFET, FPCCD

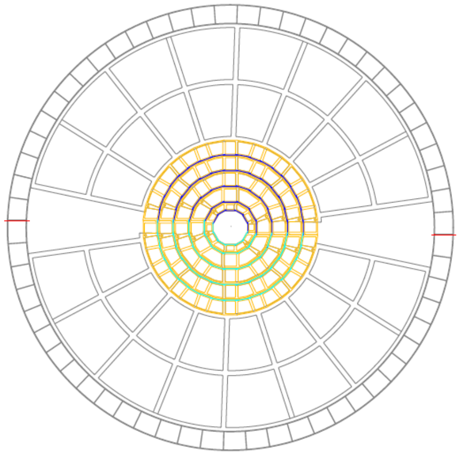


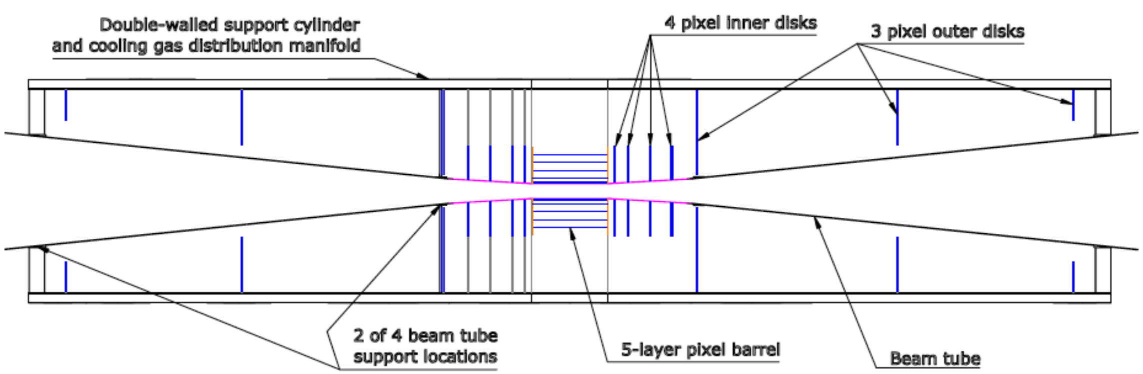


The SiD vertex detector concept

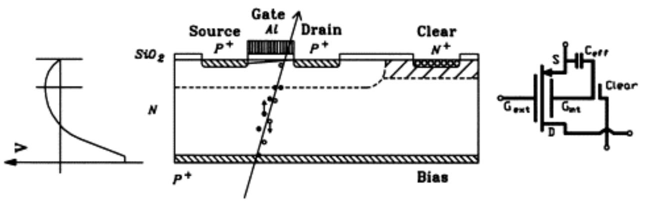
- **Material Budget**
  - ~0.1 % X0 target per layer at normal incidence
- **Physics Requirements**
  - SPR : < 5um
  - Double hit separation : < 40um
  - Sensor thickness: ~ 50-100 um
  - 5T magnetic field
- **Foreseen Technology**
  - 3D Hybrid , DEPFET, CHRONOPIX

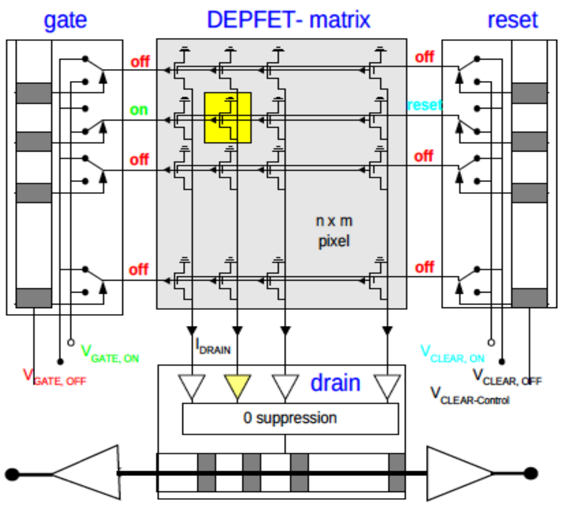
Barrel Region	R (mm)	Length (mm)	Number of sensors in φ
Layer 1	14	125	12
Layer 2	21	125	12
Layer 3	34	125	20
Layer 4	47	125	28
Layer 5	60	125	36
Disk	R_{inner}	R_{outer}	z_{center}
Disk 1	15	75	76
Disk 2	16	75	95
Disk 3	18	75	125
Disk 4	21	75	180
Forward Disk	R_{inner}	R_{outer}	z_{center}
Disk 1	28	166	211
Disk 2	76	166	543
Disk 3	118	166	834





Sensor technologies for futures linear colliders : DEPFET

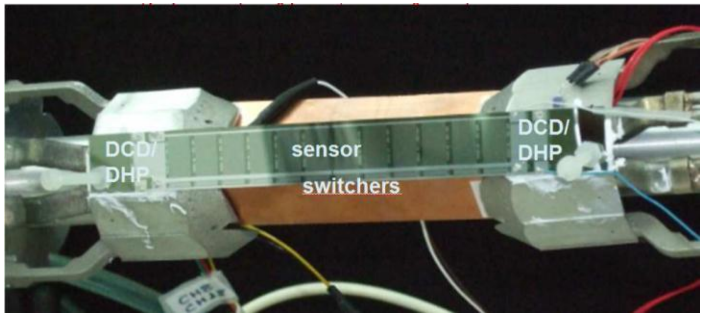




- The Depleted Field-Effect transistor relies on a depleted layer located under a FET.
- A Potential minimum is created in the channel of the transistor
- Accumulation of charge from ionizing particles modified the charge distribution in the channel and increase the Transistor current

- Monolithic Sensor allow for thin Assembly (50 um , ex: PXD6)
- Allows for small pixel size (~25x25 um)

- Integrating sensor (Frame ~25-100us), so coarse timestamping

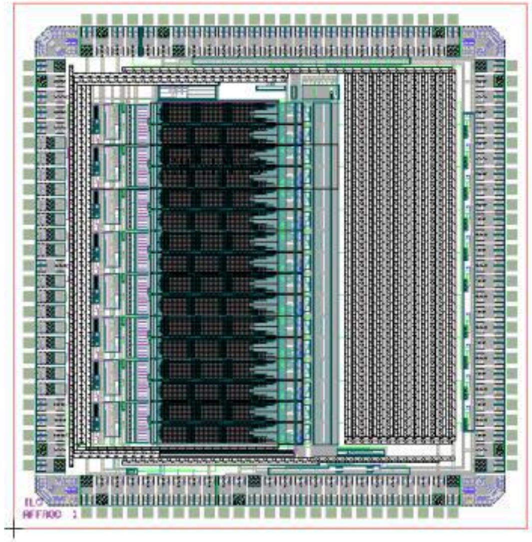


- **The ultra low mass cooling system of the Belle II DEPFET detector**
- **The Belle II pixel detector: high precision with low material**

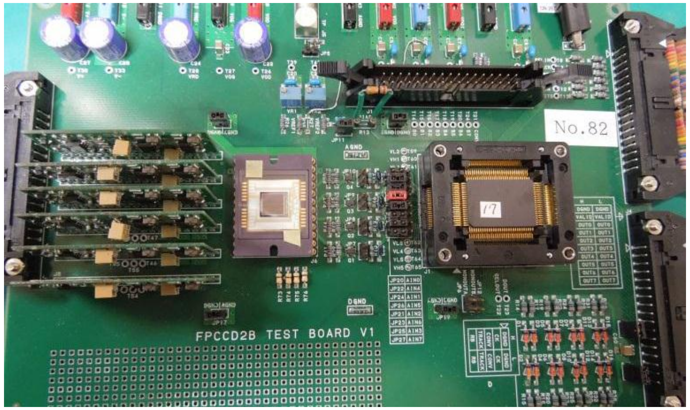
Dr Marinas Pardo, poster session, Oral presentation Session 2

Source : DEPFET active pixel detectors, Marcel Vos – IFIC Valencia, KILC2012

Sensor technologies for futures linear colliders : FPCCD



- **Fine Pixel Charge-Coupled Device** (5x5 um)
- A ~15 um depleted region in created in the sensitive area to favorize drift of carrier and limit diffusion
- Integrate over a bunch train, readout during gap between trains
  - Fast-Readout needed (>10MPixel/s)
  - No Timestamping, occupancy kept low by small pixel size, background rejected by pattern recognition
- To limit power consumption and obtain faster readout, sensor need air cooling at low temperatures ~(-40 C)

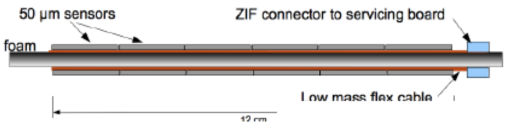


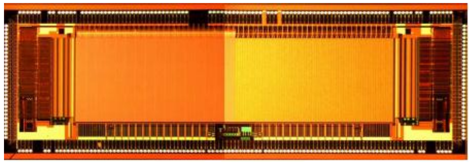
Source : Developments of Readout ASIC for FPCCD vertex detector, Eriko Kato, Tohoku U. ,[KILC2012]

Sensor technologies for futures linear colliders : CMOS Pixel Sensors (MAPS)

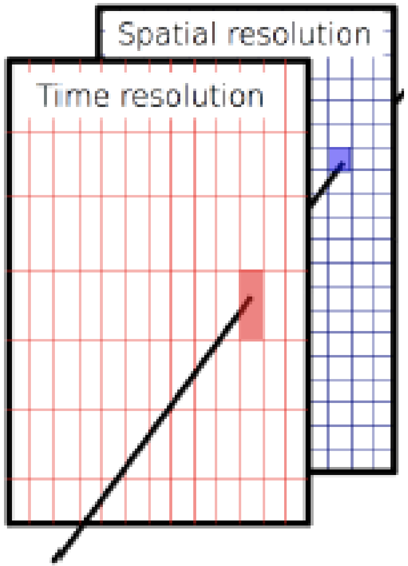
Ex : MIMOSA Family (IPHC)

- Monolithic sensor, CMOS process with high-resistivity epitaxial layer to increase signal and limit diffusion
- Electronics integrated in pixel
  - Correlated-Double Sampling (CDS) in pixel
  - Rolling shutter read-out (coarse timing)
  - Analog or digital readout possible





- Proposed 2 type of sensors for inner and outer layers (PLUME)
  - MIMOSA-30 : Dual sided readout out
  - 1 side for spatial resolution (16x16 um pixel), 1 side for timing (~10us, 16x80 um pixel)
  - MIMOSA-31 : Larger pixel for reduced power consumption (35x35 um)



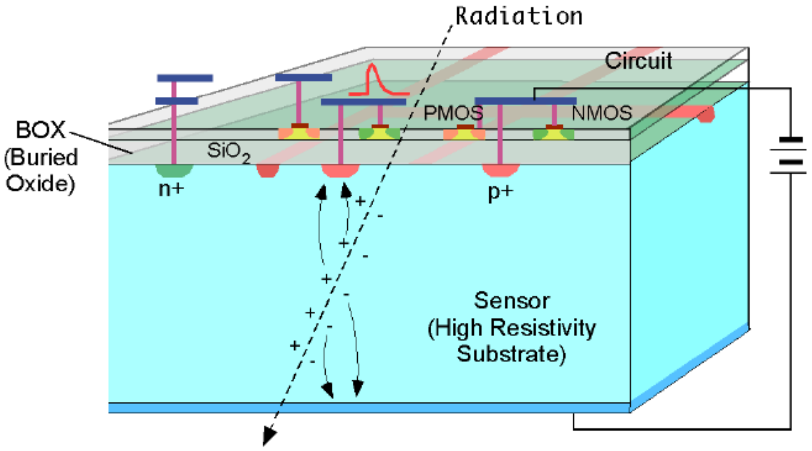
- R&D Ongoing to develop faster-readout, sparsified readout, stiching of sensors , larger depleted area

See Session 6 for details on the MAPS technology

Source :Towards a Vertex Detector Concept with a Microsecond Timestamping, Marc Winter, IPHC, KILC2012

Sensor technologies for futures linear colliders : SOI Pixel Sensors

- CMOS sensor on SOI wafers
  - Fully depleted High-Resistivity sensor
  - Electronics on low resistivity wafer separated by BOX from sensing layer
- Allow for standard CMOS electronics
  - Fast time stamping possible
  - Complex pixel « intelligence »
  - Insulation of each device from bulk allow for low leakage current operation



Progress of SOI Pixel Process
Yasuo Arai, Session 2

High-Resolution Monolithic Pixel Detectors in SOI Technology
Toshinobu Miyoshi, session 4

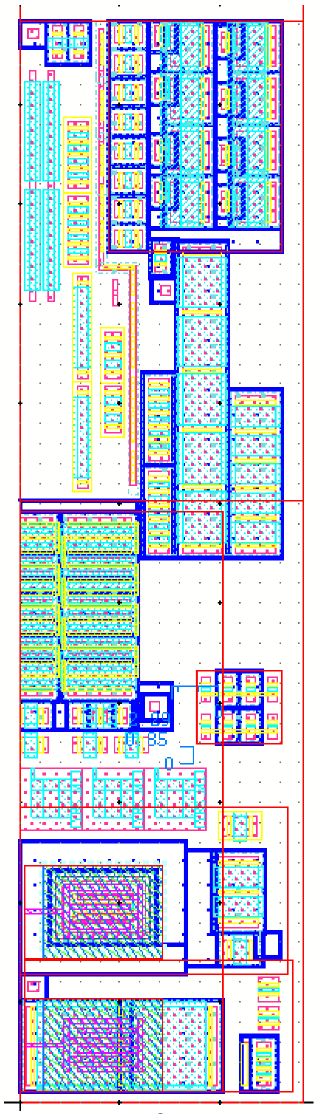
A thin fully-depleted monolithic pixel sensor in SOI technology
Serena Mattiazzo, session 4

3D Integration for SOI Pixel Detector
Makoto Motoyoshi , session 4

Source : Monolithic Pixel Detector with SOI technology, Yasuo Arai, CERN seminar, June 28th 2011

SmallPix: analog specifications, area & power estimate

- **Analog Design**
  - Analog front-end in synergy with TimePix3 development
  - Based on a Krummenacher feedback preamplifier and a single-threshold discriminator
  - Small feedback capacitor => high gain => the system works in saturation for charges bigger than 12ke$^-$
  - Analog noise ≈80e$^-$@C_{det}=25fF, allowing thresholds as low as 500e$^-$
  - Leakage current compensation: -10nA (e$^-$), +20nA (h$^+$)
  - Peaking time <25-50ns
- **Digital Design**
  - Timewalk <25ns for Q_{in}=1500e$^-$
  - TOT monotonicity for big positive charges up to >300kh$^+$
  - TOA resolution 1.5ns
- **Footprint**
  - Analog area: 630-780um^2 with 3-4bit pixel equalization DAC
  - Digital area: 575um^2 for 10bit, 644um^2 for 12bit, 705um^2 for 14bit
  - Equivalent to a Pixel size ≈40x40um^2 with 14bit TOT/TOA counters
- **Power Consumption**
  - Analog consumption: 7.4uA/pixel (3uA single-ended preamplifier, 4uA discriminator);
  - Assuming 0.5uA/pixel digital@1.5V => 740mW/cm^2, before power pulsing



780um^2 draft for TimePix3

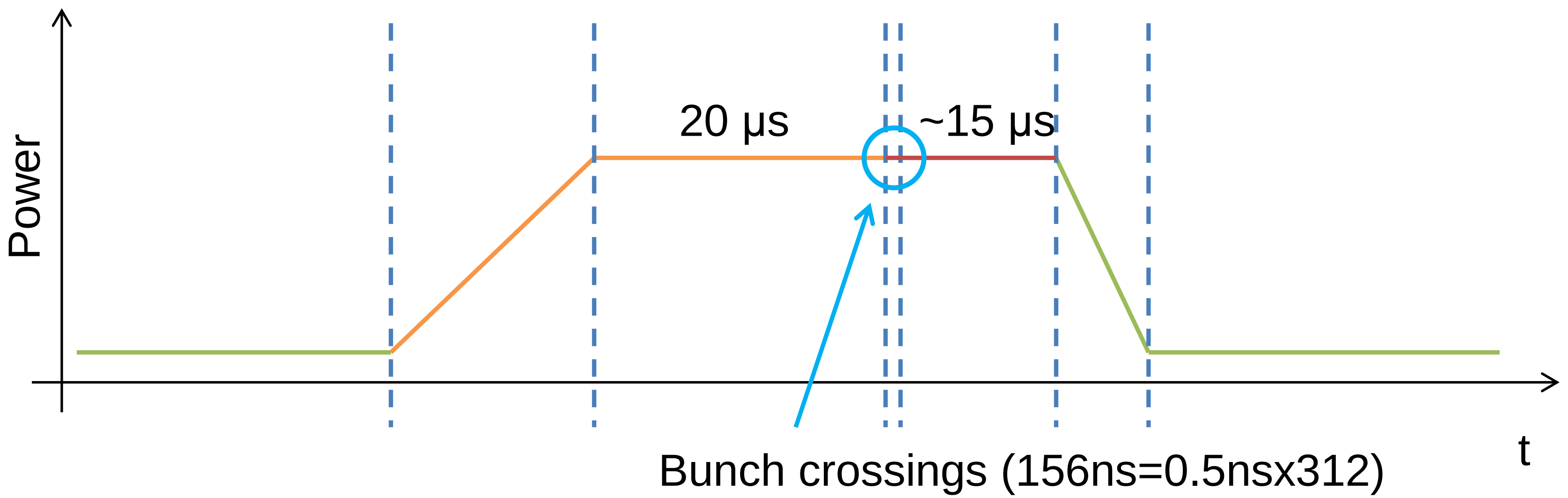
- Submission target: Q1/Q2 2013.

R Ballabriga, M De Gaspari, CERN

CLICPix : Power consumption

- The main contribution to the power consumption is the analog front-end, which would use ~2W/cm^2 if run continuously
- A **power pulsing scheme has been implemented** allowing for the reduction of the average power consumption to be less than 50 mW/cm^2 (allowing the use of air cooling)

- The submission for **November 2012** with a Multi-Project Wafer (MPW)
- The demonstrator will have a **fully functional 64 by 64 pixel matrix**



P Valerio, CERN