Development of Data-Acquisition Front Ends enabling High-bandwidth Data Handling for X-ray 2D Detectors: A Feasibility Study

Choji Saji*, Toru Ohata, Takaki Hatsui[1)], Togo Kudo[1)], Takashi Sugimoto, Ryotaro Tanaka, Mitsuhiro Yamaga
(JASRI/SPring-8, [1)]RIKEN)

Introduction & Objective

- Output data of X-ray 2D detector' for synchrotron radiation and X-ray free-electron laser experiments should be large throughput because of larger number of pixel, higher dynamic range and frequent repetition for more detail information on sample.
- Data-Acquisition systems will be composed by various kinds of detectors and back-end analysis/storage system.

Data-Acquisition Front End (DAQ-FE) system for future X-ray 2D detector needs to achieve High-bandwidth and support various input/output interfaces.

High-bandwidth:

- Some of our target detectors are for X-ray free-electron laser experiments in SACLA (SPring-8 Angstrom Compact X-ray free Laser).
- Throughput for single sensor will increase from ~0.5 Gbps to 20 Gbps in the future.

Support various interfaces:

DAQ-FE will be used for various experiments as follows,

Various detectors/sensors:

- SPring-8 facility has many beamlines and various detectors/sensors
  - 57 beamlines for synchrotron radiation experiments
  - 1 beamline for X-ray free-electron experiments

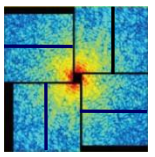
Various scale of DAQ system:

- Network distributed system: VMEs, PCs, storages connected via network
- Standalone system: compact DAQ system installed all device into a computer

Upgrade to next generation detector

MPCCD (Multi Port CCD)

- CCD type X-ray detector
- Currently provided as photon sensor for SACLA



Data rate:

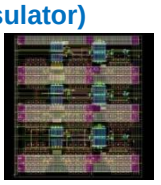
Single sensor (whole 8 sensors):
(512x1032) pixel x 16 bits (depth)
x 60 Hz (acc. repetition) **= 0.5 Gbps**

FE-DAQ input/output:

Input: Camera Link Base Configuration
Spec < 2.04 Gbps
Output: Gigabit Ethernet
Spec < 1 Gbps

SOPHIAS (Silicon On Insulator)

- Under developing
- Next generation photon sensor for SACLA



Data rate:

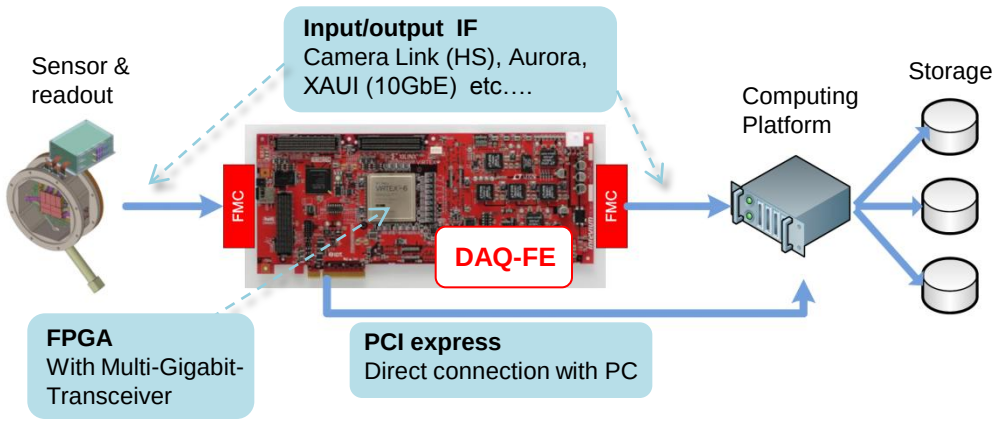
Single sensor (whole 40 sensors)
~2M(pixel) x 16~32 bits (depth)
x 60~300 Hz (acc. repetition)=2 **~ 20 Gbps**

FE-DAQ I/O:
Need high-bandwidth interfaces

Target Data-rate
Single: 2 ~ **20 Gbps**
We need next generation technology
→ Start feasibility study

Implementation

DAQ schematic view:



Hardware:

High-bandwidth: FPGA w/ Multi-Gigabit-Transceiver (MGT)
Support various IF: FPGA Mezzanine Card (FMC | ANSI standard VITA57)

FPGA evaluation board

FPGA: Vertex6
W/ 6.6 Gbps MGTs → ~20 Gbps by 4 lane-bonding
FMC: HPCx2 → 8 MGTs for each FMC, Select both I/O interfaces
PCI express: gen2x8 → high-bandwidth interface to connect with PC directly

FMC

3 FMCs were selected to study 2 physical layers and 2 transformation protocols.

FMC	Physical layer	Protocol
TD-BD-OPT4	SFP+ 4ch	Aurora
FMS-28	QSFP+ 2ch	Aurora
HTG-FMC-SFP	SFP+2ch (10G PHY)	XAUI

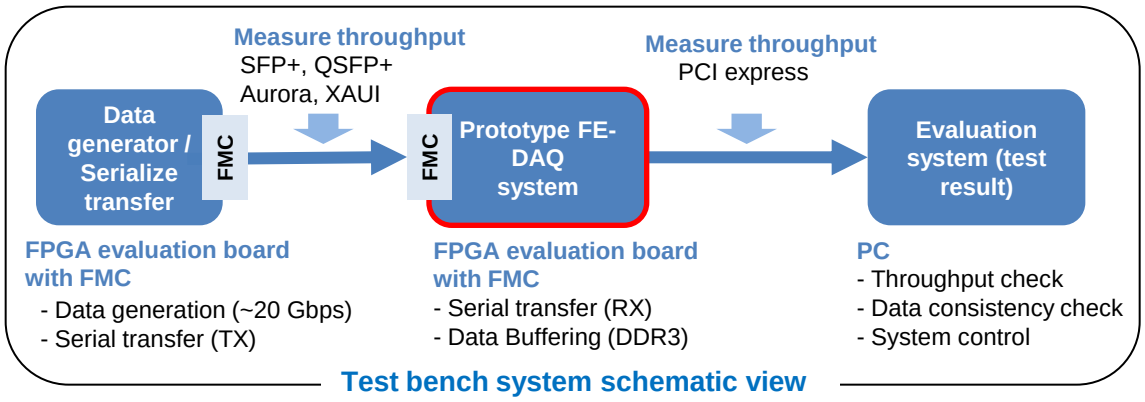
Feasibility Study:

Objective:

- Is FMC really effective to support some interfaces?
- Can we achieve ~20 Gbps high-bandwidth using FPGA and FMC?

Test bench system:

- Composed of FPGA evaluation board, FMC and PC
- Using a pair of evaluation board, we can study some physical layers and protocols by changing FMCs
- Developed FPGA logics for each FMCs



Test bench system schematic view

Results

High-bandwidth:

- Successfully measured effective bandwidth of around 20 Gbps through SFP+/QSFP+ with AURORA. It shows FPGA, evaluation board and FMC potential is enough for required bandwidth.

Support various interface:

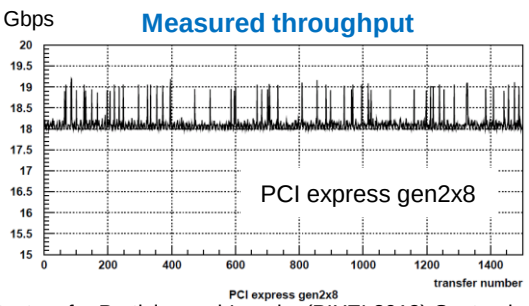
- We could successfully test some physical layers and protocols by changing FMCs. It found various interface of FMC will support various type of experiments.

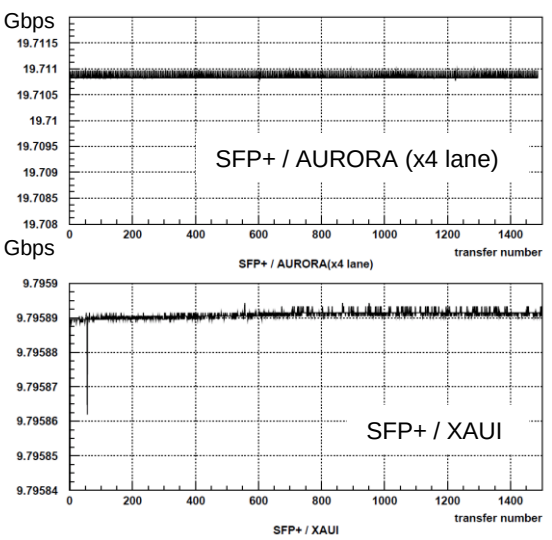
Summary:

- We have found a combination of FPGA and FMC has enough potential for data acquisition of the next generation synchrotron radiation experiments. We will adopt them for the development of the actual DAQ system.

Physical layer	Protocol	Throughput (Gbps)
SFP+	Aurora (x4 lane)	19.7
QSFP+	Aurora (x4 lane)	19.7
SFP+	XAUI	9.8
PCI express (gen2 x 8)	PCI express	18.1

Measured throughput





* saji@spring8.or.jp

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