A thin fully-depleted monolithic pixel sensor in Silicon On Insulator technology

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Outline

- Monolithic pixel sensors in Silicon On Insulator technology

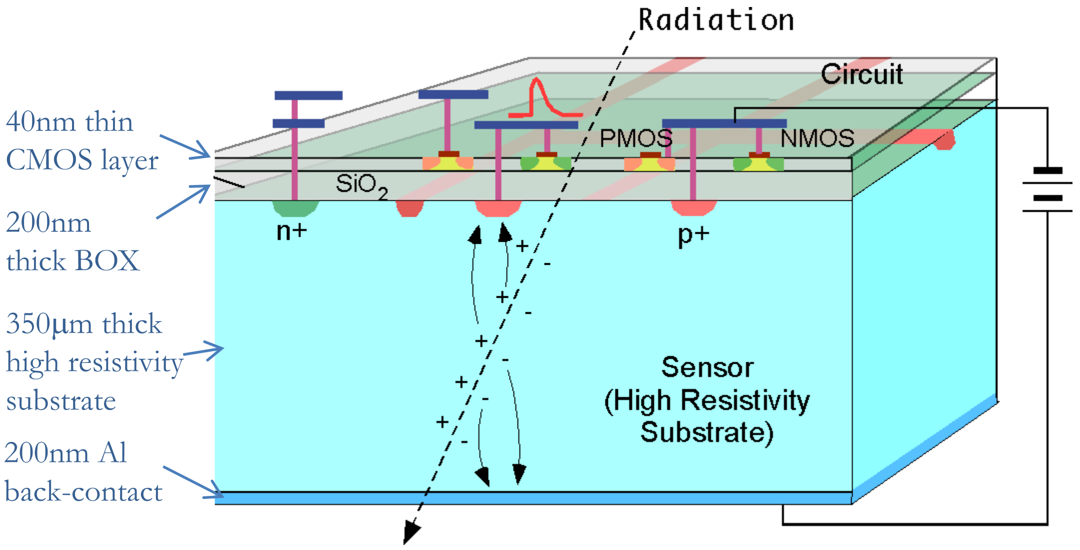
- Review of LBNL-PD-UCSC chip production

- Latest chip produced (SOImager-2):
  - Thinning and back-processing
  - Test on thin detector with Soft X-rays
  - Test on thin detector with MIPs
  - Measurement of the Lorentz Angle

- Conclusions

Monolithic Pixel Sensors in SOI technology

- In the Silicon On Insulator (SOI) technology, CMOS electronics is implanted on a thin silicon layer on top of a buried oxide (BOX): this ensures **full dielectric isolation, small active volume and low junction capacitance** (higher latch-up immunity, lower power consumption, higher speed applications).

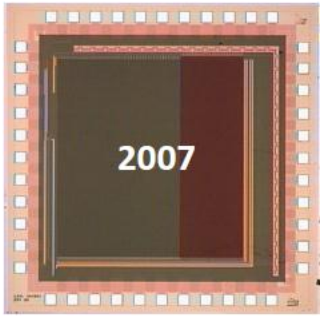


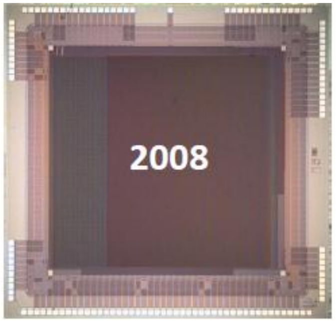
- In the SOI technology **depleted monolithic pixel sensors** can be built by using a high resistivity substrate and providing some vias to interconnect the substrate through the BOX;
- Pixel implants can be created and a reverse bias can be applied; charge is collected by drift.

➢ LAPIS (former OKI, **Japan)** provides a 0.20µm Fully Depleted (FD) SOI process on high resistivity substrates

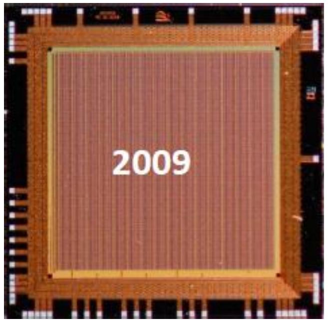
A brief history of SOI pixel prototypes

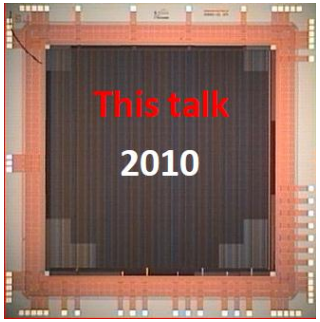
Within an international collaboration between the Lawrence Berkeley Laboratory, UC Santa Cruz, the University of Padova and the INFN of Padova, we are developing depleted monolithic pixel sensors in Silicon On Insulator technology





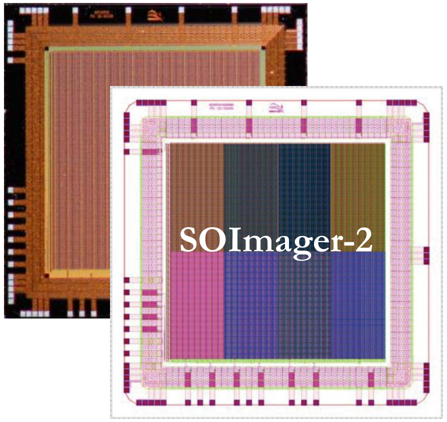
- LDRD-SOI series: technology demonstration with high momentum particles on analog and digital pixels. Limited by the backgate effect
  - **NIM A 583 (2007) 526**
  - **NIM A 604 (2009) 380**
  - **JINST 4 P04007 (2009)**



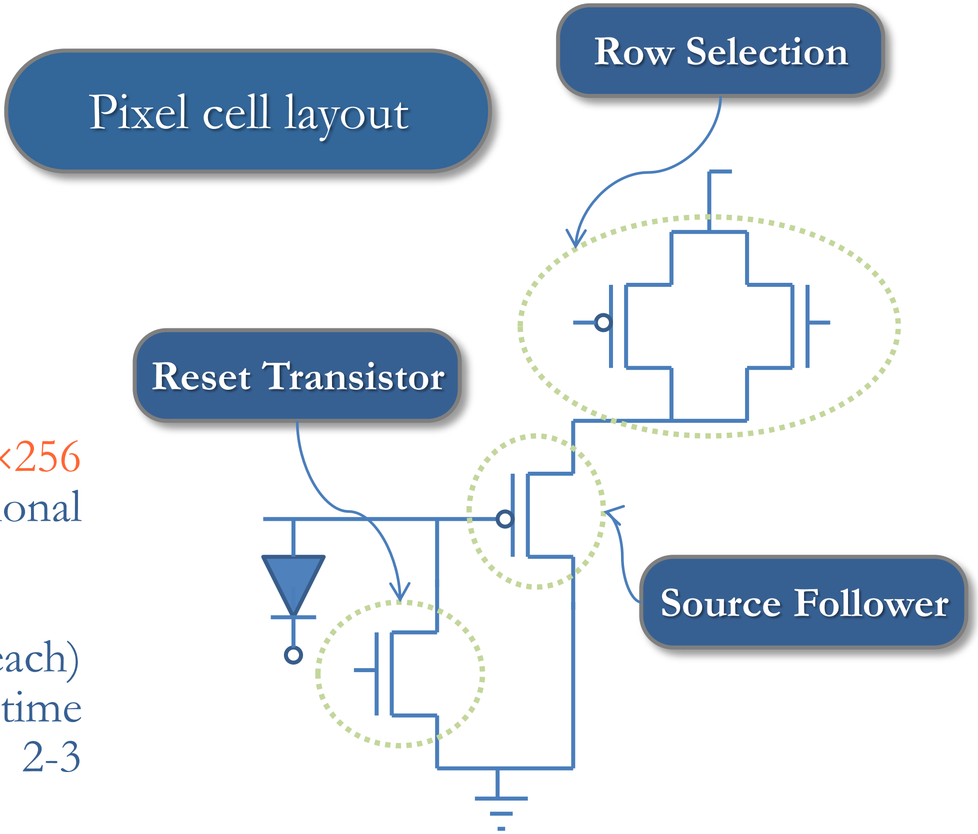


- SOImager series: optimization of pixel layout, test of different substrates

2009-2012: SOI-Imager series

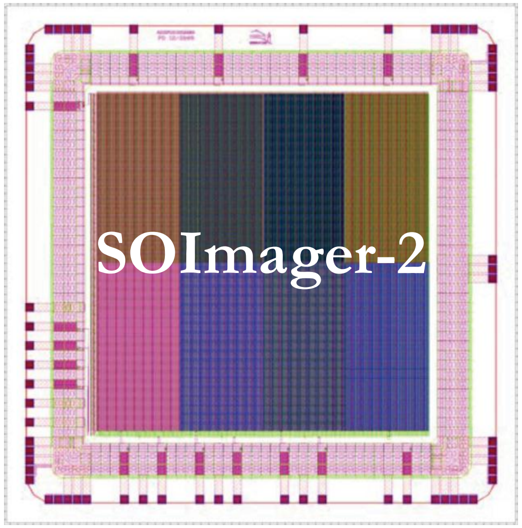


Optimization of the pixel layout, more effective solution against back-gating, larger area

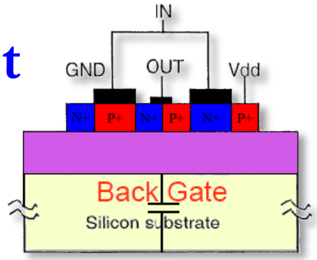


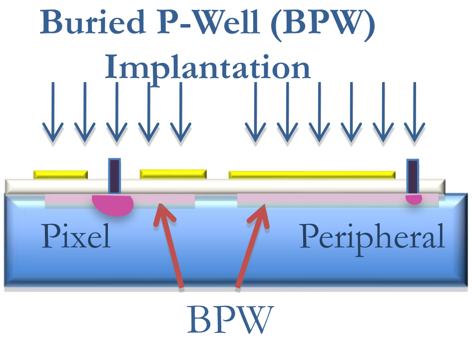
- LAPIS 0.20 µm FD-SOI process
- 5×5 mm^2 (active area is 3.5 ×3.5mm^2) 256×256 analog 3T pixels, 13.75 µm pitch, 1.8 V operational voltage
- 4 parallel analog outputs (64×256 pixels each) read out up to 50 MHz, 328 µs integration time (rolling shutter readout architecture) ➡ 2-3 kframes/sec

SOImager-2: pixel layout study



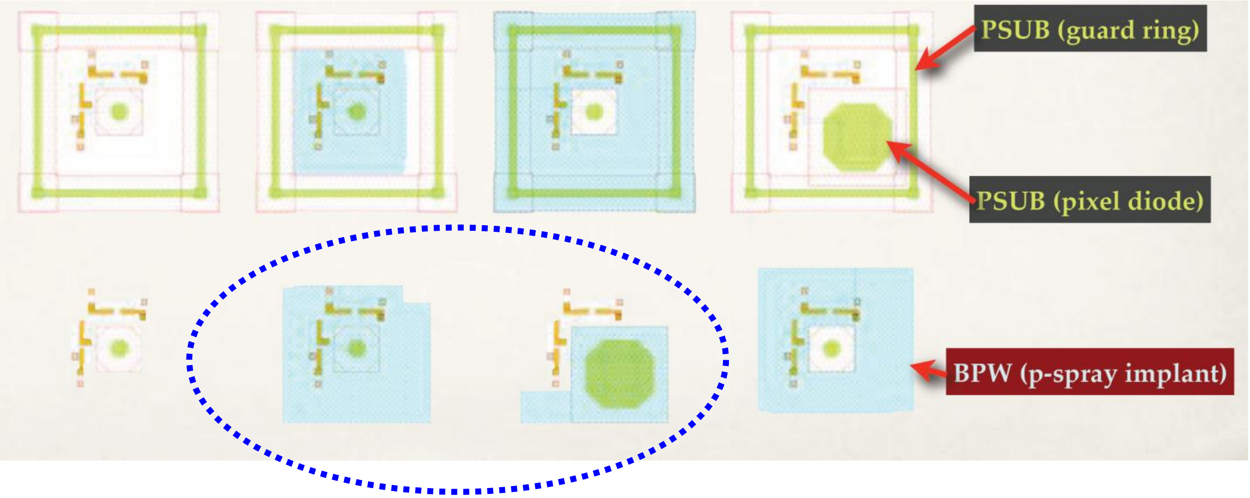
Backgate effect and BPW





Pixel layouts for the 8 sectors

- NIM A 650 (2011) 184
- NIM A 654 (2011) 258
- NIMA 658 (2011) 125



Thinning and back-processing

Breakdown at 130V prevents full depletion

A set of sensors has been back-thinned to 70µm using a commercial grinding technique

The backplane is damaged after the thinning process

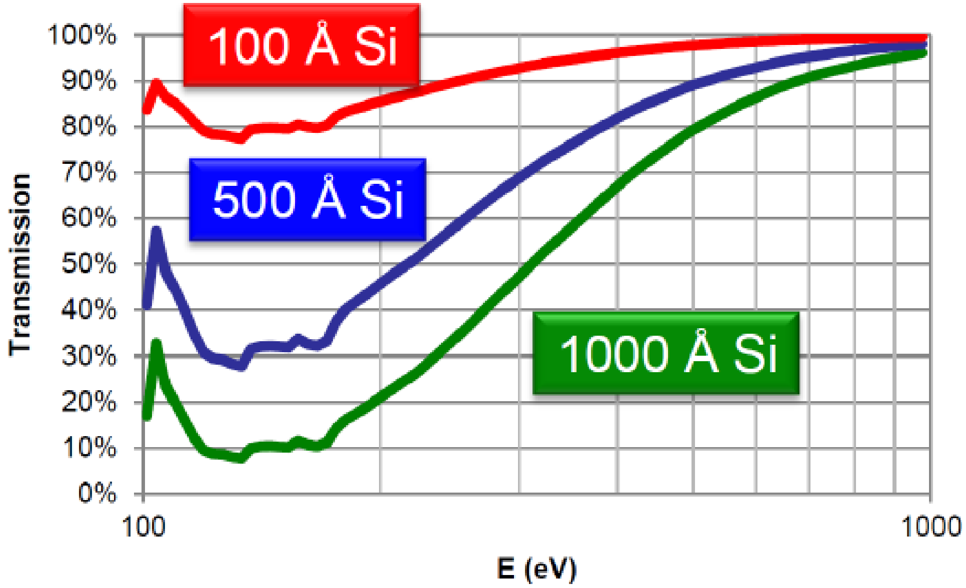
Need good contact to extend electric field to detector back-plane

Goal: create a thin entrance window for soft X-ray photon detection via back-illumination

R&D on back-processing

- Need 100 Å window thickness for an efficient O(100eV) X-ray sensitivity

- Several processes under test at LBNL



Process	Window Thickness	Status
Low energy implantation + 500°C annealing	1000-2000 Å	Process dependent, several SOI prototypes functional
Low energy implantation + laser annealing	400-700 Å	Several SOI prototypes functional
a-Si (amorphous silicon) contact deposition by sputtering	300Å	Prototypes functional after processing, high leakage
Molecular Beam Epitaxy	50-75 Å	Building in-house capability

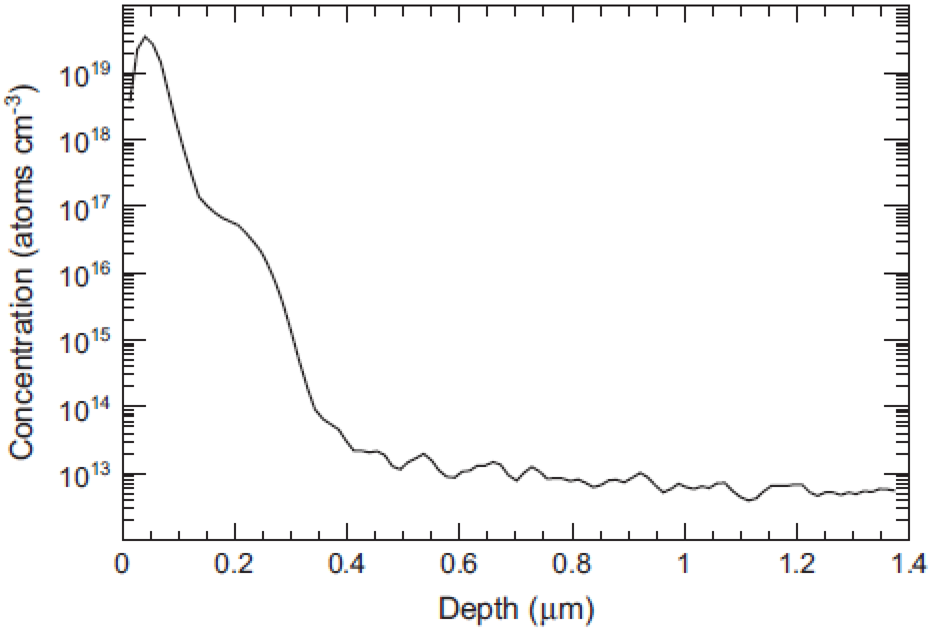
Back-processing: LBNL low-temperature process

- Low temperature process developed at LBNL: phosphorus implant at 33keV using a cold process at -160°C to create amorphous layer, followed by annealing @ 500°C (10 minutes in Nitrogen atmosphere), compatible with CMOS devices; simple process and equipment needed

- Very promising results from tests on PIN diodes: good yield and low leakage current

- Process applied to 70 μm thin SOImager-2 chips, which are fully functional after processing

- Spreading Resistance Analysis (SRA) measurements show P contact extending to 0.3 – 0.4 μm depth

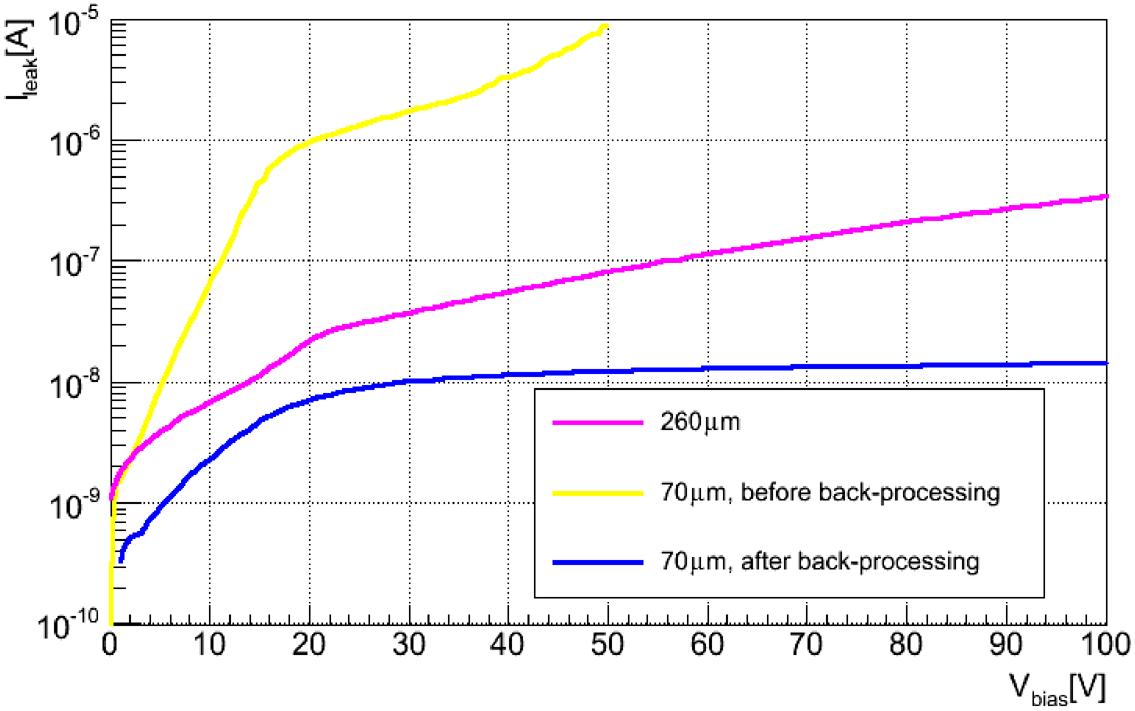


- SRA data for the implanted contact on a post-processed chip

- Expect detection threshold of 1.5 keV for 0.4 μm thick contact

[from Craig Tindall, LBNL]

Thin, back-processed SOI-Imager-2



- Good leakage current performance after back-processing; thermal annealing recovers surface damage due to back-grinding process

- **No influence of back-processing on pixel noise and conversion gain (95±6e^- consistent with 83 ±8e^- on a thick, un-processed sensor)**

X-rays characterization at the ALS

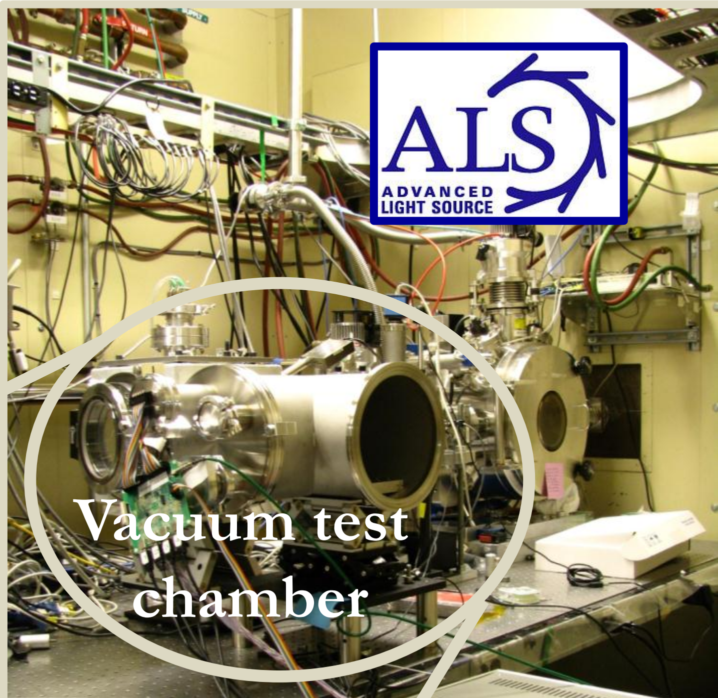
- Quantum efficiency for X-rays on the SOImager-2 studied on data collected at the 5.3.1 beamline of the Advanced Light Source at LBNL

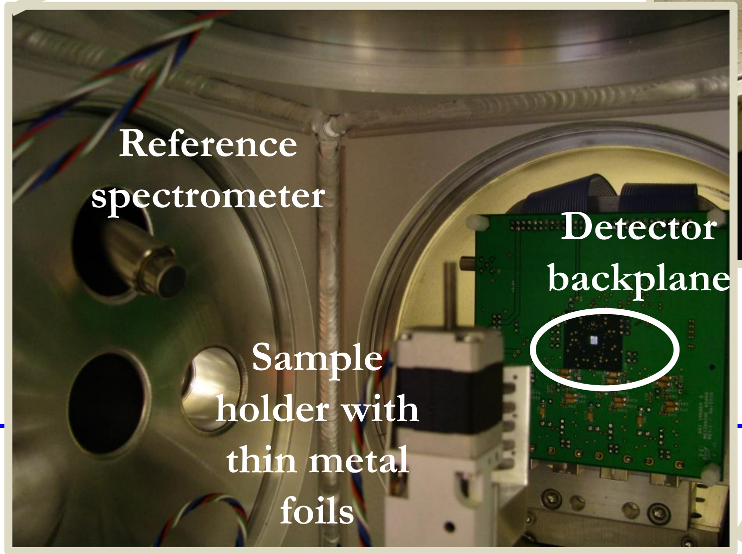
- In-vacuum test capabilities, reference spectrometer and translation stages for sample and sensor positioning

- Thin, back-processed SOI-Imager-2 sensor tested with fluorescence X-rays from metal foils in the energy range 2.1 keV< E < 8.6 keV

$$N(x) = N(0)e^{-\frac{x}{\lambda}}$$

Element	E (keV)	λ (μm)
Au	2.12	1.7
Ag	2.98	4.1
Ti	4.50	13
Fe	6.40	37
Ni	7.47	56
Cu	8.08	70
Zn	8.60	86



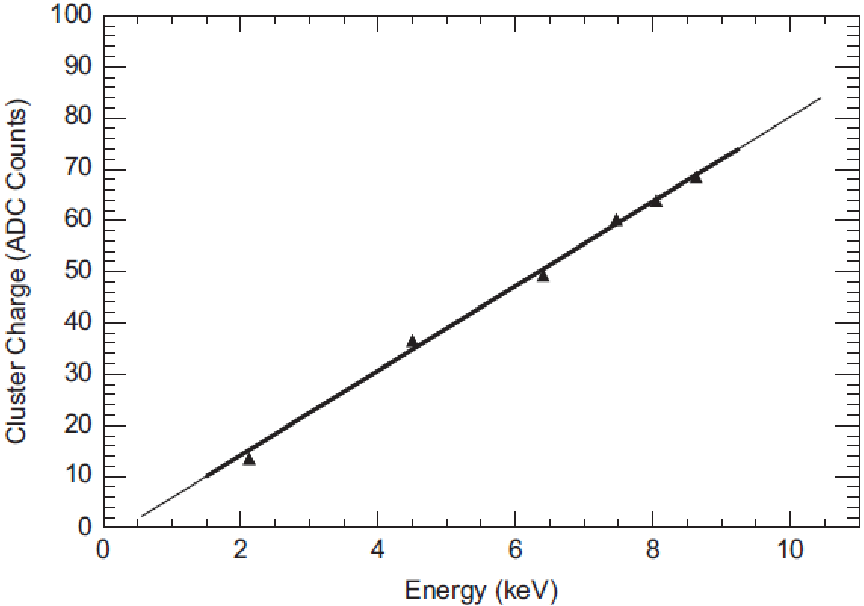


Results

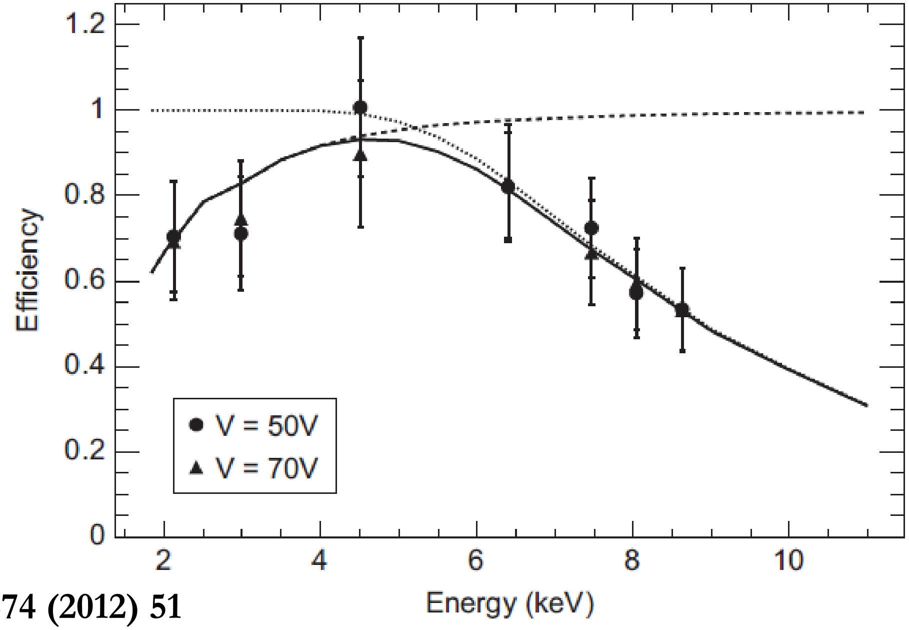
- Sensor operated in full depletion and over-depletion
- Good **pulse height linearity** as a function of X-ray energy

- **Quantum efficiency** (continuous black line) measured by comparing hit rates on SOI sensor with reference spectrometer accounting for absorption in Si (dotted line) and transmission through thin entrance window (dashed line).

Calibration and linearity



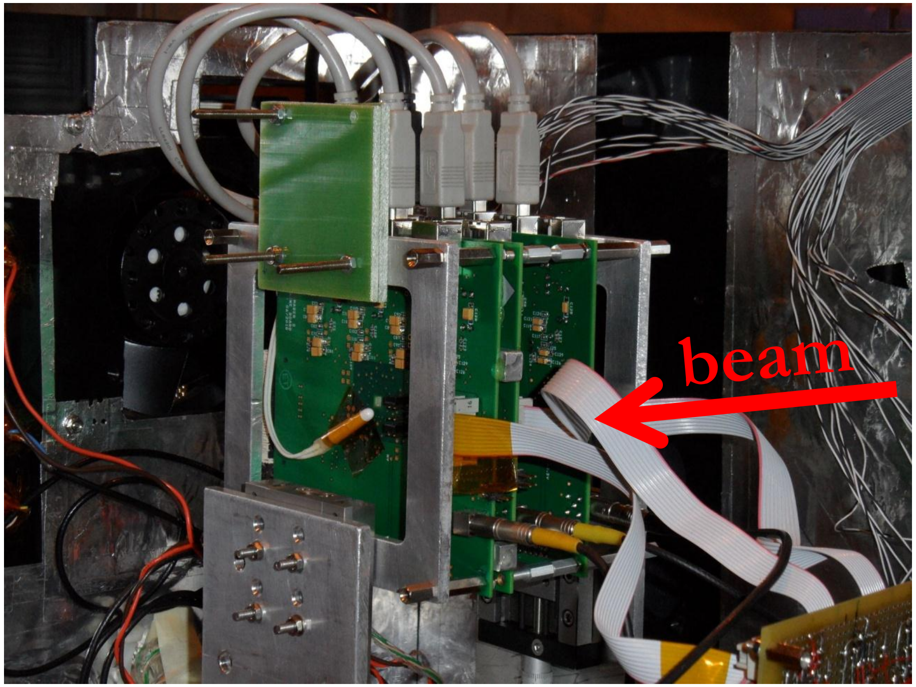
Quantum efficiency



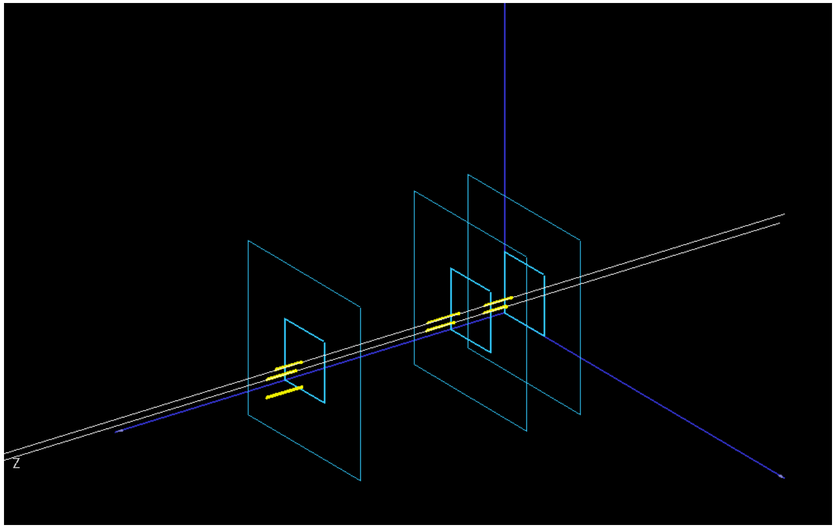
- NIM A 674 (2012) 51

Test on the thin SOImager-2

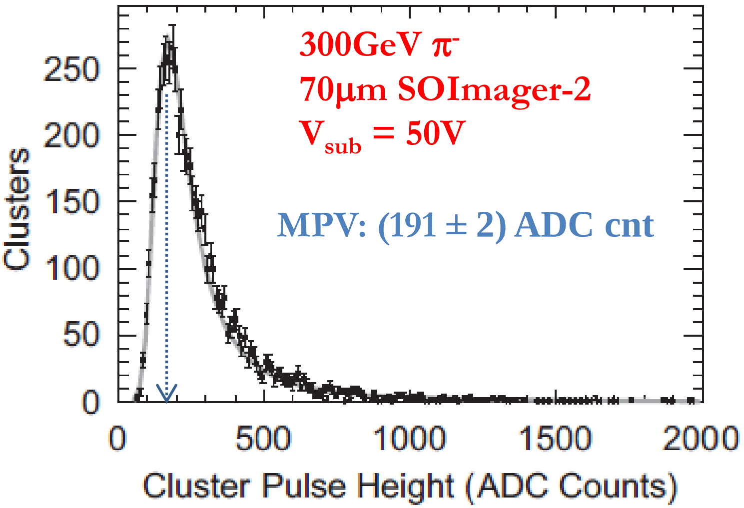
300 GeV π^- at CERN SPS

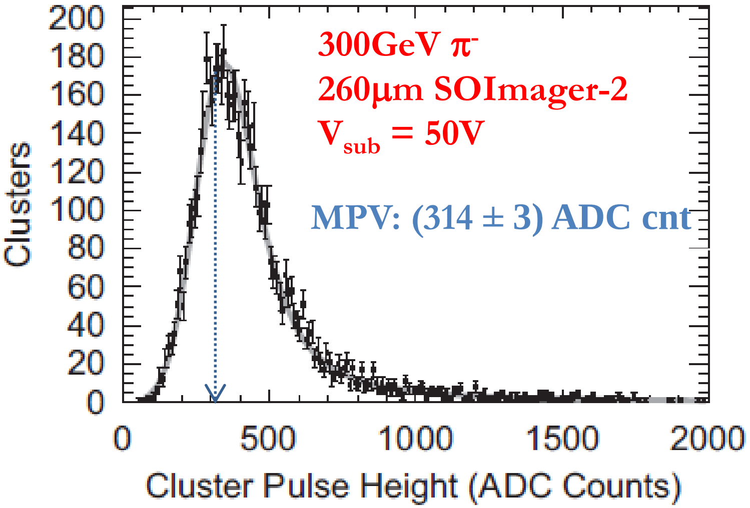


- Detectors arranged in one cemented "doublet" (2 thick detectors, 9 mm spaced) and one "singlet" (1 thin detector, 33 mm spaced).
- The doublet is optically aligned with a better than 50 µm precision ➡ easy and precise coincidence cuts in cluster recognition.
- Temperature is maintained around 20° C by cool air flow and continuously monitored.



MIP detection: thick vs thin sensor





- Ratio of Pulse height: 0.61 ± 0.01
- Ratio of estimated sensitive thicknesses: 0.62 ± 0.05

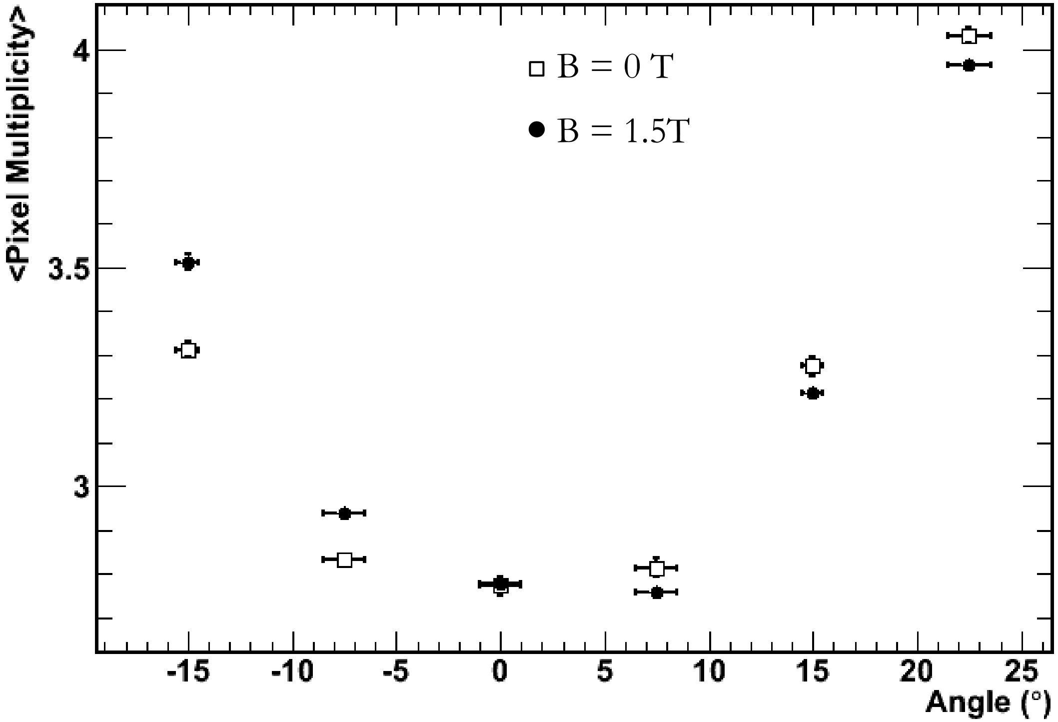
⬇

Perfect agreement

- **NIM A 676 (2012) 50**
- **NIM A 681 (2012) 61**

SOI sensor	V_{sub} (V)	Cluster <S/N>	Efficiency	σ_{point} (μm)
Thin	30	25.0	0.90 ± 0.04	3.1 ± 0.80
Over depletion	50	28.2	0.94 ± 0.03	1.7 ± 0.50
	70	28.8	0.96 ± 0.03	1.8 ± 0.60
	90	31.2	0.98 ± 0.02	1.9 ± 0.70
Thick	30	23.3	0.89 ± 0.03	1.36 ± 0.04
	50	47.4	$0.98^{+0.02}_{-0.04}$	1.12 ± 0.03
	70	52.7	$0.99^{+0.01}_{-0.05}$	1.07 ± 0.05

Lorentz angle measurement



Measurement on a thick detector at V_{sub} = 70V

Measurement repeated at the end of July on a thin detector, but data analysis still ongoing

	B = 0 T	B = 1.5 T
V_{sub} = 70V	0.14 ± 0.14	1.71 ± 0.11

Summary & Outlook

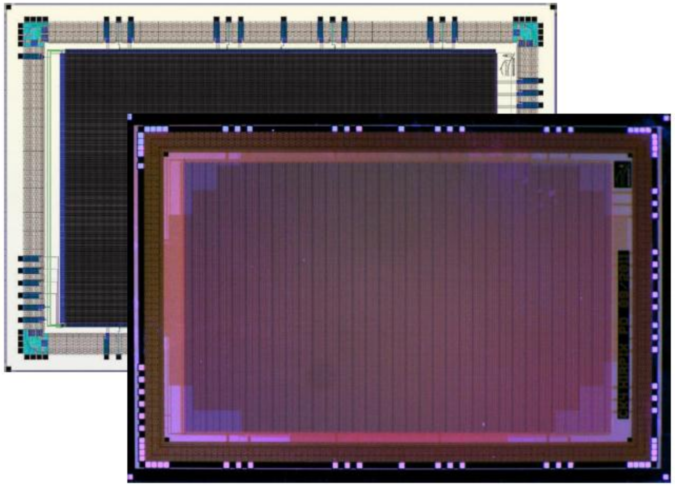
- LBNL, Padova and UC Santa Cruz are involved in SOI monolithic pixels R&D in LAPIS deep-submicron FD-SOI technology since about 2006 (with more than 7 prototypes).

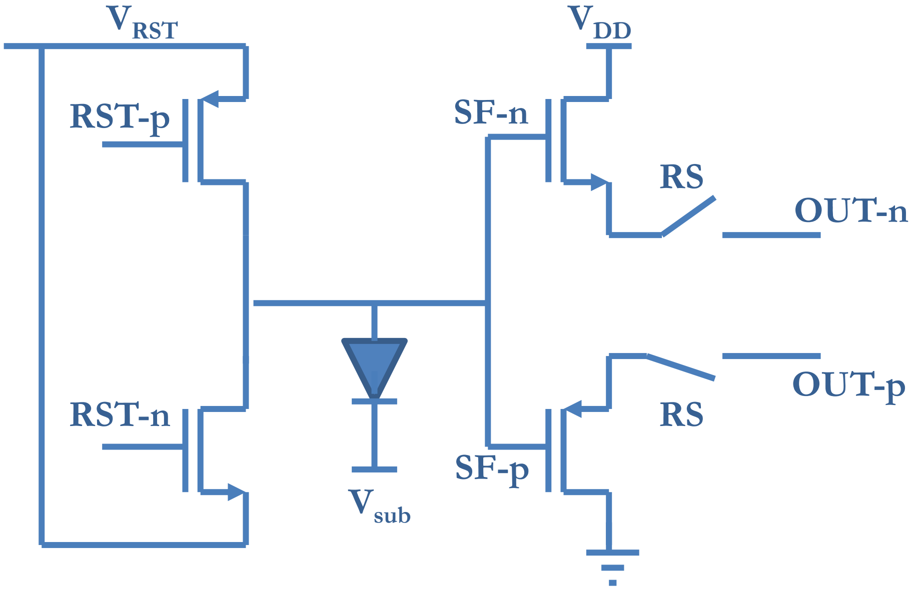
- Introduction of **Buried P-Well (BPW)** implant led to pixel layouts operable at up to 100 V depletion voltages, showing very good performance for MIP tracking.

- Thinning the sensor substrate and providing a conductive entrance window enable **full depletion operation**. Very encouraging results from first X-ray characterization at 2-9 keV and with MIPs.

- Looking forward to exploring **high-resistivity, FZ-Si substrates**, that should provide higher quality sensor substrates (lower leakage, better energy resolution) and achieve full depletion at low voltages.

New test chips on High Resistivity substrates



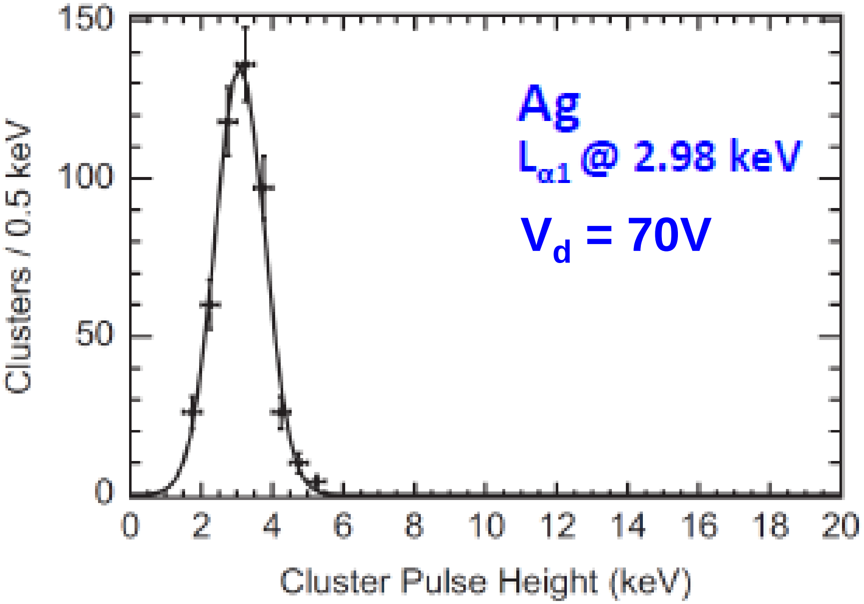


- $V_{RST} = 0$ for n-type substrate
- $V_{RST} = V_{DD}$ for p-type substrate

- 0.20 µm LAPIS process, Oct 2011 submission
- 512 × 320 analog pixels, 13.75 µm pitch
- Complementary architecture for both p-type and n-type substrates
- Devices on CZ substrate (HR1, n-type) and FZ-p arrived in June (evaluation ongoing). HR3 (n-type) and FZ-n to arrive soon!

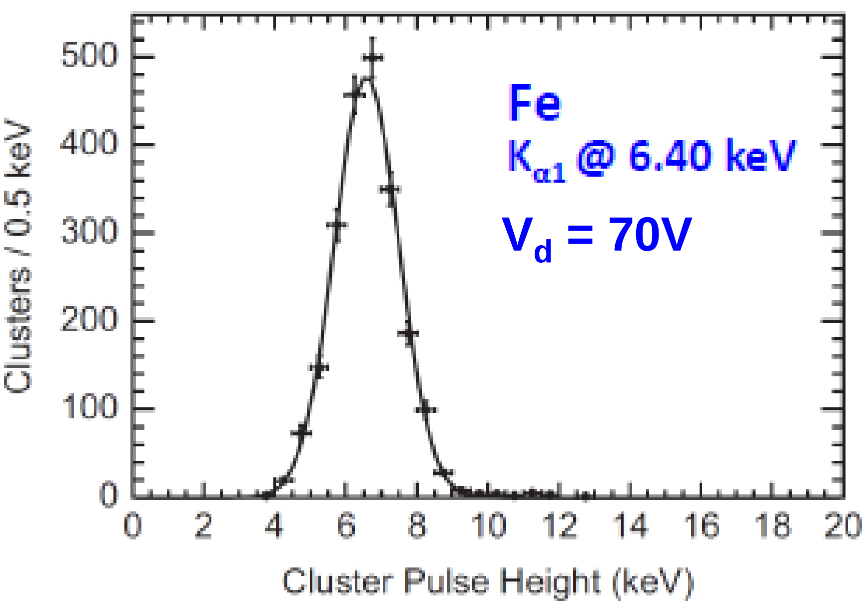
Backup Slides

Energy resolution



Fitted Gaussian width

(0.70 ± 0.03) keV

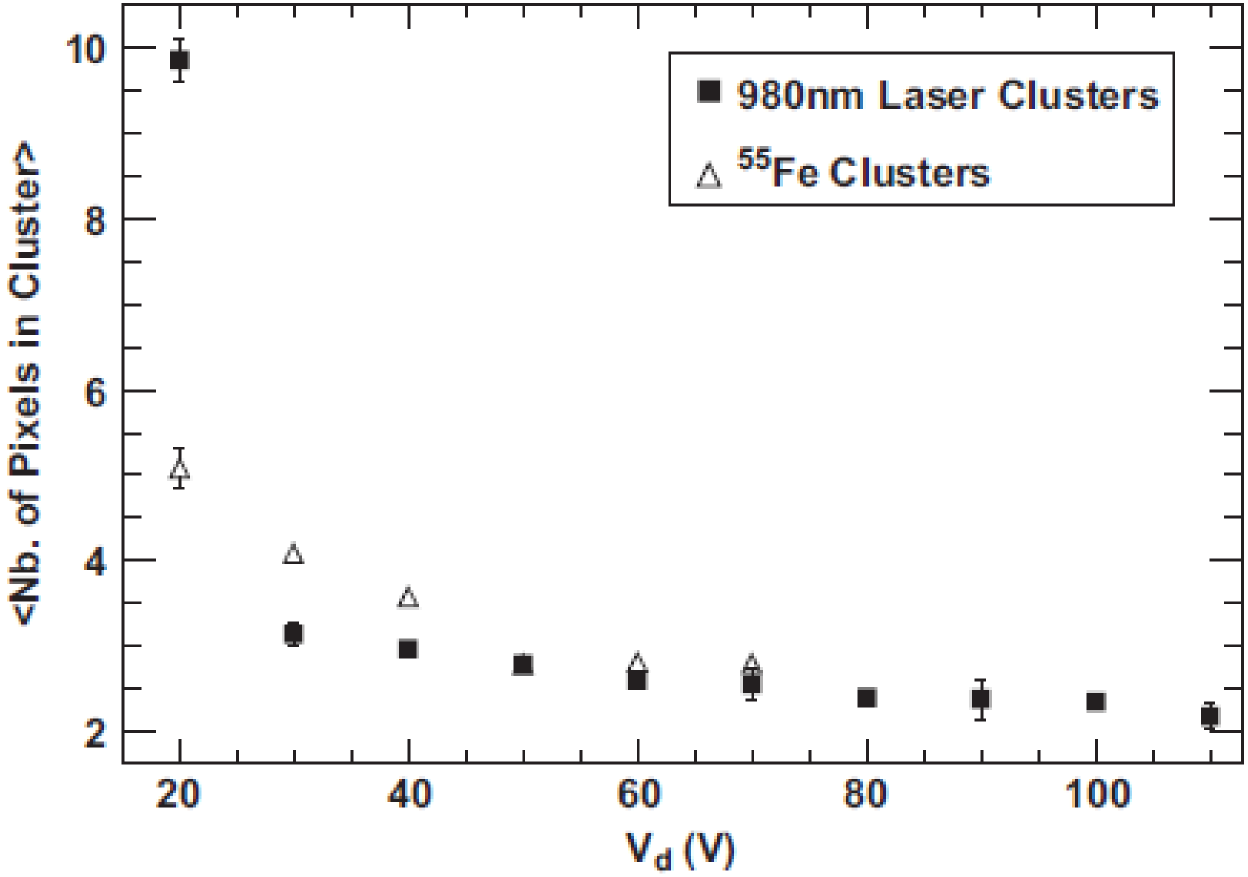


Fitted Gaussian width

(0.99 ± 0.02) keV

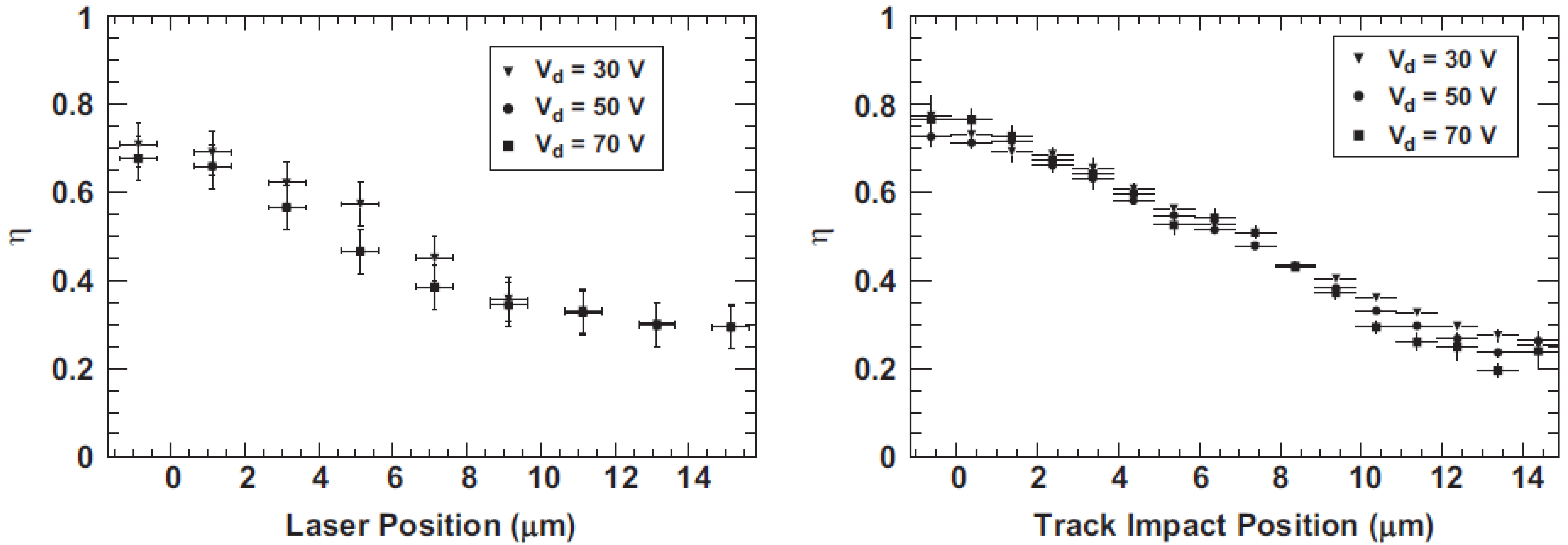
Pixel multiplicity

Pixel multiplicity in signal clusters as a function of V_{dep} for 980nm laser pulses (filled squares) and 5.9keV X-rays (open triangles).



- Cluster size decreases with V_{dep} as expected
- Signal is distributed among multiple pixels also for large voltages: capacitive coupling?

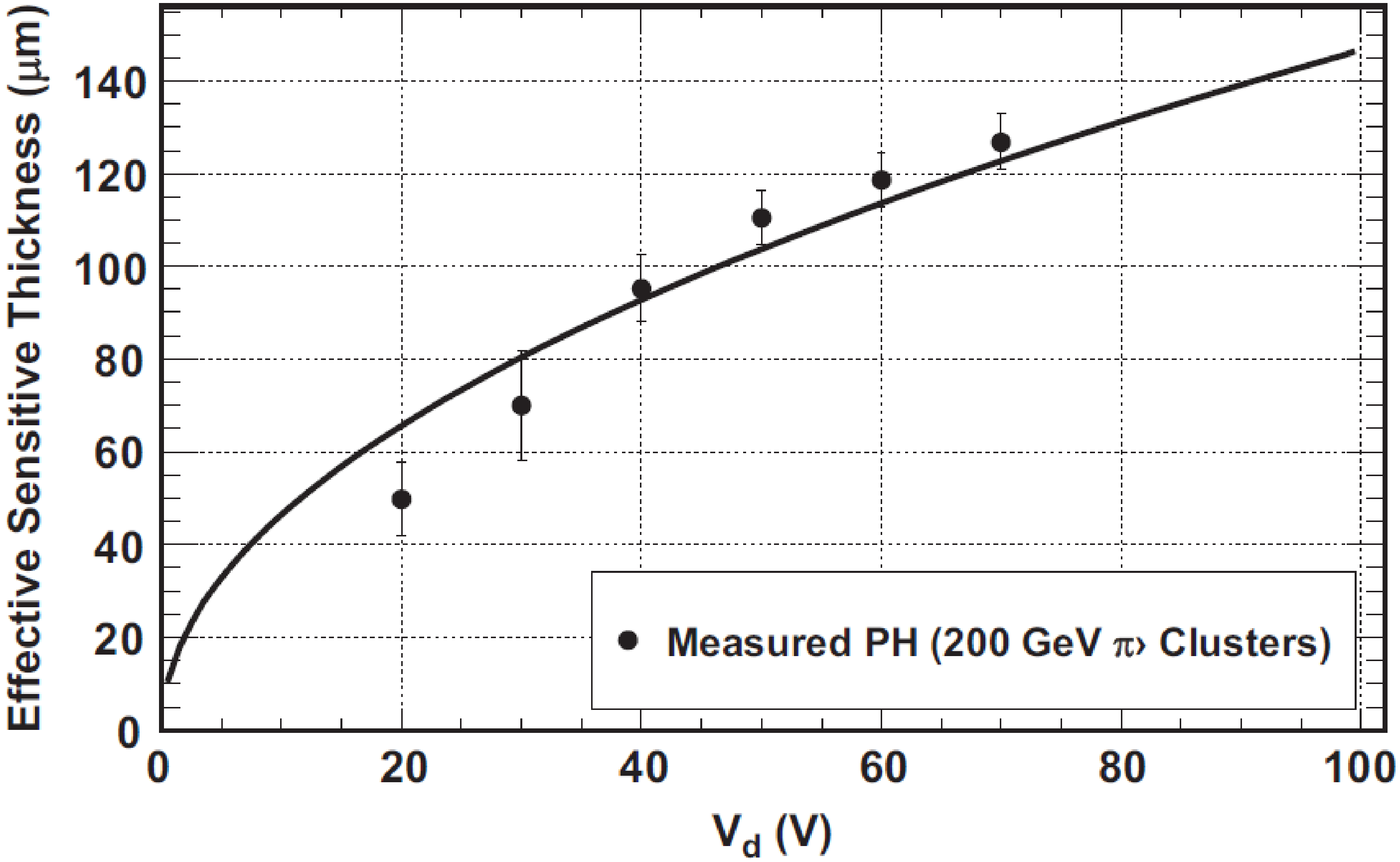
Charge sharing



η distribution at different values of V_d for (left) 980nm laser pulses and (right) 200GeV π.

- Small variation of the η distribution with V_d using the980nm laser and no significant variation with energetic pions.
- Charge sharing among neighboring pixels is not dominated by the charge carrier cloud size and that, instead, the pixel capacitive coupling plays a significant role in determining the observed signal distribution

Depletion thickness

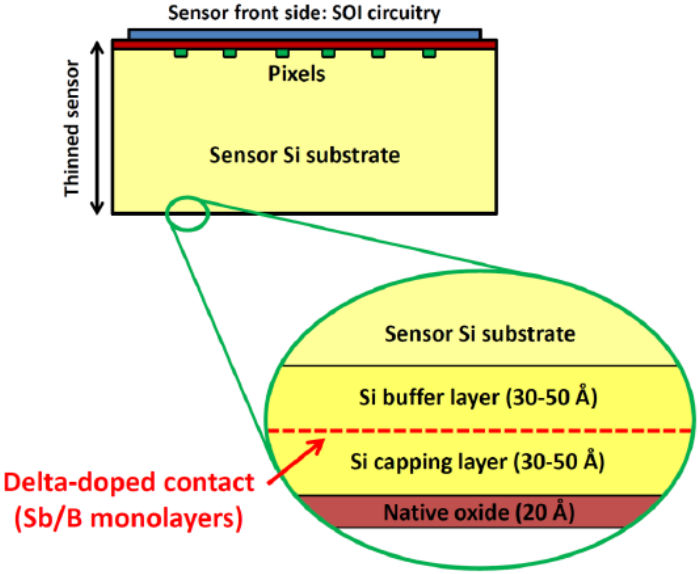


MBE

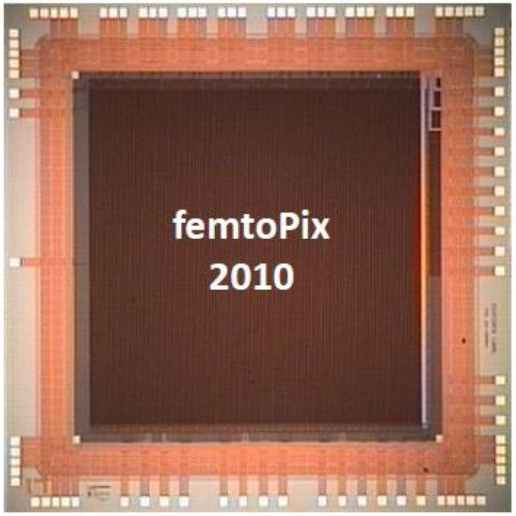
- Molecular Beam Epitaxy (MBE) system being acquired, expected to be operational by mid-2013

- Conductive implants few atomic layers thin created by evaporation in ultra-high vacuum (“delta doping” approach first demonstrated by NASA/JPL); final contact thickness ~ 10nm

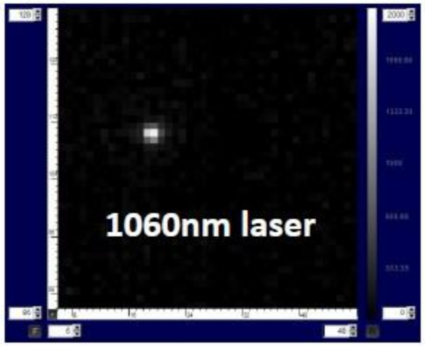
- Low thermal budget (< 450°C) technique, applicable to full-processed devices



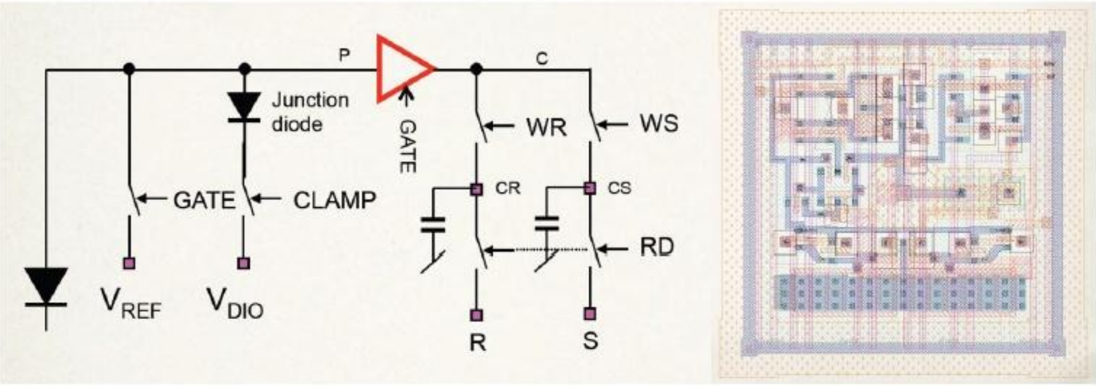
Other applications: FemtoPix

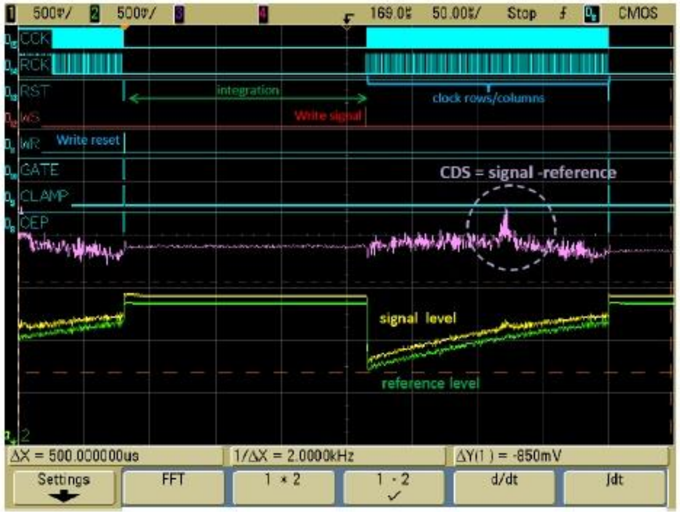


- OKI/Lapis 0.20 μm process, Jan. 2010 submission
- ns-gateable, high frame, direct soft X-ray pixel sensor for ultrafast X-ray absorption spectroscopy at ALS BL 6.0 (fs e^- bunch slicing)
- 192×192 pixels, 17.5×17.5 μm^2; clamped reset, in-pixel gated amplifier and storage nodes for Correlated Double Sampling (CDS)
- Testing in progress



Pixel sketch

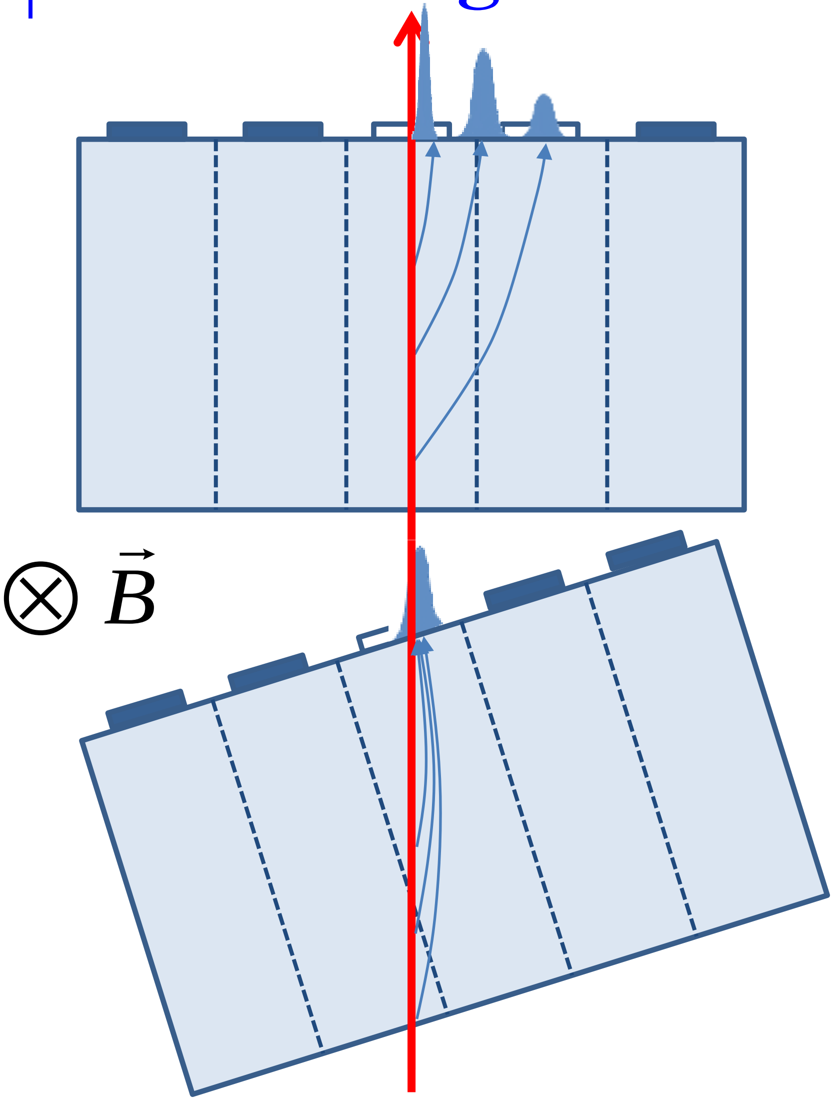




HEP requirement for radiation hardness

Machine	Luminosity $[cm^{-2}\ s^{-1}]$	Non Ionizing Fluence $[n_{eq}\ cm^{-2}\ yr^{-1}]$	Ionizing Fluence $[krad\ yr^{-1}]$
LHC	10^{34}	1.4×10^{14}	11300
HL-LHC	10^{35}	1.4×10^{15}	71400
CLIC	10^{34}	1.0×10^{11}	50
Super B	$> 10^{36}$	3.5×10^{12}	3000

Lorentz angle



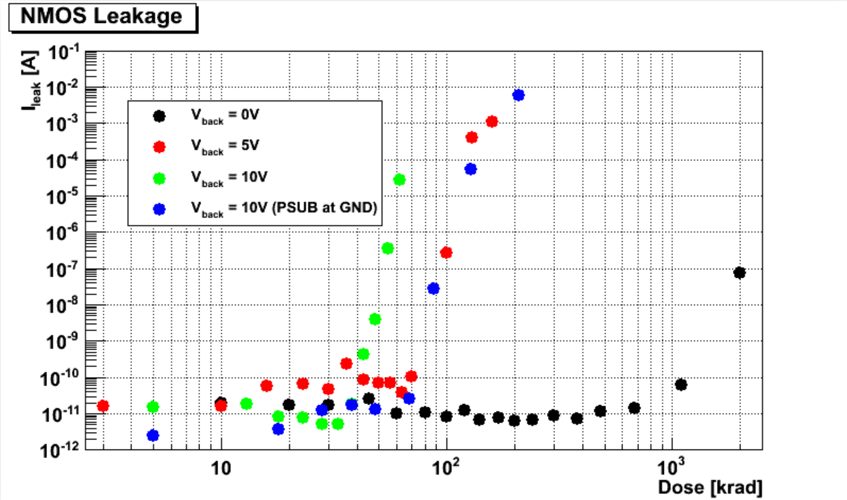
- In the presence of an electric field (E) and a magnetic field (B), the charge carriers released by a charged particles in the detector drift along a direction at an angle **Θ_L (Lorentz angle)** with respect to the electric field direction

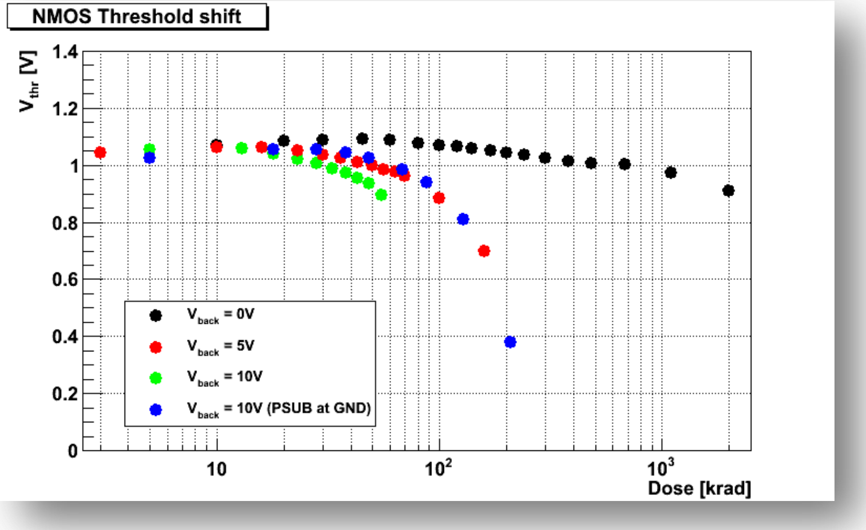
- The charge usually spreads over several pixels, depending on the angle of the incident particle

- The spread is minimum for an incident angle equal to the Lorentz angle

- Knowledge of this angle is needed to optimize the spatial resolution by tuning the angular orientation of the detectors

Radiation damage studies on the 0.20 μm process



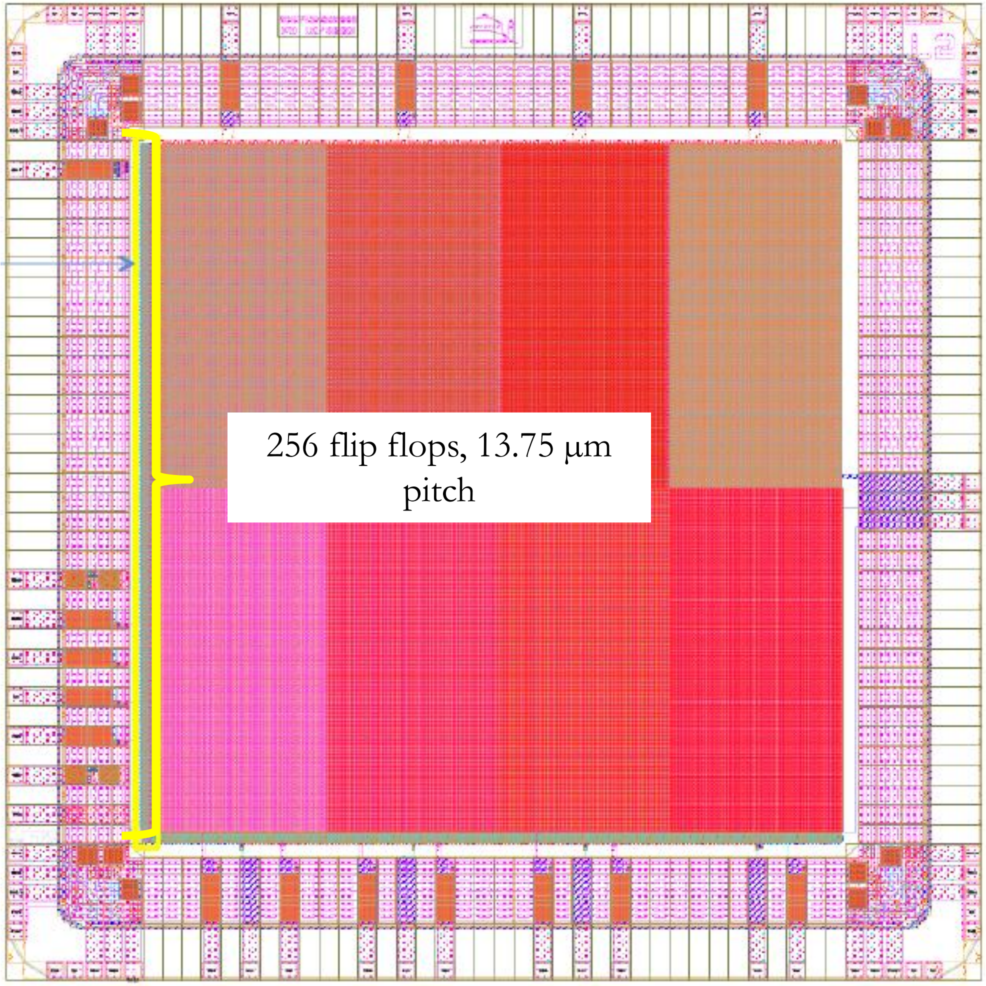


- X-ray irradiation (10 keV L-line photons.) on single transistors 0.20 μm FD process). Irradiations in air at room temperature. Dose rate: 165 rad(SiO_2)/sec.
- NMOS and PMOS transistors, each surrounded by 1μm PSUB guard ring
- NMOS and PMOS Body of Body-Tie transistors at 0V. Drain and source at 0V, gate NMOS HIGH (1.8V), gate PMOS LOW (0V).
- V_{back} = 0V, 5V, 10V with PSUB guard-ring floating; V_{back} = 10V with PSUB guard-ring at 0V

For V_{back} = 0V the transistor is still working properly up to doses of ~100krad.

The PSUB guard-ring tied at GND during irradiation indeed limits the electrical field through the BOX and improves the radiation hardness of the device.

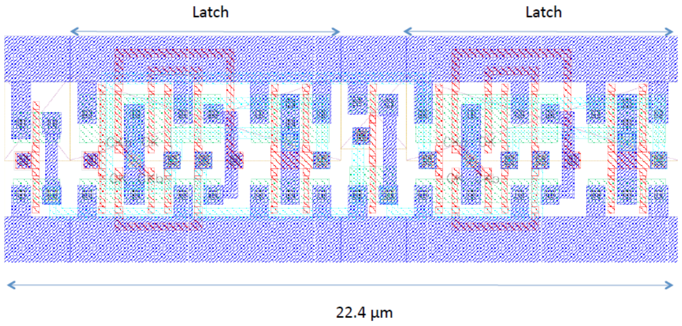
Single Event Upset tests



256 flip flops, 13.75 µm pitch

- We tested the technology for **SEU sensitivity**.
- The periphery **shift register** for row-selection has been used to check for bit-flip through a dedicated test pad.
- **Mind: the design is not hardened in any special way against SEU!**

FLIP-FLOP layout



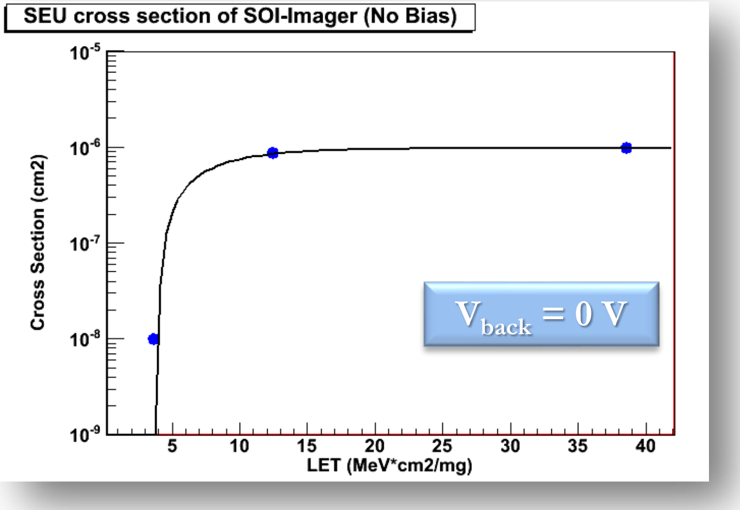
SEU cross section

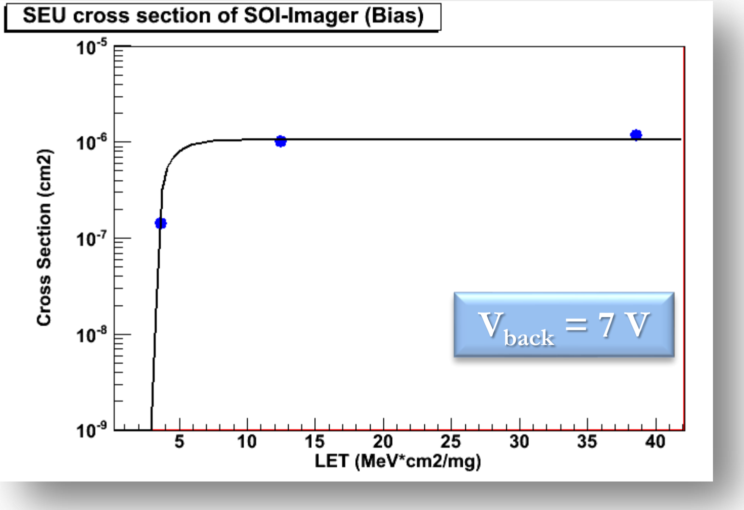
- A Single Event Upset (SEU) study was performed at the **SIRAD irradiation facility**, located at the 15MV Tandem XTU-Accelerator of the INFN Legnaro National Laboratory.

- A known logical pattern is written in and read back from the row selection shift register through dedicated pads during irradiation. Differences between the loaded and read-back pattern highlight a SEU occurred in the cells

- Irradiation performed with three different ion species and, for each ion beam, for two substrate bias conditions (V_{back} = 0V - 7V).

Ion species	Energy (MeV)	LET_0 in Si ($MeV \cdot cm^2/mg$)
^{19}F	118	3.67
^{35}Cl	170	12.5
^{79}Br	240	38.6





No apparent difference with or without bias

- $LET_{thr} \sim 4\ MeV \cdot cm^2/mg$
- $\sigma_{sat} \sim 10^{-6}\ cm^2$