Evaluation of novel n^+-in-p pixel and strip sensors for very high radiation environment

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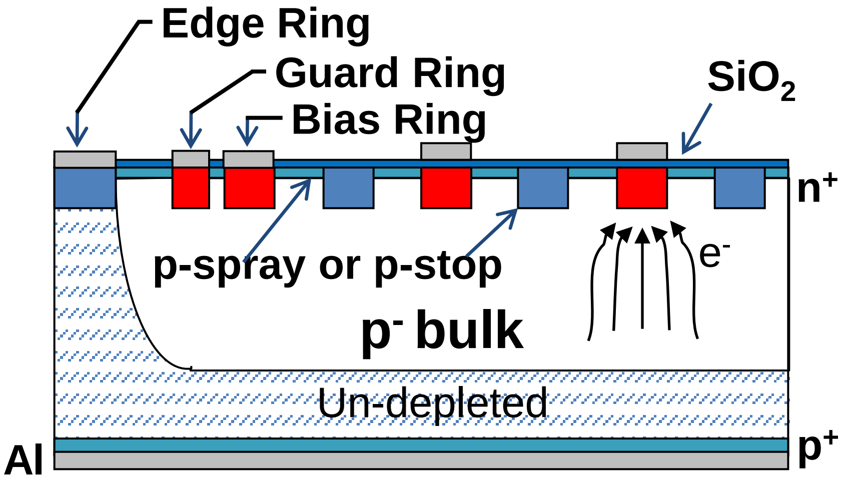
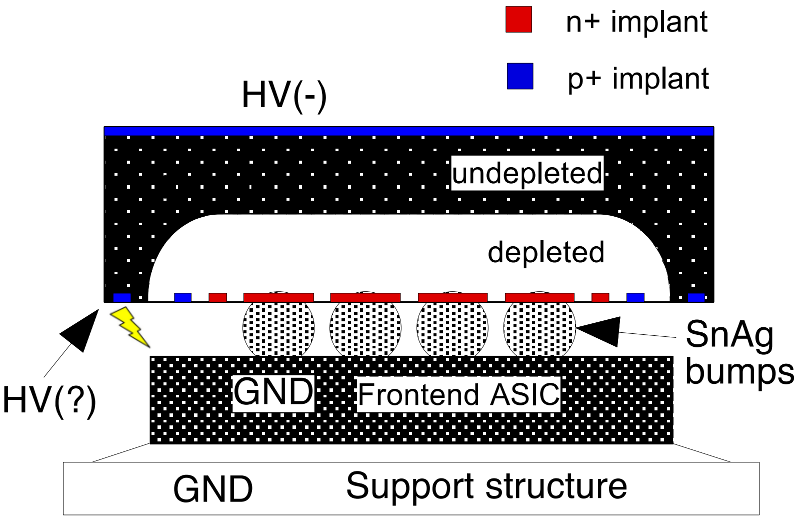
n^+-in-p Benefits and Issues

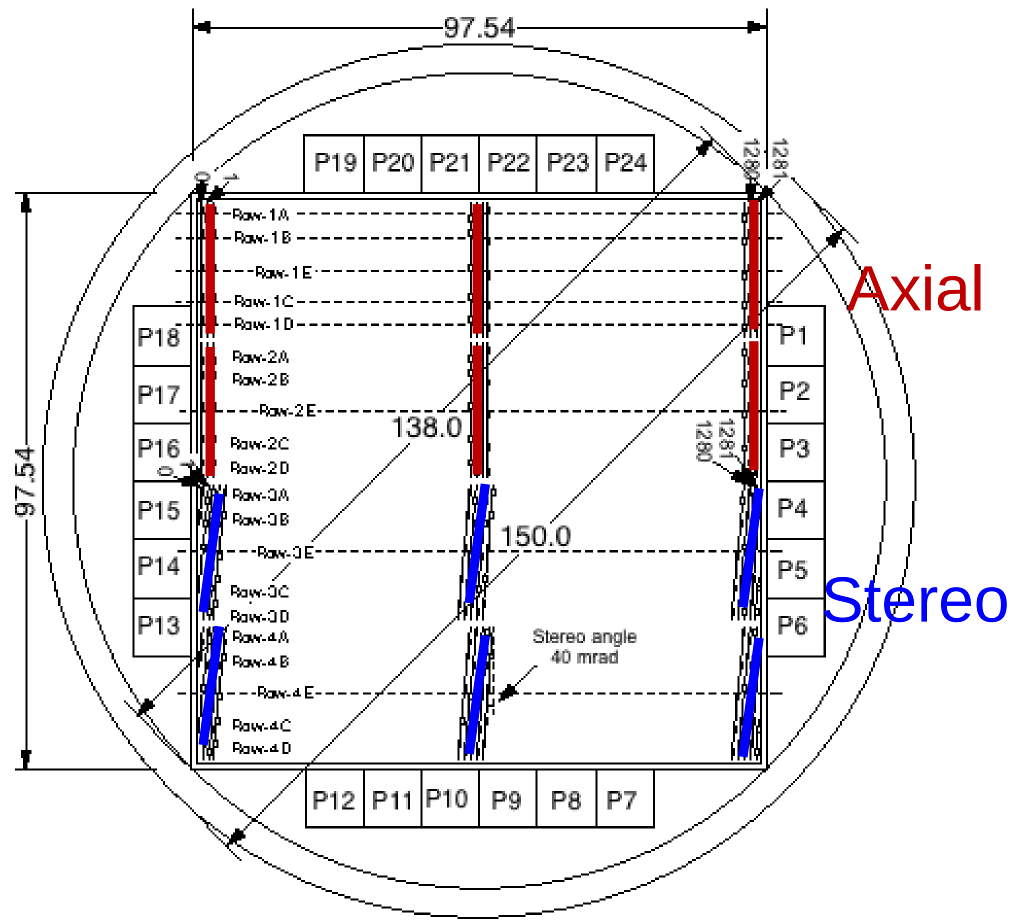
- Starting with "p-type" silicon, with n^+-readout , (n-in-p), has benefits:
  - Tolerance against radiation (bulk) damage
    - Depletion from the readout side always
    - Good signal even partially depleted, initially or heavily damaged towards the end of life
  - Collecting faster carrier, electrons
    - Larger signal, reduced charge trapping
  - Single-sided process
    - Cheaper than double-side process
    - More foundries and available capacity, world-wide
  - Easier handling/testing
    - due to more robust back-side than patterned
  - Wafer availability in 6-in. with higher resistivity
- Specific requirements
  - N-side Isolation
    - against electron-layer in the silicon surface attracted to the "positive" charges in the Si-SiO_2 interface
    - p-stop or p-spray
  - Bias structure
    - if AC-coupling readout, e.g., strip sensors
    - if requesting testability in DC-coupling, e.g., pixel sensors
  - HV protection
    - between the front edge and the ASIC, in hybrid pixel modules





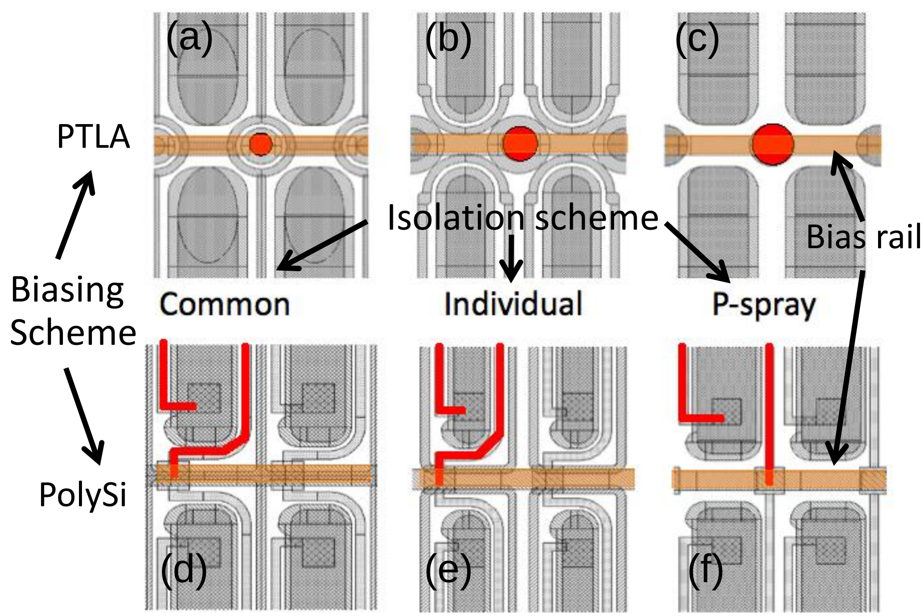
Novel n$^+$-in-p Strip Sensors

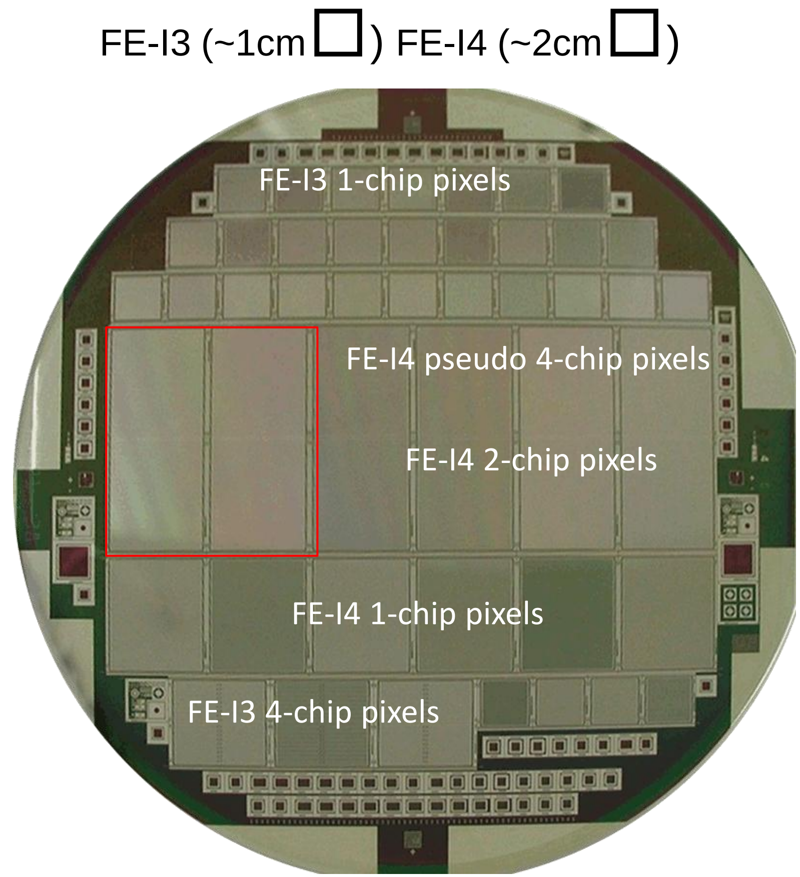
- Collaboration of ATLAS with Hamamatsu Photonics K.K. (HPK)
- Silicon wafers
  - 6 in., p-type, FZ <100>, 320 µm thick wafers
  - >3 kΩ cm wafers available industrially
- Strip sensors
  - large area
    - 9.75x9.75 cm^2 sensors
  - 4 segments
    - 2 axial, 2 stereo
    - 1280 strip each, 74.5 mm pitch
  - Miniature sensors
    - 1x1 cm^2 for irradiation studies
  - Y. Unno, et. al., Nucl. Inst. Meth. A636 (2011) S24-S30
  - And the poster (ID=8)



Novel n^+-in-p Pixel Sensors

- n-in-p 6-in. wafer process in HPK
  - ATLAS FE-I3 and FE-I4 pixel sensors
  - Isolation structures
    - p-stop (common, individual) or p-spray
  - Biasing structures
    - Punth-thru dot at 4-corner (PTLA) or PolySi resister
    - "Bias rail" is a metal over insulator, no implant underneath.
    - No electrode in the silicon, other than the bias "dot"
  - Y. Unno et al., Nucl. Instr. Meth. A650 (2011) 129–135



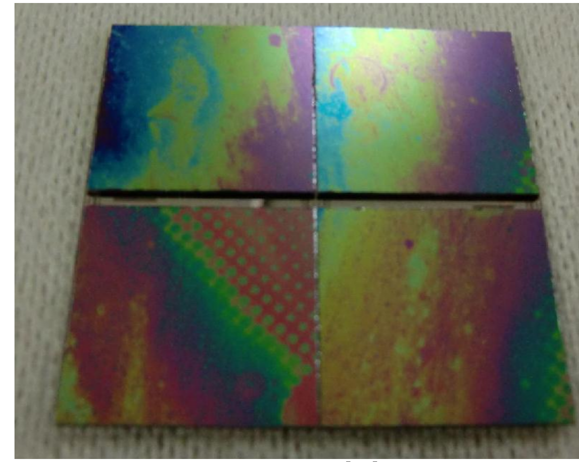


HPK n-in-p 6-in. wafer

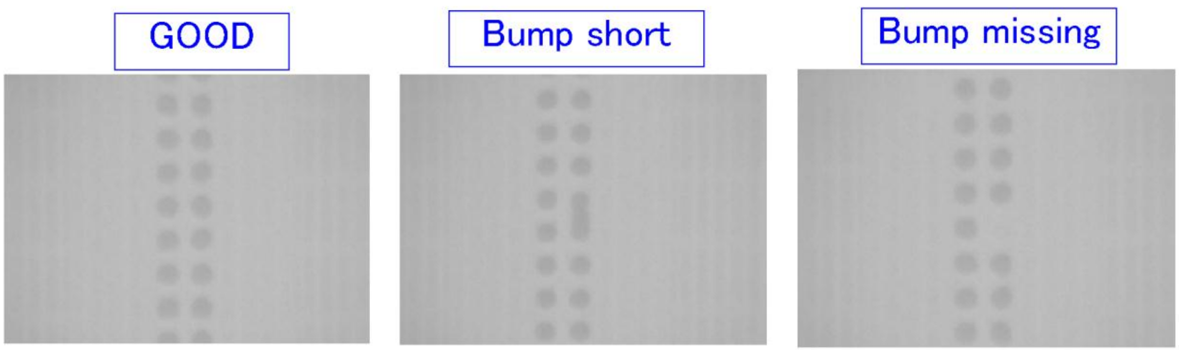
Thinned sensors
- Finishing 320 μm wafer process first
- Thinning the wafers to 150 μm

Pixel modules - Bumpbonding

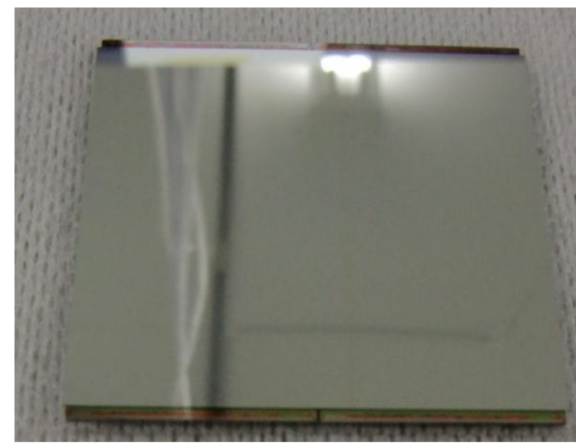
- Latest achievement
  - Lead-free bumps (SnAg)
  - 4 cm x 4 cm pixel sensor
  - 4x FE-I4 (2 cm x 2 cm) readout ASIC's
  - 80 col.*336 row*4 chips =1M bumps
  - A sample in the HPK display table



ASIC side



Most of bumps(>about 99.8%) look "GOOD".
But, some of bumps have short or missing.
We are trying to improve the yield.

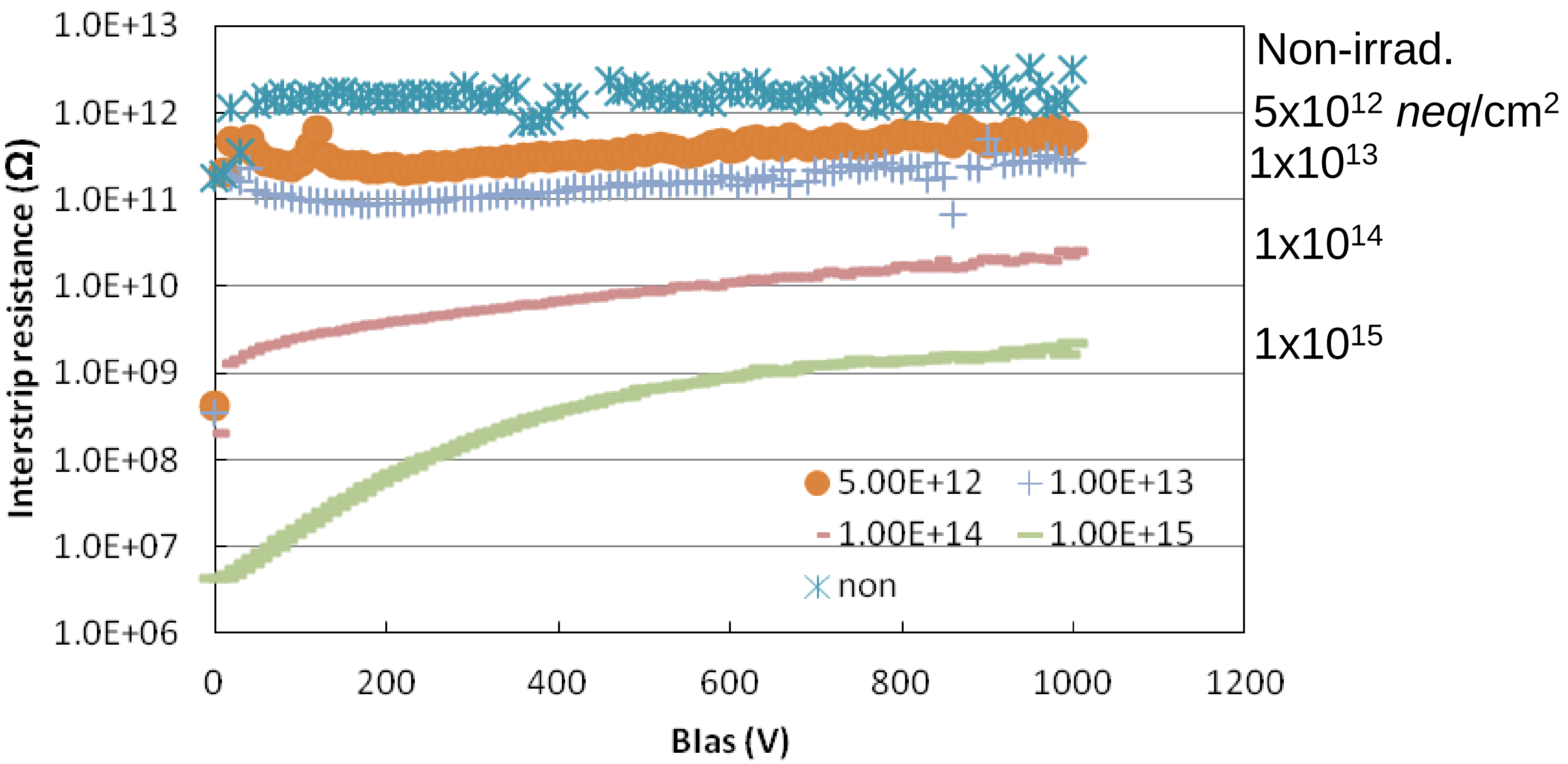


Sensor side

The goals of R&D

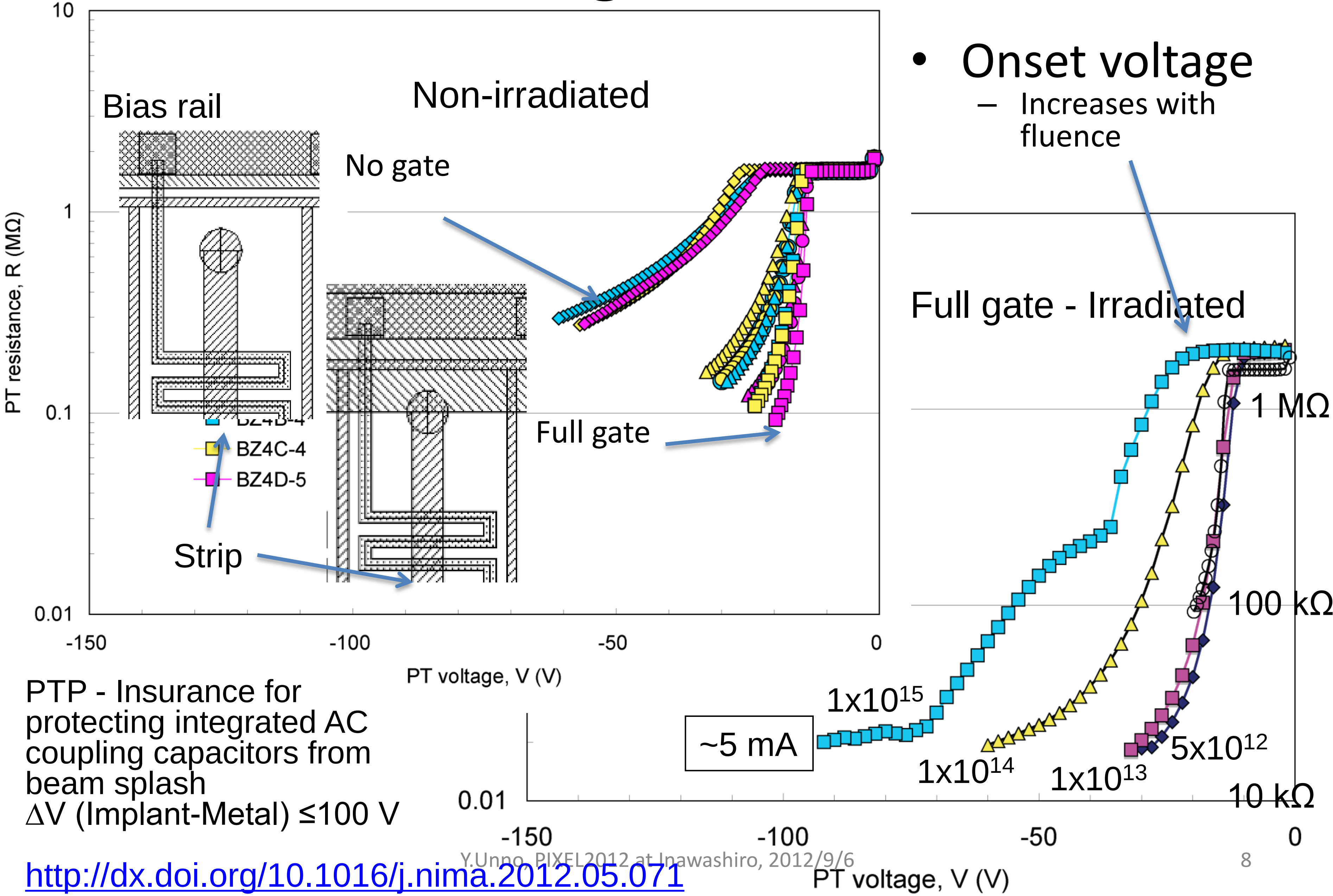
- Application
  - For the very high radiation environment, e.g.,
  - High-Luminosity LHC which aims to collect data of 3,000 fb^{-1}
    - Presently running LHC goal is 300 fb^{-1}
- Fluences of hadronic particles in HL-LHC
  - Pixels: ~2×10^{16} 1-MeV neutron-equivalent (*neq*)/cm^2
  - Strips: ~1×10^{15} *neq*/cm^2
- Understanding of the radiation effect, specially in the surface, after the studies of irradiated sample:
  - Surface resistance – Interstrip resistance
  - Punch-thru onset voltage – PTP structures
  - Effect of the surface potential – Bias rail, Bias-PTP gate
  - Potential of the p-stop

Interstrip Resistance



- Interstrip resistance
  - decreases with fluence
  - increases with bias voltage

PTP Onset Voltage – after irradiation



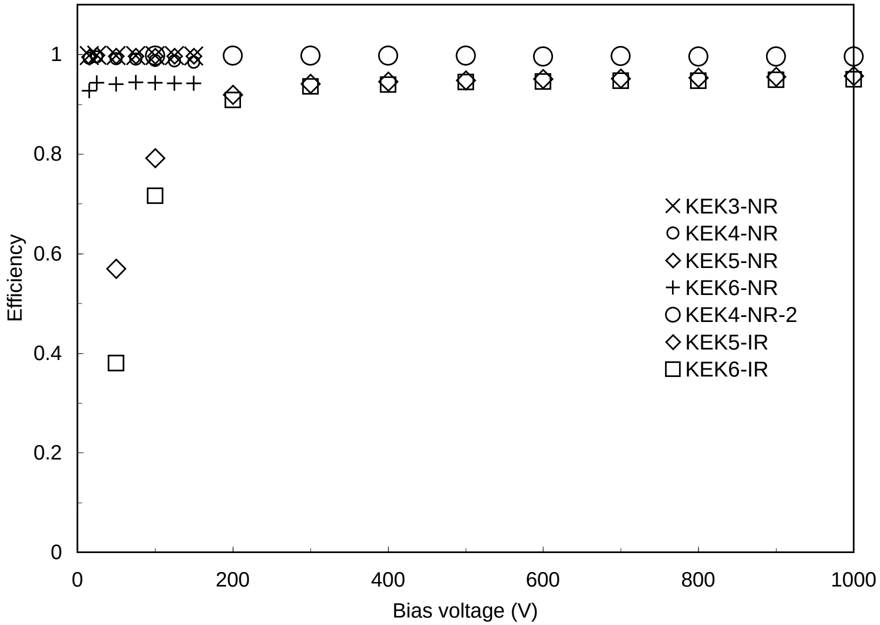
- Onset voltage
  - Increases with fluence

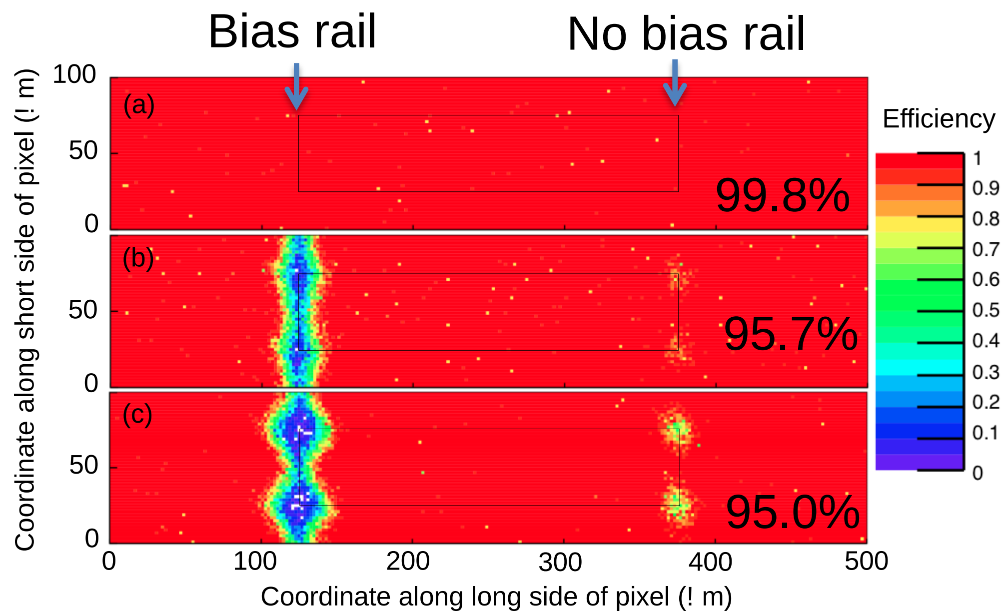
PTP - Insurance for protecting integrated AC coupling capacitors from beam splash

ΔV (Implant-Metal) ≤100 V

http://dx.doi.org/10.1016/j.nima.2012.05.071

Bias Rail Effect – after irradiation





(a) PolySi x p-stop (b) PolySi x p-stop, 2×10^{15}

(c) PTLA x p-stop

	1st beamtest	2nd beamtest
SCC93	[a]99.7±0.005% (NR)	N/A
SCC94	[a]98.7±0.01% (NR)	[b]99.6±0.01% (NR)
SCC95	[a]99.7±0.01% (NR)	[c]95.6±0.02% (IR)
SCC96	[a]94.2±0.02% (NR)	[c]94.9±0.02% (IR)

Weighted averages and errors of: [a](100, 125, 150 V), [b](100, 200, 300 V), [c](800, 900, 1000 V)

http://dx.doi.org/10.1016/j.nima.2012.04.081

- **Beamtests** with MIP particles
- Thin (150 μm) FE-I4 pixel sensors
- Irradiation (2×10^{15} *neq*/cm^2)
  - Successful operation up to 1000 V
- Reduction of efficiency specially underneath the bias rail

Insensitive area - after Irradiation

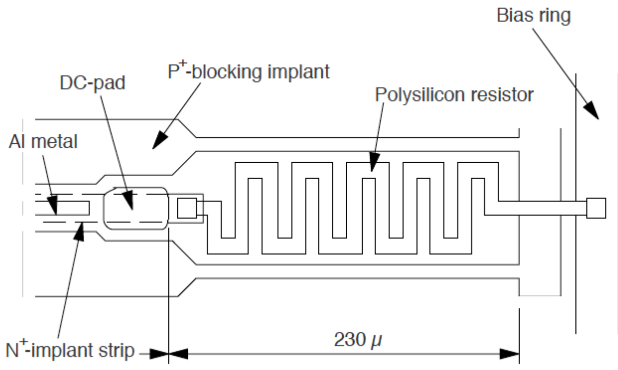


Fig. 9 Structure around the polysilicon bias resistor of the n-side. The n^+-implant strip ends at the DC-pad; no n^+-implant strip was designed under the bias resistor in this detector.

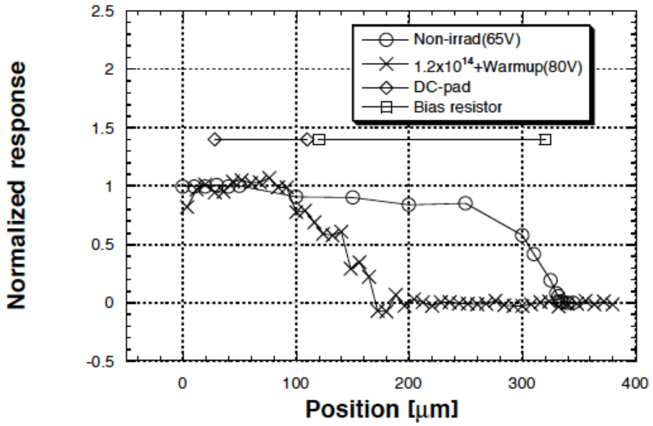
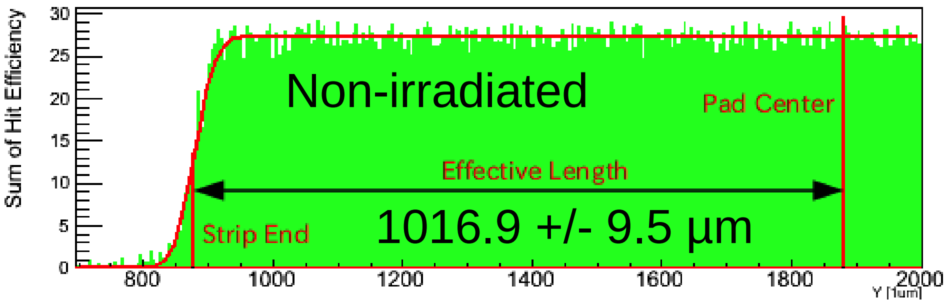
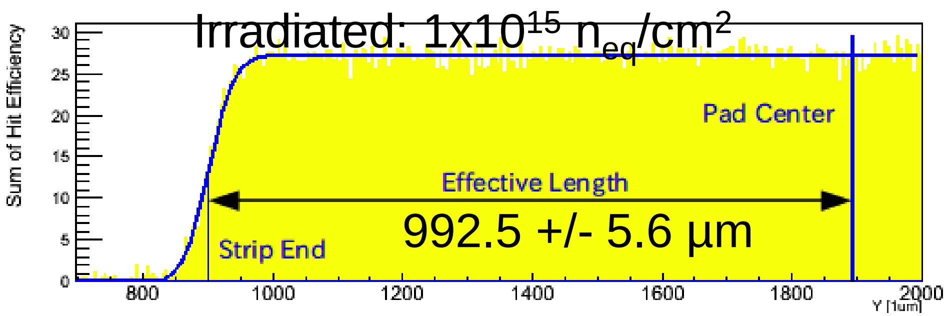
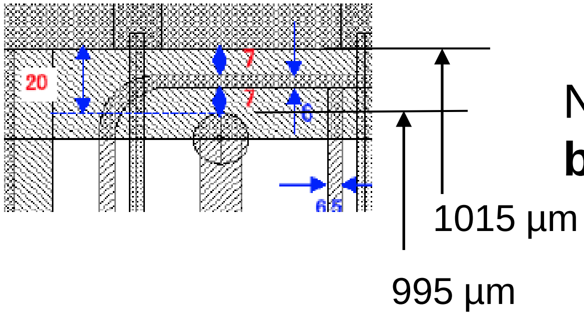


Fig. 10 The charge collection under the bias resistor where no n^+-implant strip was fabricated has been measured by using a laser light (1064 nm). The laser response was obtained for non-irradiated (circle) and the irradiated (cross) detectors. The areas of the bias resistance (square) and the DC-pad (diamond) are shown together.

Y. Unno et al., IEEE TNS 44 (1997) 736-742







New result from a **beamtest** (Poster ID=52)

- Underneath the gate (metal) seems insensitive after irradiation
  - 20 μm width

Sensor Edge – Field Width

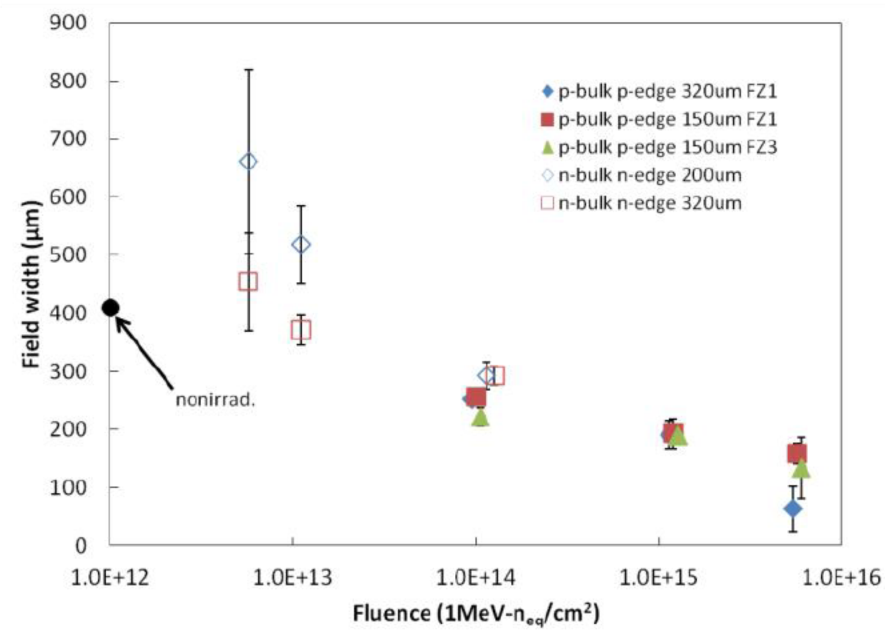
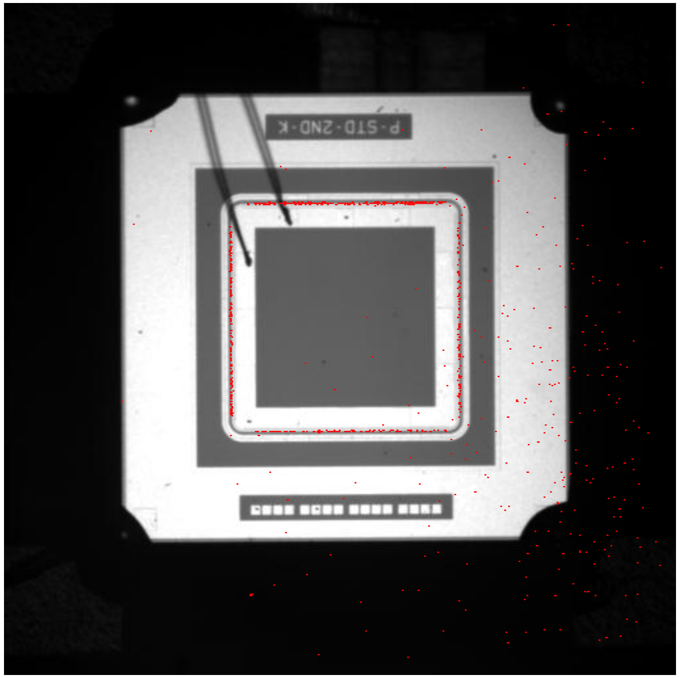
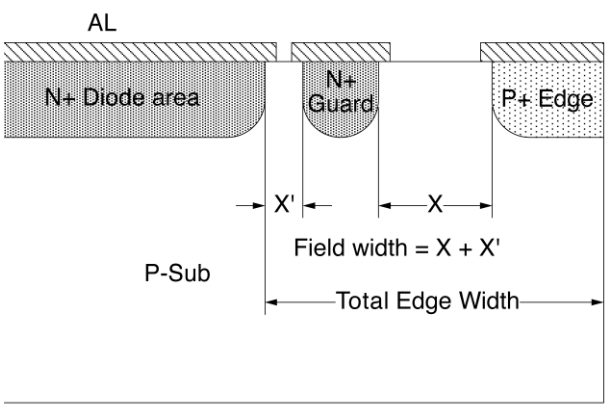


Figure 5: Fluence dependence of field width hold up to 1000 V.

http://dx.doi.org/10.1016/j.nima.2012.05.071

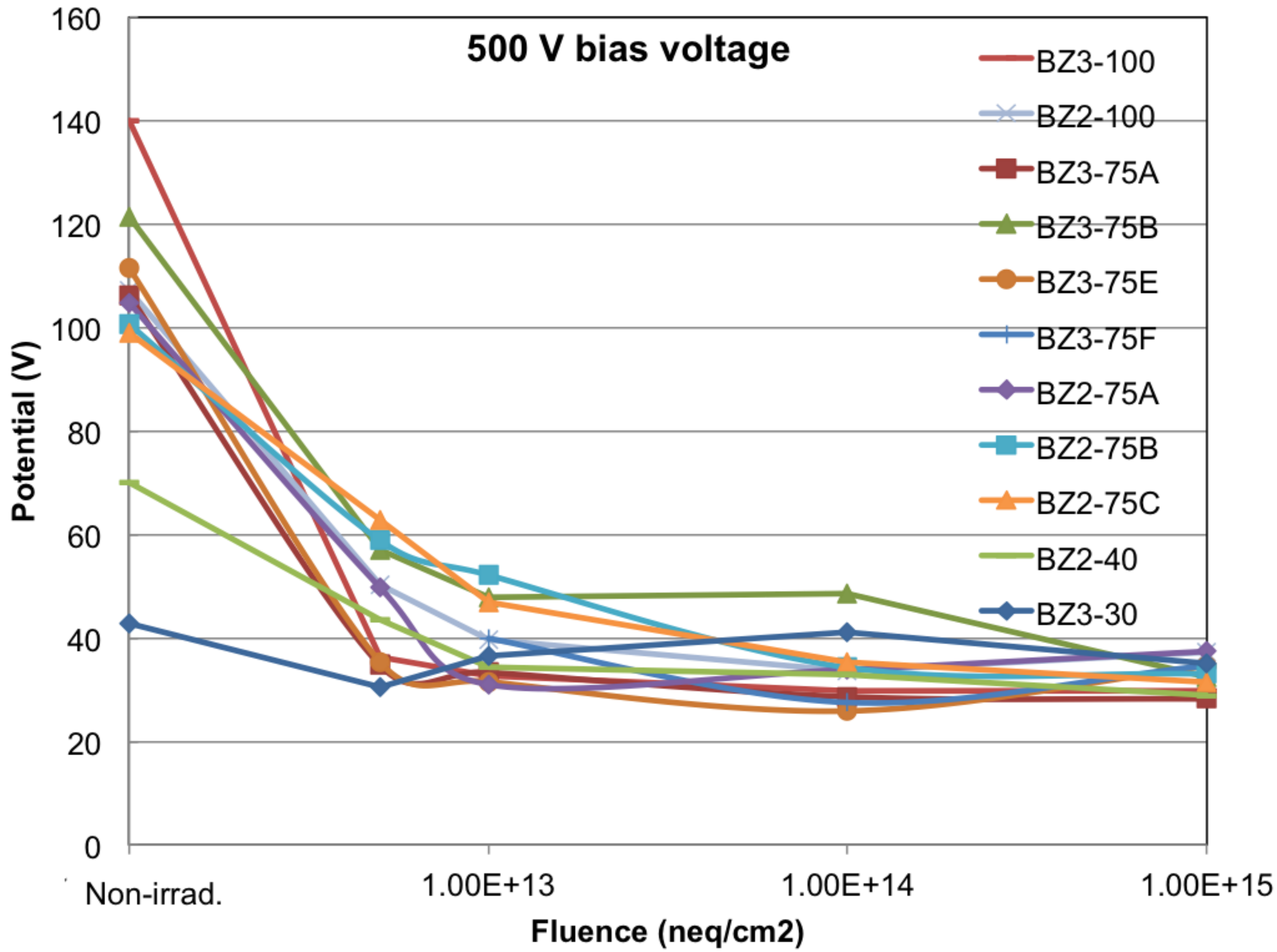


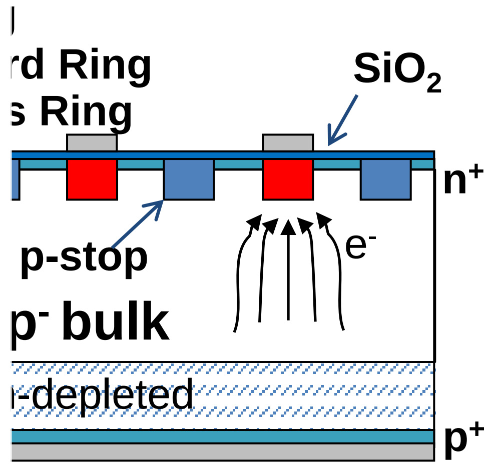
1x10^{14} neq/cm^2
10uA at 2000 V
-15 ° C



- Field width
  - Area with no implantation
- Required field width
  - decreases as fluence increased
- Hot electron images confirm that
  - the highest electric field is
  - in the bias ring (n$^+$ implant)
  - not in the edge ring (p$^+$ implant)

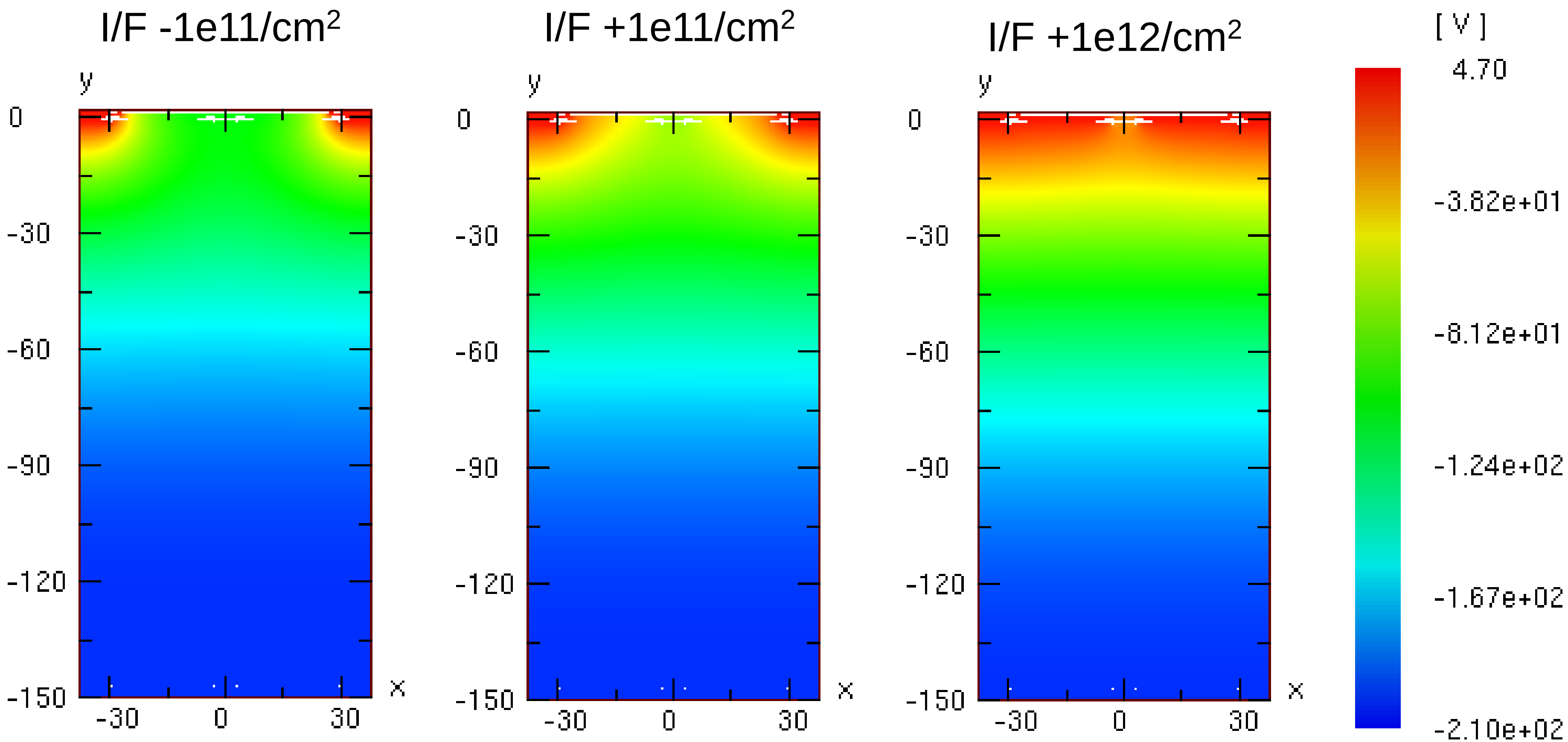
Potential of p-stop





- Wider the pitch, larger the potential
- Potential decreases and saturates as fluence increase

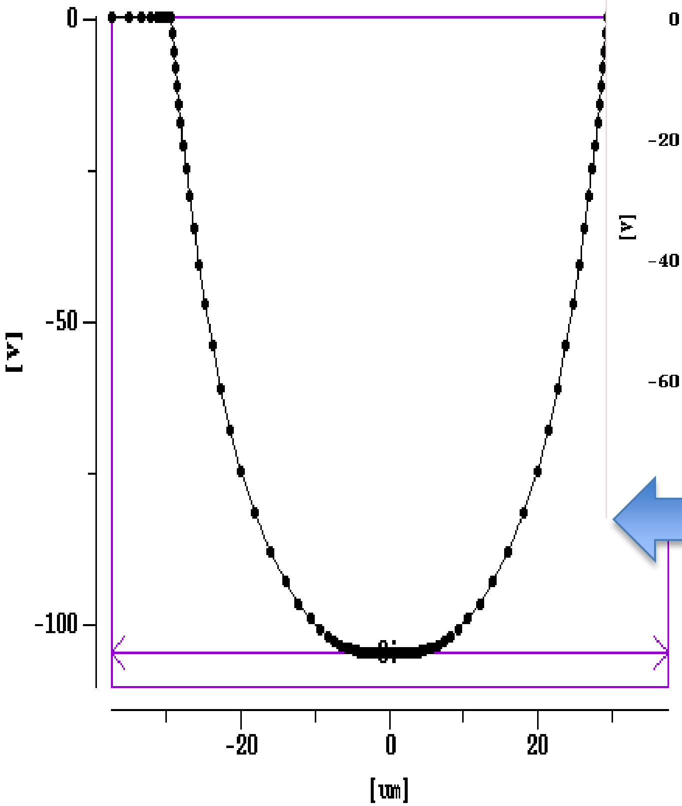
P-stop Potential - TCAD



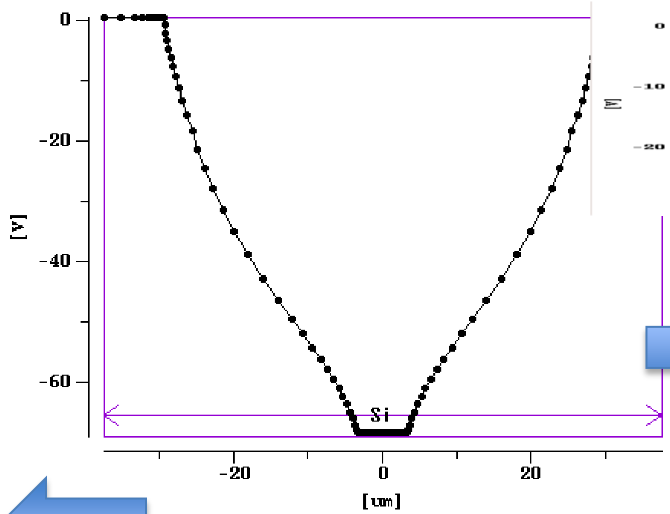
- TCAD model
  - Thickness 150 µm, Bias voltage = 200 V
  - Radiation damage in bulk - Bulk resistivity is reduced by increasing the acceptor states, N_{eff} ~ 1.4 x $10^{12}/cm^3$, full depletion voltage of ~1 kV at 320 µm.

P-stop Potential - TCAD

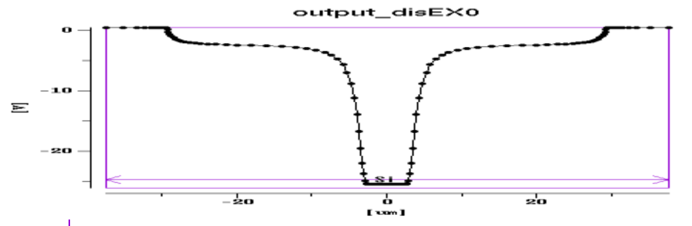
I/F charge -1e11/cm^2



I/F charge +1e11/cm^2



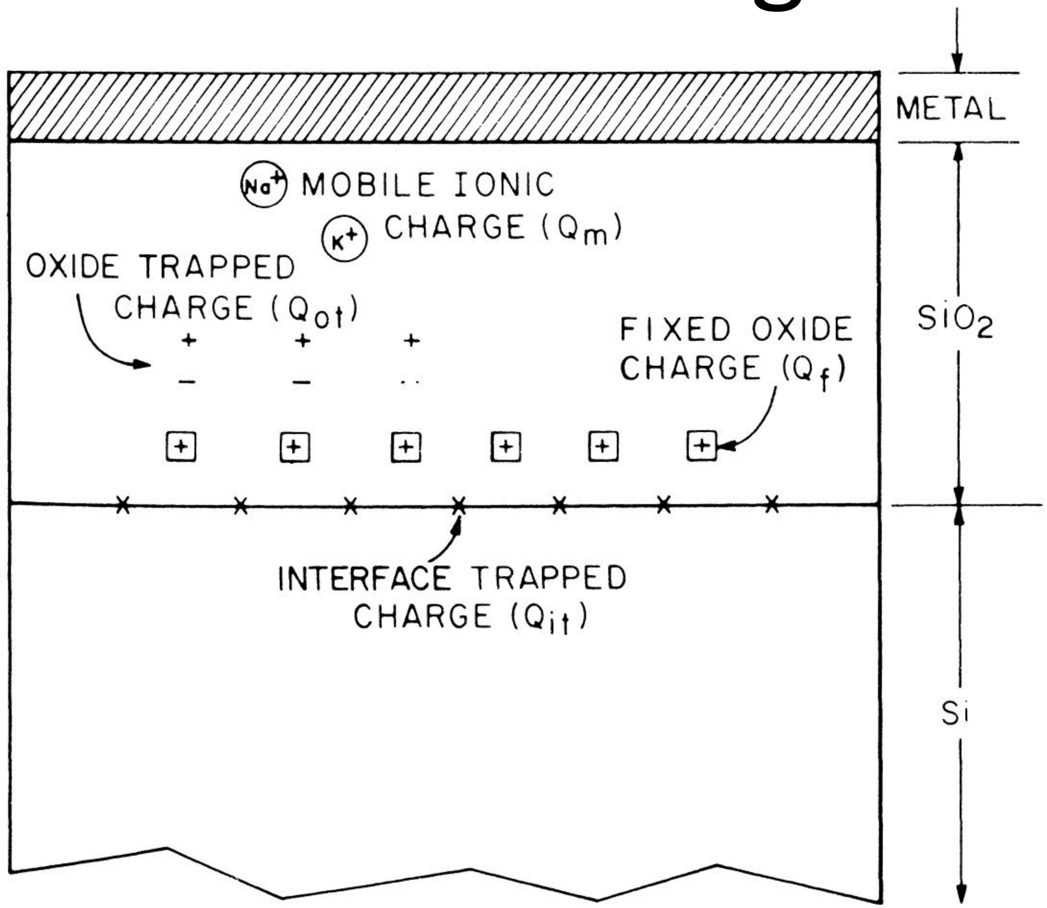
I/F charge +1e12/cm^2



- Positive charge-up
  - explains "decrease of p-stop potential", but
  - does not explain "PTP onset voltage increase" nor the highest field at the bias ring side.

- Negative charge-up
  - does not explain "p-stop potential".
  - explains "PTP onset voltage", hot spots at the bias ring.

Interface charges

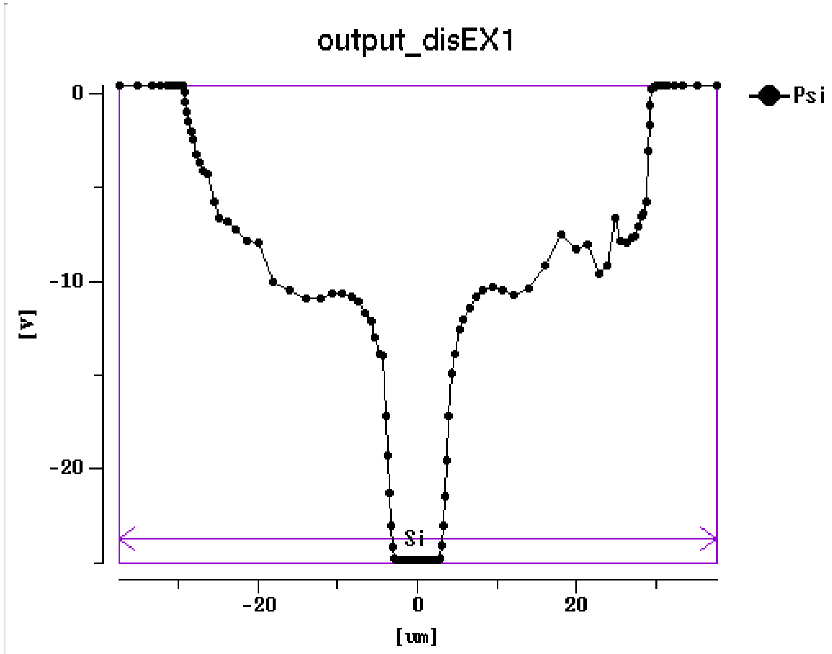


- Fixed oxide charge (Q_t) – known to be "+"
- Interface trapped charge (Q_{it}) – can be "+" or "-"
  - depending on the conditions

Our explanation, backed with TCAD

- After irradiation,
  - Primary factor is the increase of "+" charges, e.g., in the fixed oxide charge
  - The evidences suggest that there is a secondary factor of increase of "-" charges in the "interface trapped charge".
  - This may explain all observations.

- An example of TCAD…



… failed to converge, though.

Summary

- Novel n^+-in-p silicon strip and pixel sensors have been fabricated at HPK successfully.
  - and lead-free bumpbonding as well, which makes one-stop fabrication of pixel detectors from the sensor to the module.
  - Issues especially associated with the n^+-in-p sensors were addressed.
    - Isolation structures that are robust against the bias voltage up to 1000 V.
- We have accumulated a number of evidences on the surface damage, after irradiation, that we explain, backed by TCAD simulation,
  - (1) Primary factor is “+” charge-up of, e.g., Fixed oxide charge, and
  - (2) Secondary factor is “-” charge-up of “interface trapped charge”.

Backup slides

P-stop Potential - TCAD

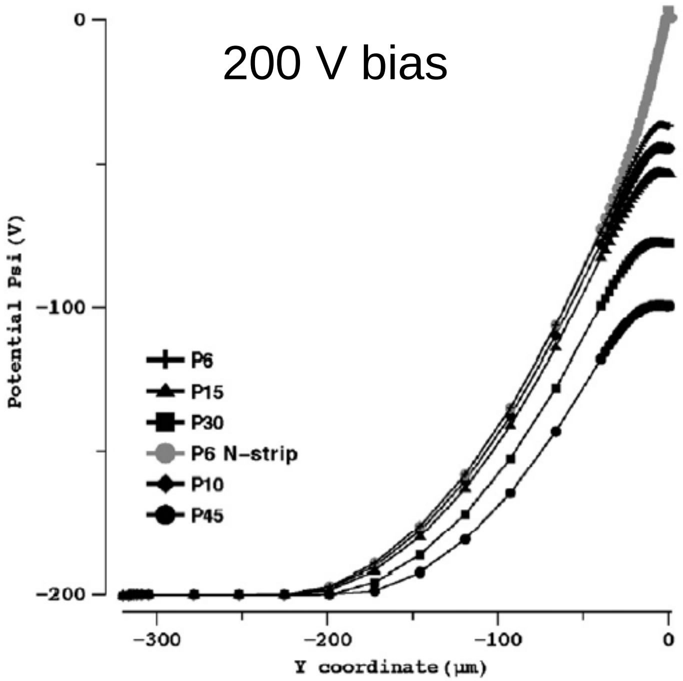


Fig. 7. Electric potential Psi charted vertically through silicon in common p-stop structures with p-stop widths of 6–45 µm at the centre between the n⁺-strips (P6–P45), and at the n⁺-strip (P6 N-strip).

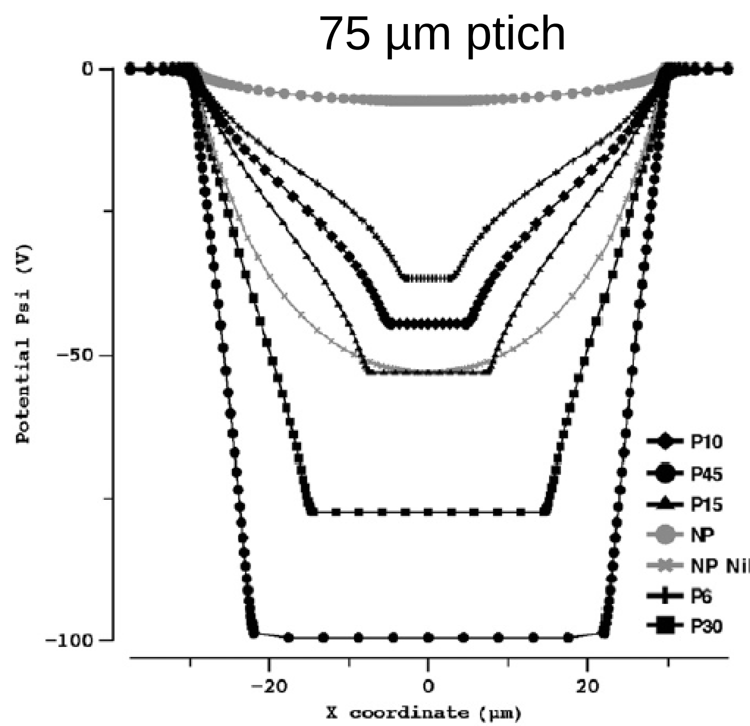


Fig. 6. Electric potential Psi near the silicon surface between n⁺-strips in common p-stop structures with p-stop widths of 6–45 µm (P6–P45), together with references without p-stop and with interface trap charges of 1×10^{11} cm^{-2} (NP) and nil (NP Nil).

- Silicon wafer
  - 320 µm, 3 kΩ cm (=4.7x10^{12} cm^{-3})
- Condition: Non-irradiated
- Ratio of p-stop potential-to-bias voltage seems stable for the change of the bulk resistivity
- Y. Unno et al., Nucl. Instr. Meth. A636 (2011) S118–S124