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Development of Readout System of FE-I4 Pixel Module Using SiTCP

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The pixel detector of the ATLAS will be replaced at the future upgrade of LHC to keep the performance at high luminosity operation. For the upgrade, the sensor modules have been developed by using new front-end chips (FE-I4). Since design of the FE-I4 chip is different from the chip used for the current pixel detector, new DAQ system is necessary to read the sensor modules. For that reason, we have developed DAQ system by using a "SEABAS"DAQ board. SEABAS processes the data from the FE-I4 chips with an FPGA (User-FPGA) and transfers data to a computer via Ether-net with SiTCP. SiTCP is a technology to realize direct access and transfer of the data in the memory of User-FPGA from the PC by utilizing TCP/IP and UDP communication with a dedicated FPGA. We have developed firmware and software for SEABAS, together with readout hardware chain, and established basic functionality for reading out the FE-I4 chips.

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