Test of TRAPPISTe Monolithic Detector System

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September 6, 2012

Section 1

Introduction

Silicon Detectors in Particle Physics

Particle Detector: device used to detect, track and identify subatomic particles. State-of-the-art high energy physics experiments use silicon detectors as innermost high-precision tracking device.

- In depleted silicon material, a MIP generates 24K $e^- h^+$ pairs in 300μm
- $e^- h^+$ pairs separate in E-field and drift to electrodes
- Moving charges $\rightarrow$ electric current pulse
- Small current signal is amplified and processed by read-out electronics

Objective: Drive to develop more precise, thinner and radiation hard detectors.

Monolithic pixel devices: Radiation sensor + charge amplifier + signal processing on single Si wafer.

Section 2

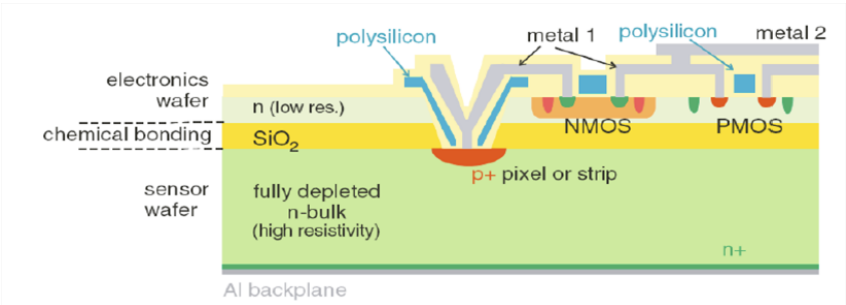
Monolithic Detector Approach: SOI Technology

SOI Technology

Monolithic pixel detector can result in a device with improved spatial resolution and minimized multiple scatterings effects. Different technological options:

- Non-standard CMOS on high resistivity bulk, CMOS technology with charge collection in epi-layer, DEPFET pixel sensors, **CMOS on Silicon-on-Insolator (SOI)**

SOI Wafer: thick high resitivity handle layer, middle SiO_2 layer and a low resistivity top active layer.



- **Detector** $\rightarrow$ handle layer
- **Read-out circuitry** $\rightarrow$ top layer
- Connected by vias

Ensure the proper operation of the readout circuitry while the detector is biased, with the effect of the back gate and radiation effects.

Section 3

TRAPPISTe Project

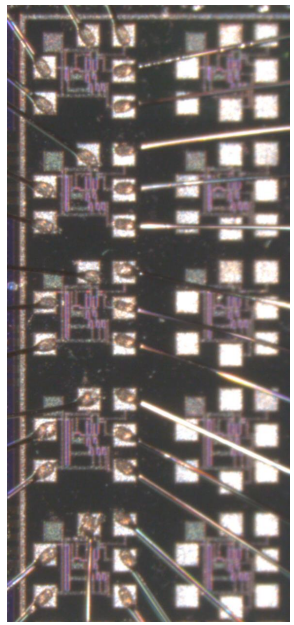
TRAPPISTe Project

Tracking Particles for Physics Instrumentation in SOI Technology

- R&D project with the aim of studying the feasibility of developing a monolithic active pixel sensor with SOI technology.
- Université catholique de Louvain and Universitat Autonoma de Barcelona (2008); part of SOIPIX collaboration (2010).

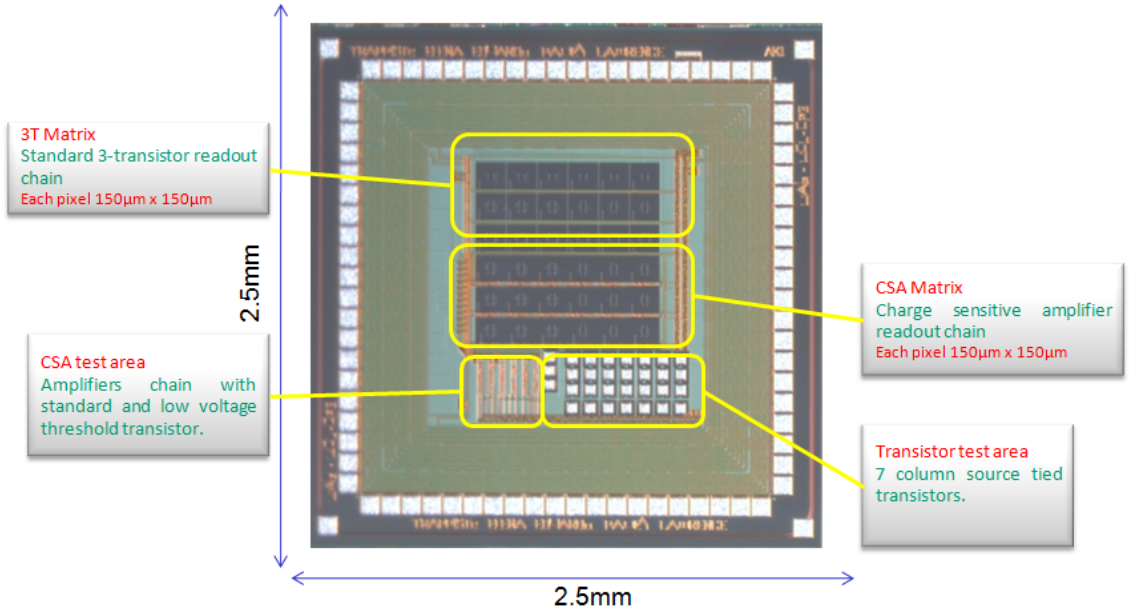
TRAPPISTe-1

- WINFAB at UCL, Louvain-la-Neuve, Belgium
- 2μm FD-SOI CMOS technology
- One metal layer, one poly layer
- 15-25 Ωcm p-type handle layer
- 100 nm top active layer
- 400 nm buried oxide
- $\sim$400 μm handle layer
- Charge sensitive amplifier study.



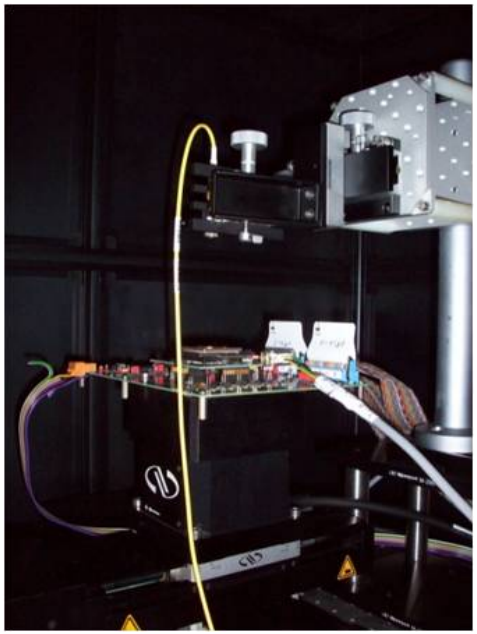
TRAPPISTe-2

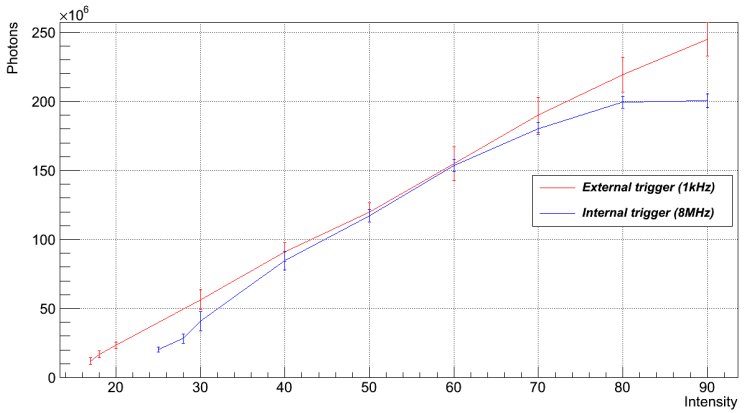
- LAPIS Technology
- 0.20μm FD-SOI CMOS technology
- Five metal layers, one poly layer
- 700 and 10k Ωcm n-type handle layer
- 50 nm top active layer
- 200 nm buried oxide
- $\sim$300 μm handle layer



Different test areas: a transistor test area, a 3T matrix, an amplifier test area and an amplifier matrix.

The TRAPPISTe chips have been characterized using a custom built PCB controlled by an Altera DE2 FPGA. A laser system LARA (Laser for Radiation Analysis) with motorized stage has been commissioned.

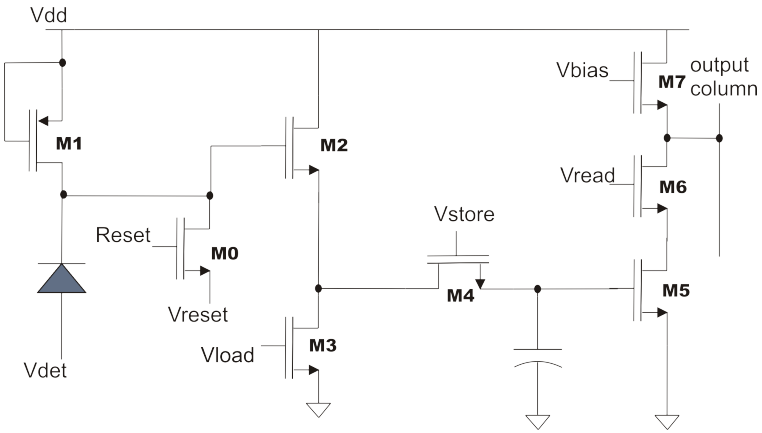




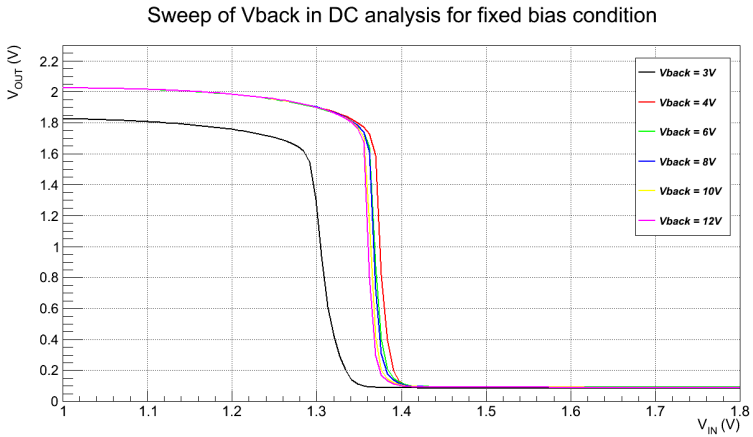
Section 4

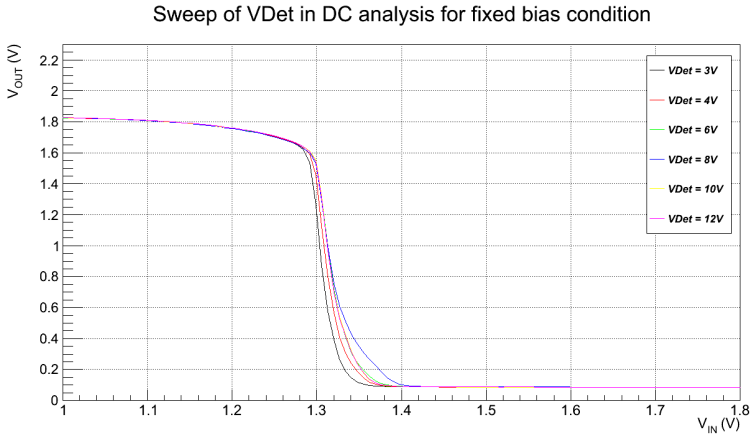
Measurements

TRAPPISTe-2: 3T Electrical Characterization I



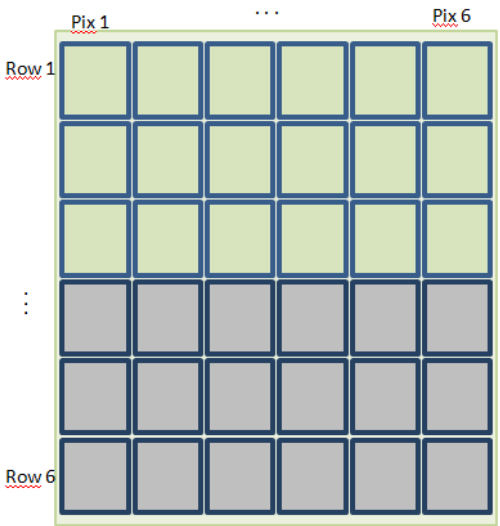
The architecture is based on a simple three transistor structure where an external shift register is responsible for activating each column output.

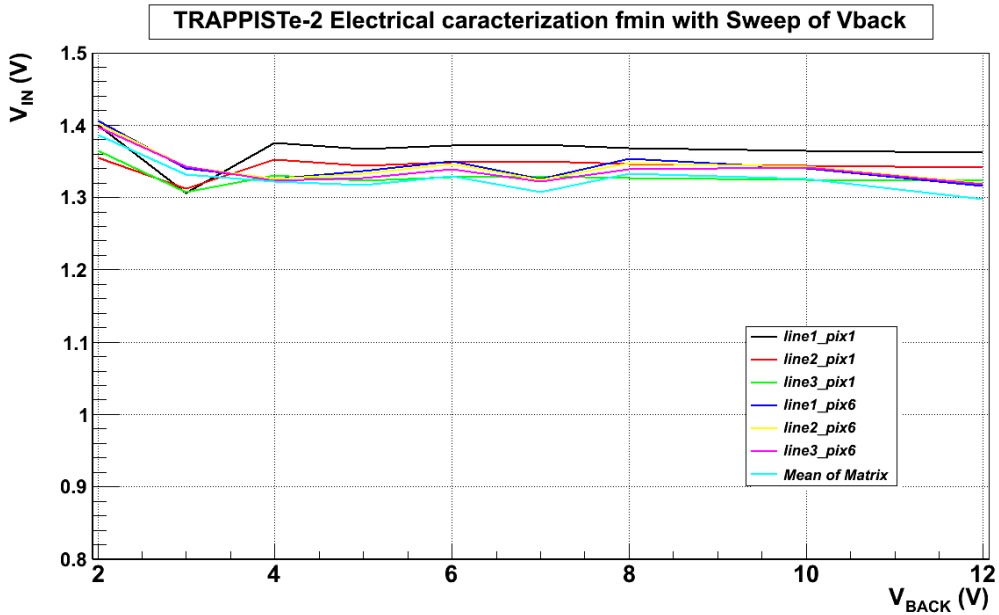


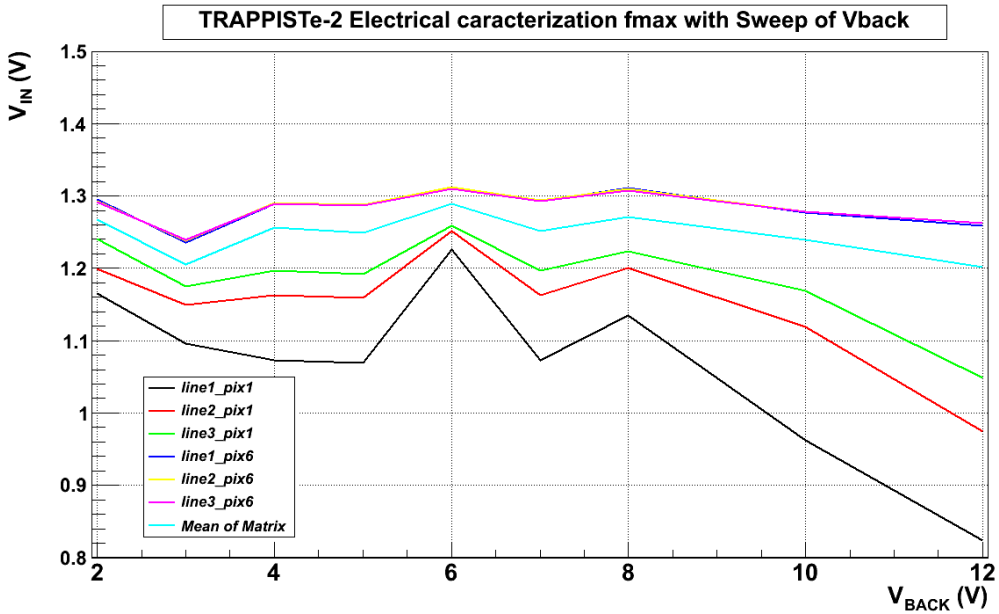


TRAPPISTe-2: 3T Electrical Characterization II

Electrical characterization was performed on pixels with 3T read-out architecture.

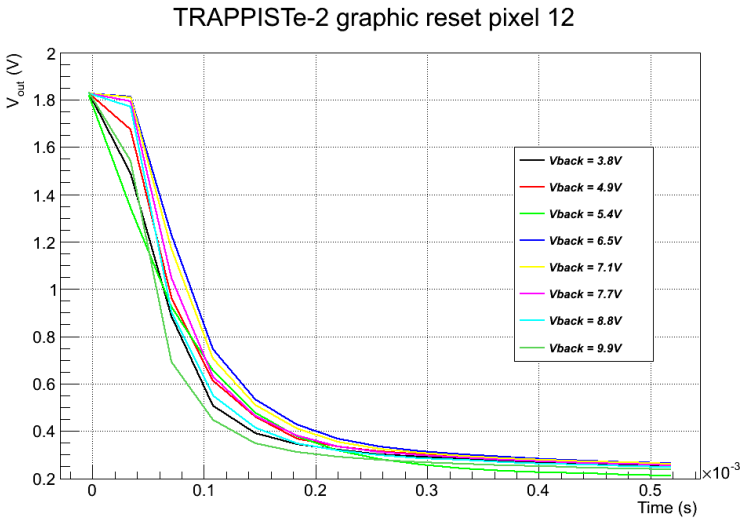


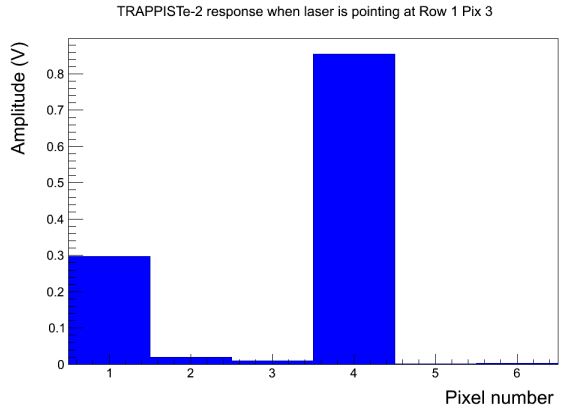


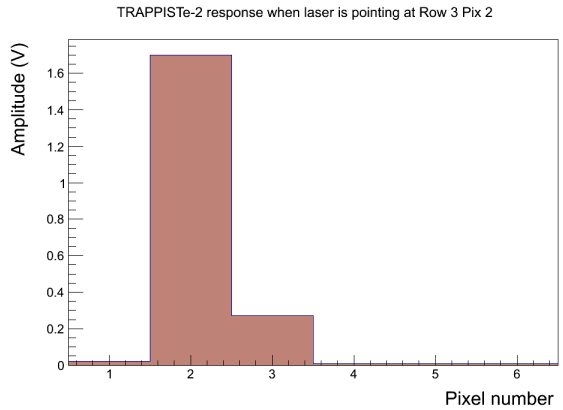


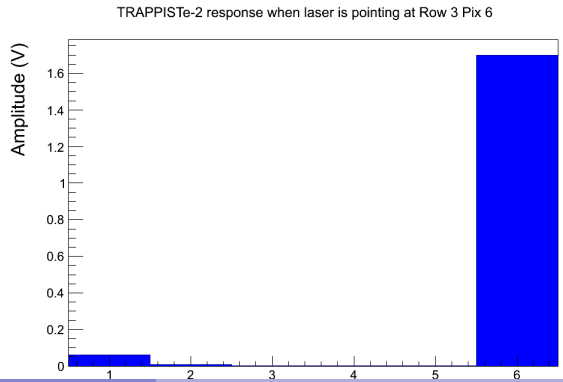
TRAPPISTe-2: 3T Laser Measurements

Laser measurements were performed on pixels with 3T read-out architecture. Six columns of pixels were implemented. Response to laser despite low back depletion voltage. Movement of laser across pixels results in corresponding pixel response.



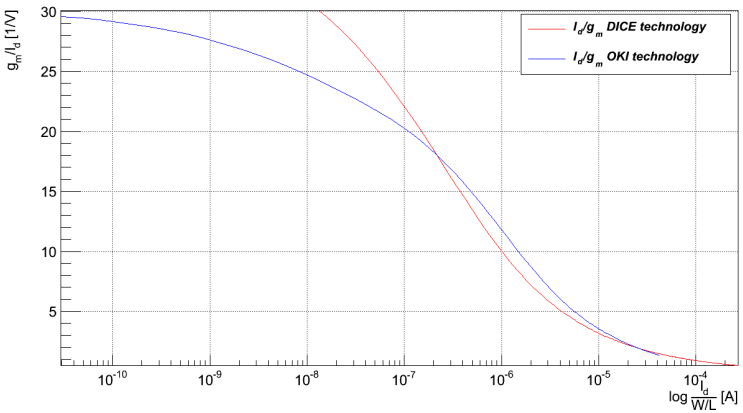




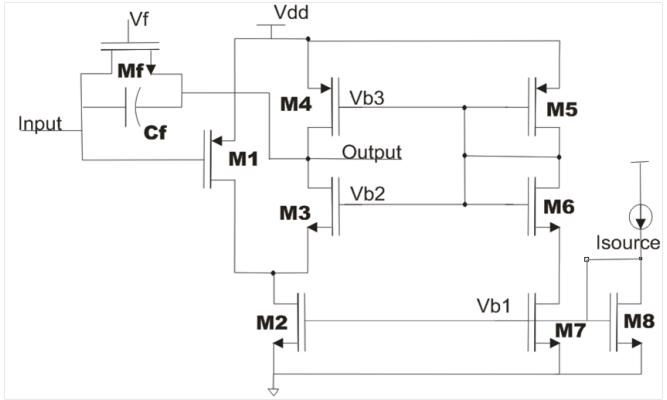


Design of Charge Sensitive Amplifier (CSA) using g_m/I_D

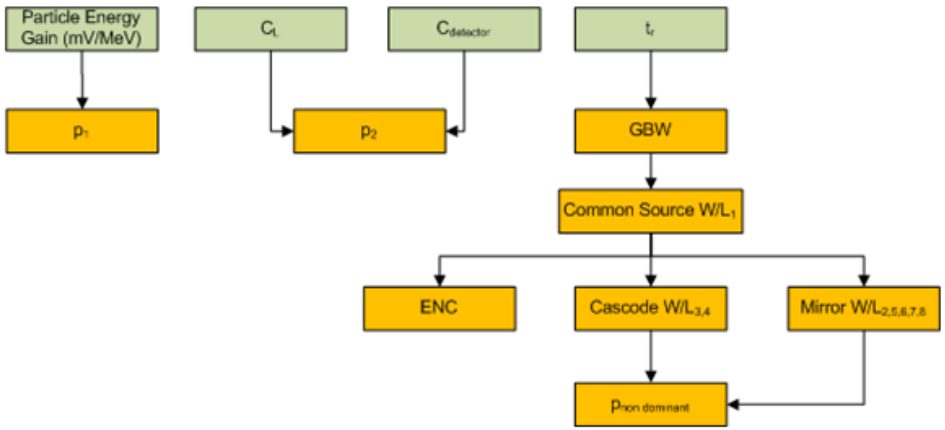
g_m/I_D Transistor Characteristic



Folded Cascode Architecture

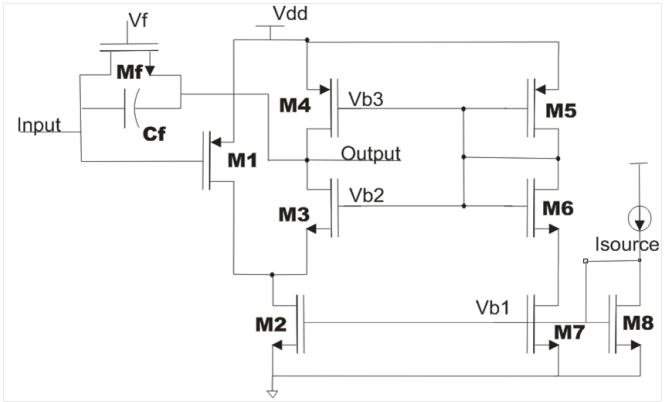


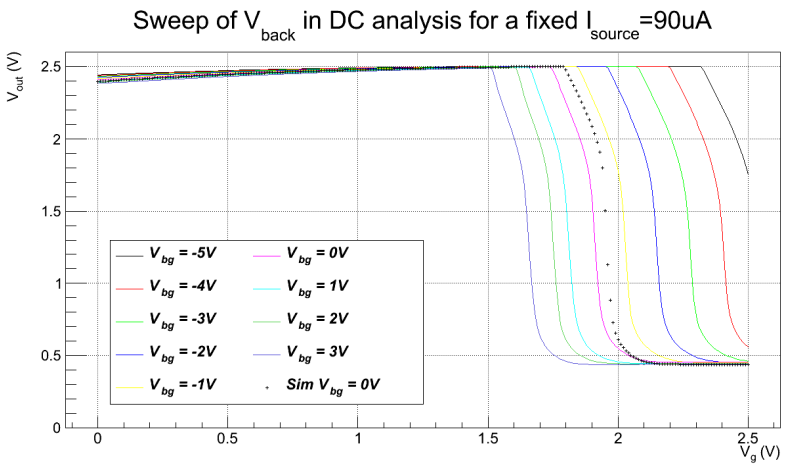
Design methodology to aid in transistor sizing based on amplifier specifications. Same methodology can be used for different techonologies.

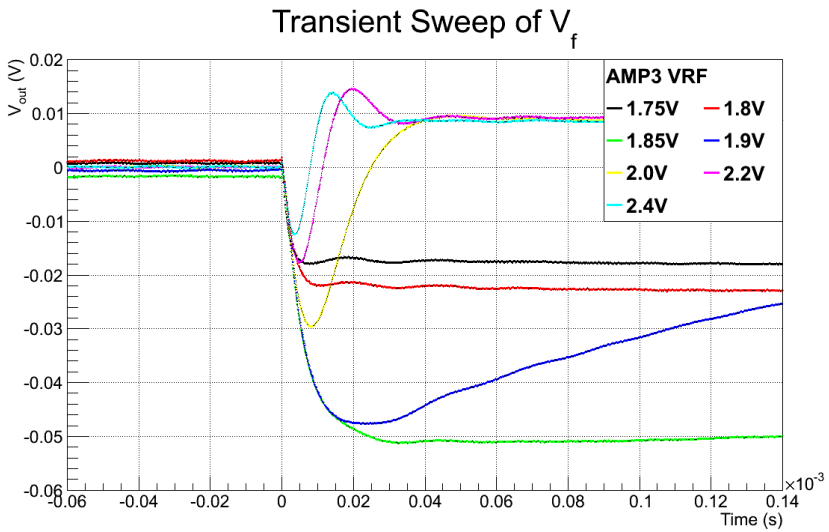


TRAPPISTe-1 Electrical Characterization

CSA test structures in UCL 2.0 μm technology were characterized. DC curves shift with back voltage until -4V. Output shape determined by feedback transistor.

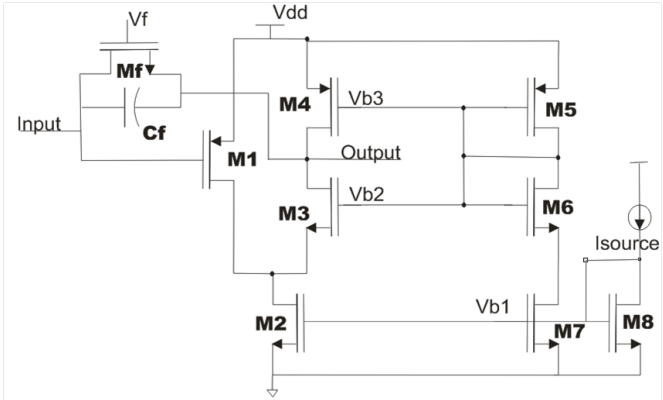


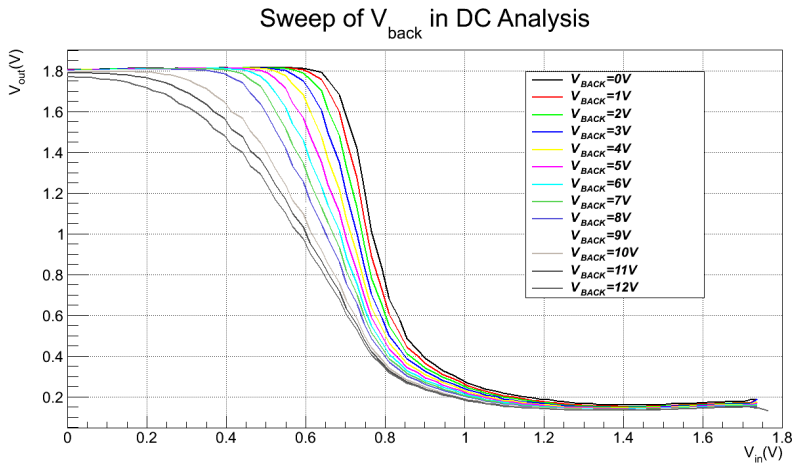


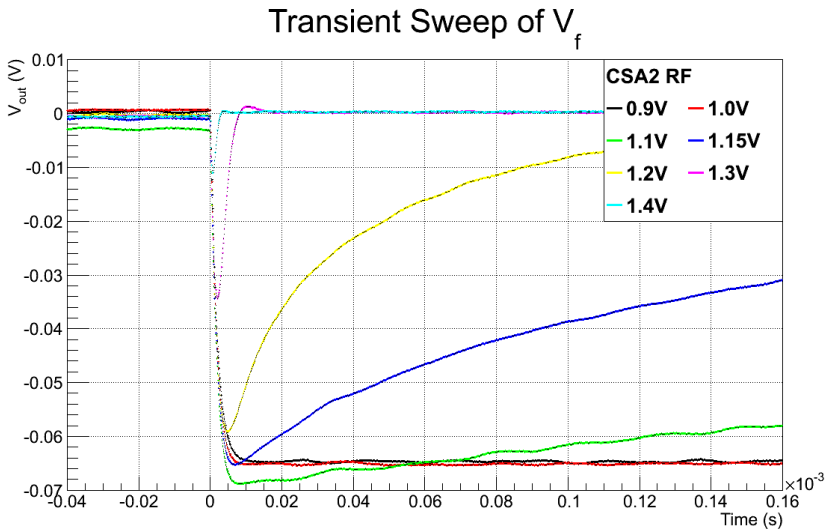


TRAPPISTe-2 Electrical Characterization

Same architecture as previous CSA, built in LAPIS 0.2 μm technology. Test structures show transfer curve shift up to higher V_{back}, more than 12V.





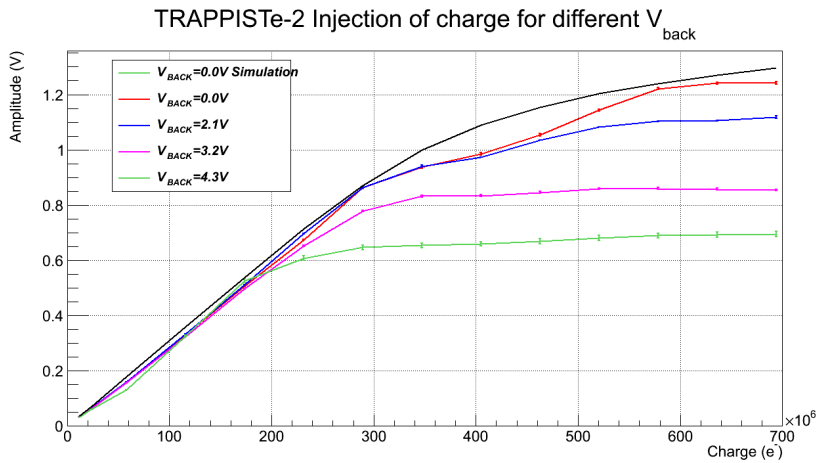


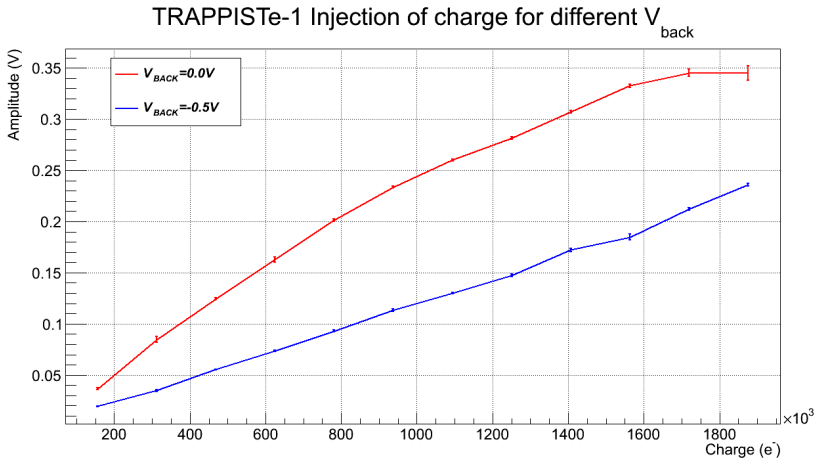
TRAPPISTe-1 and TRAPPISTe-2 charge injection

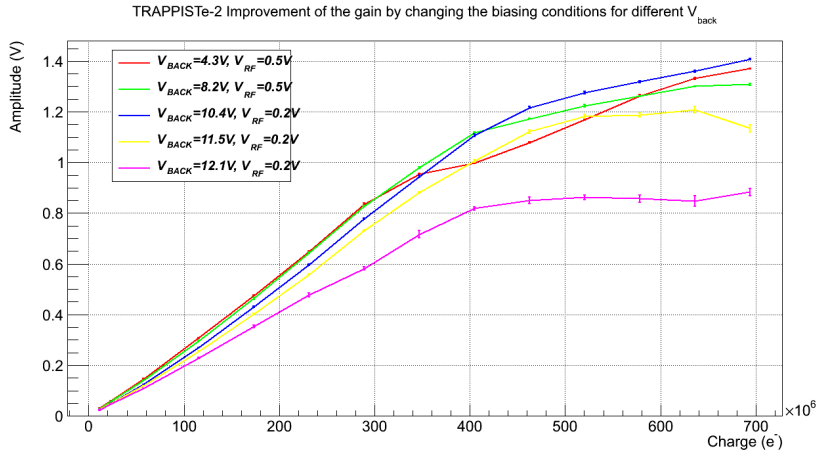
Charge injection curves on test structures with input test capacitor:

- $C_{TRAPPISTe-1}$=0.1pF
- $C_{TRAPPISTe-2}$=37.5fF

Variation of curve for different V_{back}.







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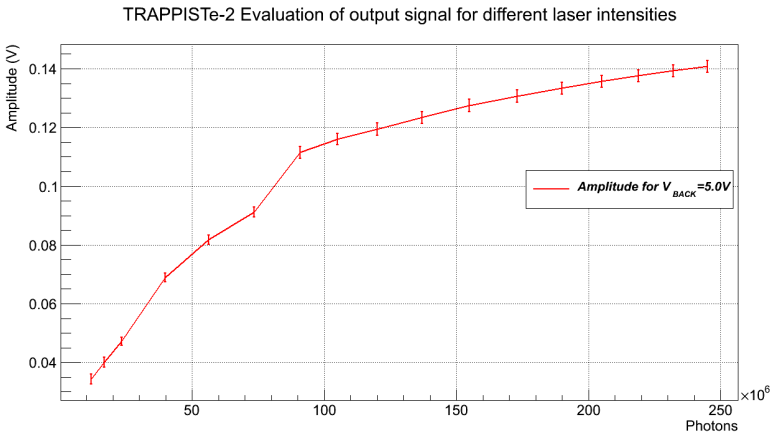

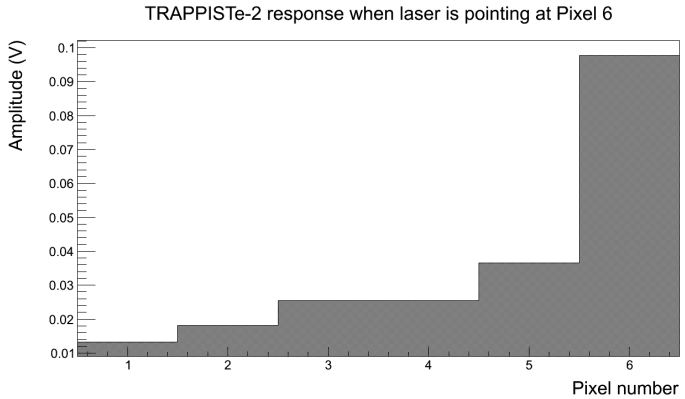

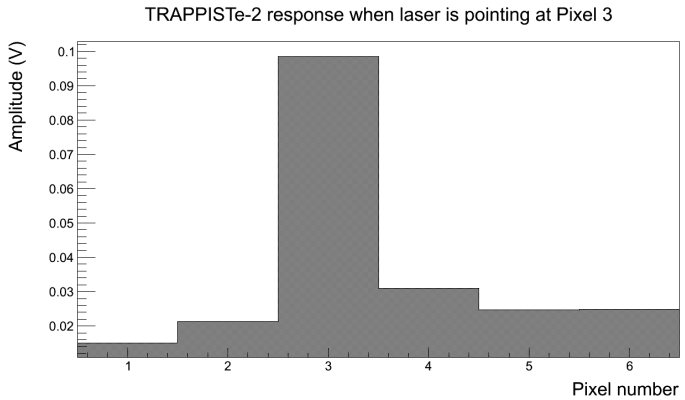

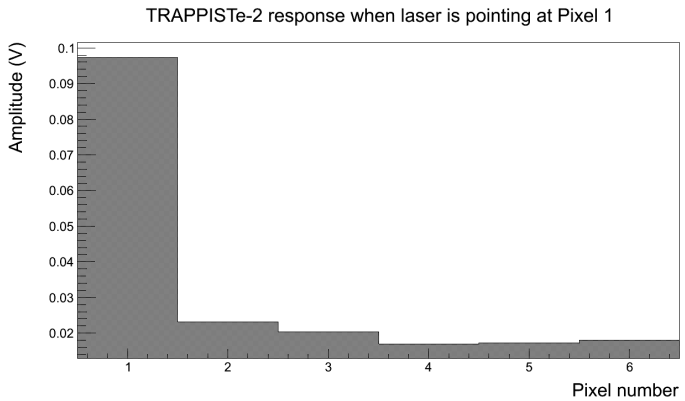

Section 5

Conclusion

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TRAPPISTe: Reasearch and development of monolithic pixel detector in SOI technology.

- TRAPPISTe-1 in WINFAB 2 μm FD-SOI CMOS, TRAPPISTe-2 in LAPIS 0.2 μm FD-SOI CMOS.
- 3T and transistor test structures characterized.
- Charge sensitive amplifier developed with g_m/I_D methodology have been characterized.
- Test structures show variation of perfomance due to back voltage.
- Laser response despite low depletion voltage.
- TRAPPISTe-3 to include process techniques to mitigate the back gate effect, such as the buried P-well and nested well process.

You are welcome to visit the Poster ID 63 **"Development of SOI Monolithic Detector System"** to find out more details about our work.

Thank you for your attention!