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# Test of TRAPPISTe Monolithic Detector System

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The use of different semiconductor technologies in the field of particle detector has been always limited by the effects of radiation in both the sensors and the processing circuitry. This fact has encouraged the teams working in future developments to evaluate the use of different technological approaches to minimize the impact of radiation by using new detector material, connections and read-out architectures.

A monolithic Active Pixel sensor for charged particle tracking has been developed. This sensor is within the frame of an R&D project called TRAPPISTe (Tracking Particles for Physics Instrumentation in SOI Technology), with the aim of studying the feasibility of developing a Monolithic Active Pixel Sensor (MAPS) with Silicon-on-Insulator (SOI) technology. Two different architectures are being evaluated, 3-transistor (3T) and charge sensitive amplifier (CSA). To compare the results, two chips have been fabricated: TRAPPISTe-1 and TRAPPISTe-2. The first prototype TRAPPISTe-1 was produced at the WINFAB facility at the Universite catholique de Louvain (UCL) in Belgium in a 2µm fully depleted (FD-SOI) CMOS process. TRAPPISTe-2 is the second prototype in this series and was fabricated with the OKI 0.20µm FD-SOI CMOS process. Each one of the prototypes analyzed implements two different approaches, 3-transistor read-out and charge sensitive amplifier.

The TRAPPISTe-1 prototype is an 8x8 pixel matrix with a shift register used to control signal readout. Each pixel contains simple 3-transistor readout and has dimensions 300µm x 300µm. An additional layout of charge sensitive amplifiers was implemented separately in order to validate the architecture in SOI, although no connection with the detector was included. The second phase of this project was developed with the TRAPPISTe-2 prototype. This version included similar readout architectures for evaluation and several test transistors, although the size of the pixel cells is 150µm x 150µm.

The TRAPPISTe chips have been measured using a custom built PCB to provide the necessary bias and control signals. The test system is controlled by an Altera DE2 FPGA and data is collected on a PC via an Ethernet connection.

The charge sensitive amplifiers were implemented in both WINFAB and OKI technologies. The amplifiers were based on a standard folded cascade core with a feedback capacitor. DC measurements of the amplifiers agree with simulations and the effect of varying the back voltage can be clearly observed. Different effects have been measured, such as the influence of the bias current and the effect of varying the feedback transistor gate voltage. Transient output measurements were performed by injecting a voltage pulse onto a test input capacitor and changing the amplifier bias currents and voltages. The 3-transistor read-out architecture was also implemented in both WINFAB and OKI technologies. The architecture is based on a simple structure where an external shift register is responsible for transferring the charge information. This structure has been used to characterize the whole matrix electrically.

A laser system named LARA (Laser for Radiation Analysis) has been developed to characterize silicon sensors. LARA contains a remote controlled 3-axis motorized stage that can position a test device under a laser beam. An infrared laser at 1060nm wavelength and a red laser at 670nm wavelength are available. The system is controlled by a PC via a LabVIEW interface. The laser measurements are being tested on both the 3T and the CSA architectures.

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