The electronic readout for the TRAPPISTe series of monolithic pixel detectors has been characterized. Developed in SOI technology, the behavior of the electronics due to the back voltage has been studied to determine the feasibility of implementing a monolithic particle detector.

Specifications:
- Particle Energy = 1MIP (24keV), Gain = 20mV/MIP, CF = 0.2pF, Cdetector = 5pF, tr = 100ns
- All of the transistors have a W/L of 10µm/2µm except for the I/O n-type Depleted MOS (DMOS) transistors which are size 2µm/10µm.

Use of 2 methods (Linear-extrapolation and minimum of 2nd derivative) at 2 different biasing conditions (Vd = 20mV and 50mV) to obtain Vth where:

\[ F_2(V_{th}) = \frac{dI}{dV} = \frac{I}{V^2 - V_{th}} \]

where:

\[ V_{th} = \frac{I_{DS}}{g_m} + \frac{V_{th0}}{g_m} \]

Threshold Voltages

Method of 2nd derivative

Charge Sensitive Amplifier

Charge amplifiers were developed in DICE and LAPIS technologies using a gm/Id methodology. Testing was performed on test structures with particular attention to the effect of varying the back side voltage as these amplifiers are to be used in the TRAPPISTe monolithic pixel detector. The charge injection curves exhibit degradation due to increasing back voltage. Variation of circuit parameters can recover charge curve functionality up to a certain point.

Future development of the amplifier would involve techniques to mitigate the back gate effect, such as buried p-well process technology foreseen for TRAPPISTe-3.

TRAPPISTe-1

Comparison of gm/Id curves for DICE and LAPIS Technology

TRAPPISTe-2

DC response at different Vback

Conclusions

- Future development of the amplifier would involve techniques to mitigate the back gate effect, such as buried p-well process technology foreseen for TRAPPISTe-3.