Development of SOI Monolithic Detector System

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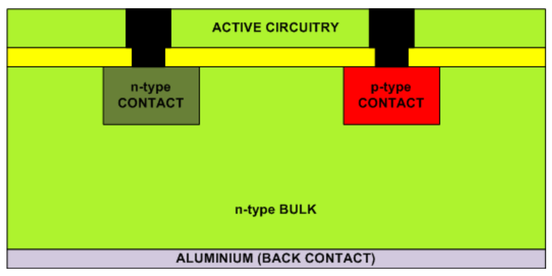
Abstract

The electronic readout for the TRAPPISTe series of monolithic pixel detectors has been characterized. Developed in SOI technology, the behavior of the electronics due to the back voltage has been studied to determine the feasibility of implementing a monolithic particle detector.

Silicon-on-Insulator CMOS technology

Silicon-on-Insulator CMOS technology can be used to develop monolithic radiation detectors.

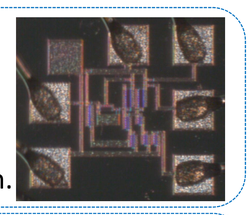


Challenge: Its use is subject to the back gate effect because of the voltage applied to deplete the detector.

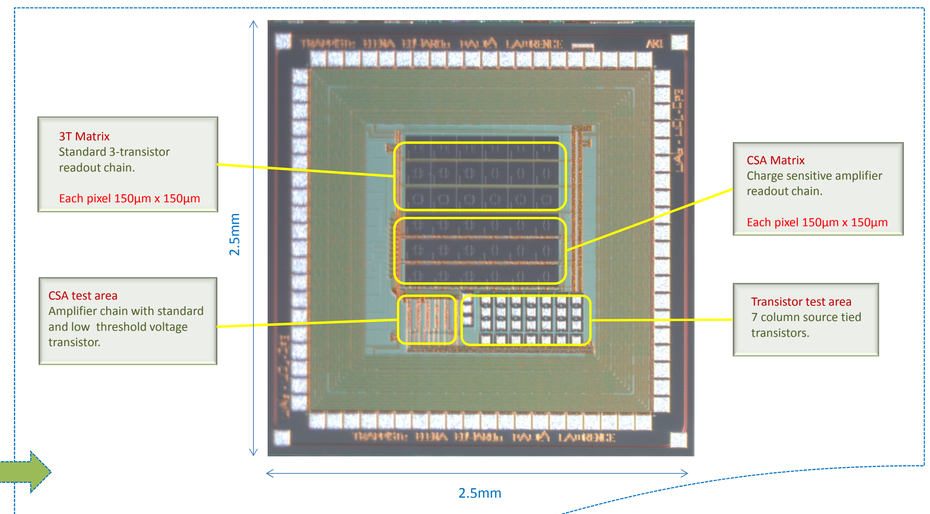
Solution: Among others, increasing the oxide thickness and including different well implantations below the read-out circuitry.

TRAPPISTe (Tracking Particles for Physics Instrumentation in SOI Technology) project aims to analyze and study how to minimize effects in SOI technology. To minimize them, different technologies and read-out approaches are evaluated.

TRAPPISTe-1
was fabricated using WINFAB 2µm FD-SOI CMOS technology.
It provides one metal layer, and a p-type wafer with a resistivity ~25Ωcm.



TRAPPISTe-2
was fabricated with LAPIS Semiconductors 0.20µm FD-SOI CMOS technology.
It provides five metal layers and high resistivity n-type substrates of 700Ωcm and 10kΩcm.



Characterization of the TRAPPISTe-2 transistor

All of the transistors have a W/L of 10µm/2µm except for the I/O n-type Depleted MOS (DMOS) transistors which are size 2µm/10µm.

Use of 2 methods (Linear-extrapolation and minimum of 2nd derivative) at 2 different biasing conditions (Vd=20mV and 50mV) to obtain V_{th}

$$F_1(V_G) = \frac{dI_D/V_G}{I_D^2} = \frac{I_D}{g_m} = \sqrt{A}\cdot(V_G - V_{TH})$$

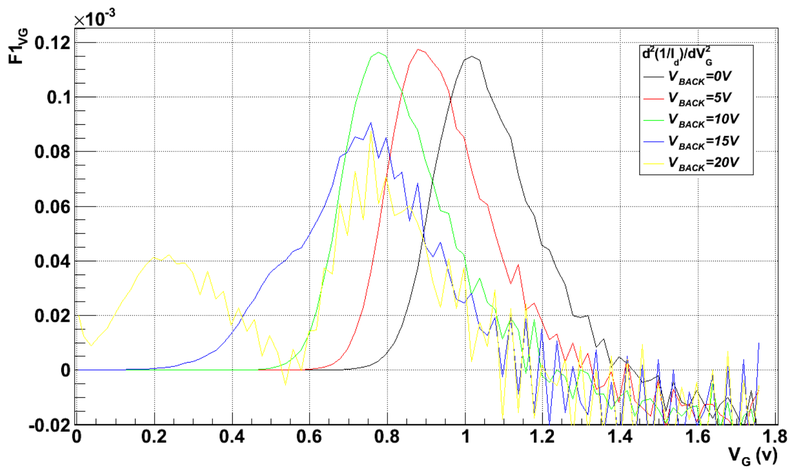
where:

$$A = \mu_0 C_{ox} \frac{W}{L} V_D$$

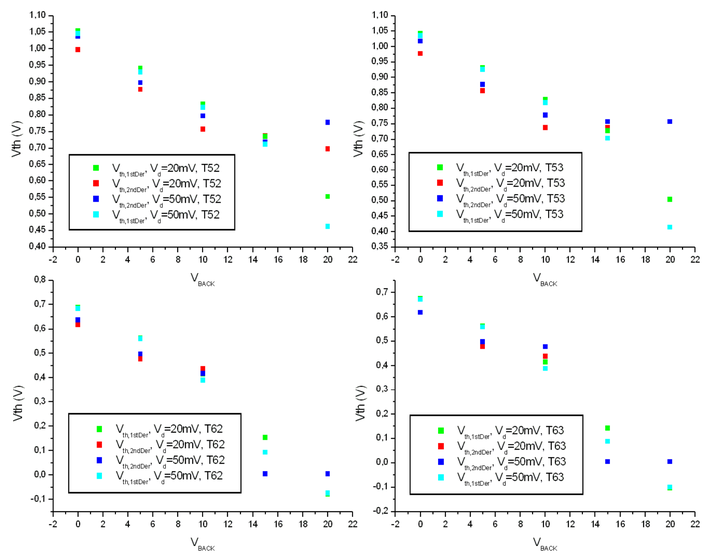
Transistor Type	Characteristics	Comment
NMOS (52)	Vth, normal	PWELL
NMOS (53)	Vth, normal	NO PWELL
NMOS (62)	Vth, low	PWELL
NMOS (63)	Vth, low	NO PWELL

❖ Method of 2nd derivative

✓ 2nd derivative for NMOS with normal threshold voltage, no PWELL.



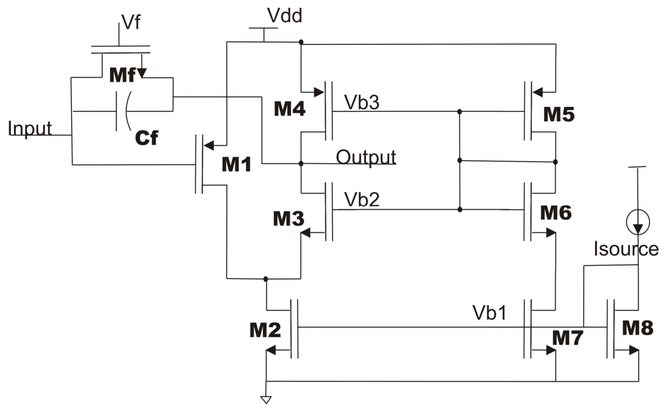
❖ Threshold Voltages



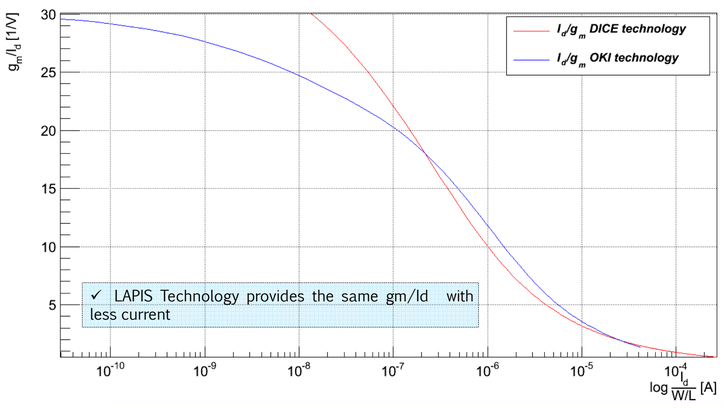
Charge Sensitive Amplifier

❖ gm/Id Design Methodology and Test

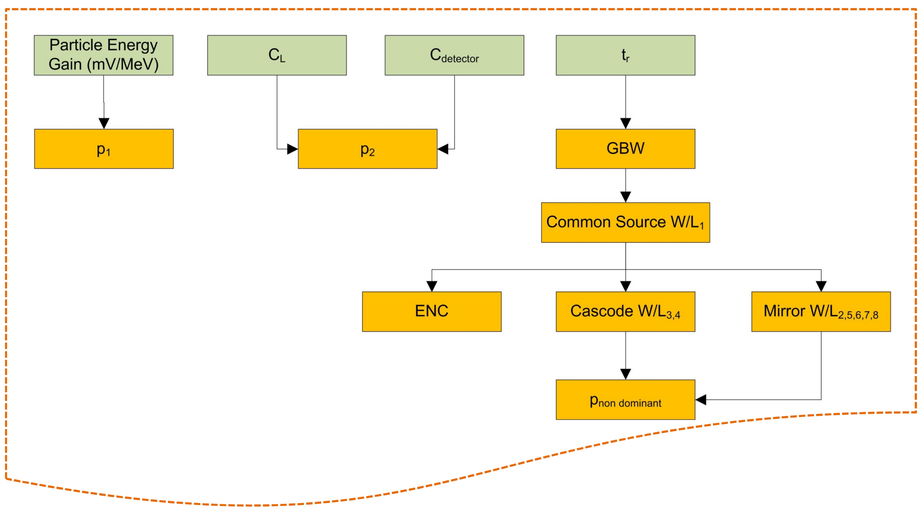
Standard folded cascode core with feedback



Comparison of gm/Id curves for DICE and LAPIS Technology

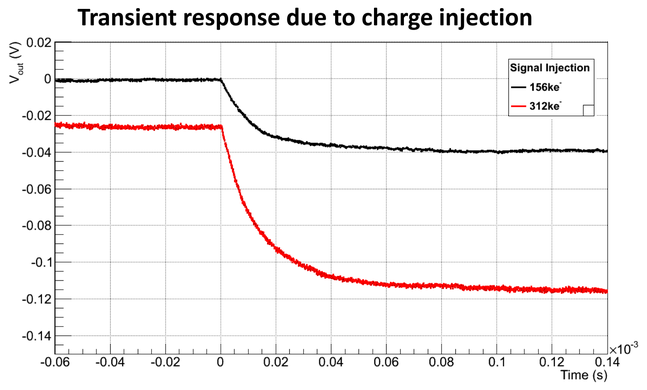


Specifications:
Particle Energy= 1MIP (24ke-), Gain=20mV/MIP, CF=0.2pF, Cdetector=5pF, tr=100ns

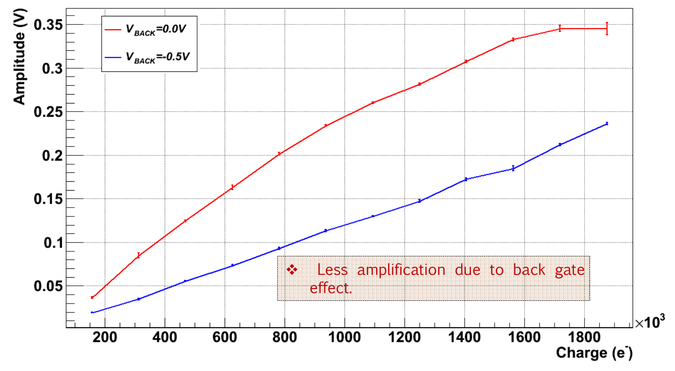


❖ TRAPPISTe-1

Transient response due to charge injection

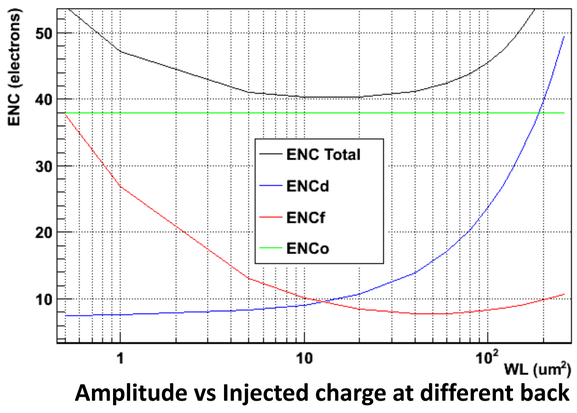


Amplitude vs injected charge at different Vback

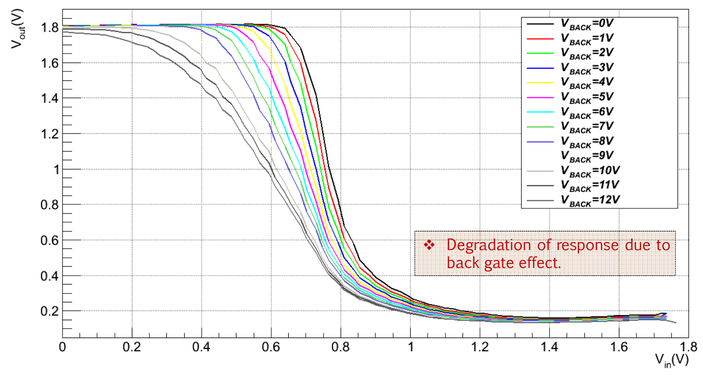


❖ TRAPPISTe-2

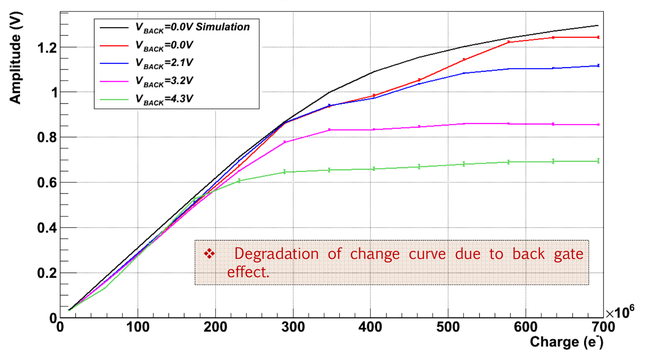
Calculated ENC Curve



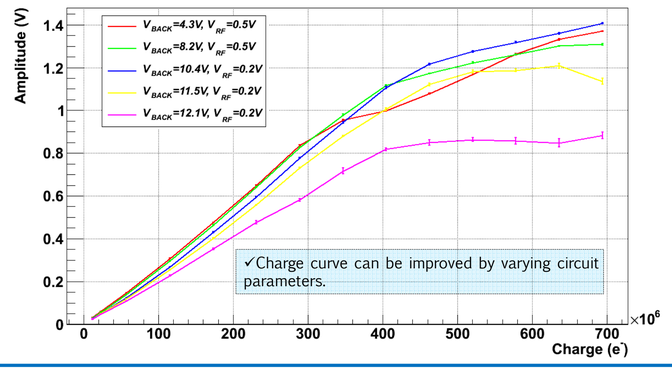
DC response at different Vback



Amplitude vs Injected charge at different back voltages, Vrf=0.9V



Improved Injected charge at different back voltages



Conclusions

- Charge amplifiers were developed in DICE and LAPIS technologies using a gm/Id methodology. Testing was performed on test structures with particular attention to the effect of varying the back side voltage as these amplifiers are to be used in the TRAPPISTe monolithic pixel detector. The charge injection curves exhibit degradation due to increasing back voltage. Variation of circuit parameters can recover charge curve functionality up to a certain point.
- Future development of the amplifier would involve techniques to mitigate the back gate effect, such as buried p-well process technology foreseen for TRAPPISTe-3.