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Characterization of SOI Monolithic Detector System

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The use of different semiconductor technologies in the field of particle detector has been always limited by the effects of radiation in both the sensors and the processing circuitry. Large numbers of research teams are evaluating the use of different technological approaches to minimize the impact of radiation in new developments by using new detector material, connections and read-out architectures. Although most pixel detectors that are in operation are hybrid active pixel sensors, they present clear limitations for particle physics applications. These problems have led to increased efforts related to monolithic solutions, where the sensor, amplification and logic circuitry are found in the same Si-wafer. One of the possible technology solutions is SOI technology, which is the one that has been studied in this project.

Silicon-on-Insulator CMOS technology has been widely used for high gain and low power consumption circuitry, but now, some research groups are studying its use for developing monolithic radiation detectors. This is done by producing an opening and implantation below the thin oxide that connects the top active circuitry and the handle wafer. The use of this technology for particle radiation detectors is subject to the back gate effect because of the voltage applied to deplete the detector. Since the area under the transistor acts as a back gate, its potential affects the threshold voltage and the leakage current of the transistor. The back gate effect depends on many factors, such as the thickness of the bulk substrate, the voltage applied for detection and the guard ring patterns that can be introduced below the oxide to improve signal acquisition. To minimize this effect, different approaches can be made, from increasing the oxide thickness to include different well implantations below the read-out circuitry. One of the main goals of the TRAPPISTe (Tracking Particles for Physics Instrumentation in SOI Technology) project is to analyze these effects and study how to minimize them. In this study/project, two different technologies are used and different read-out approaches are evaluated. Initially a first prototype (TRAPPISTe-1) was developed at the Université catholique de Louvain (UCL) in Belgium at the WINFAB facility in Louvain-la-Neuve. WINFAB provided a 2μm FD-SOI CMOS process with one metal layer. For this prototype, a p-type wafer with a resistivity about 25Ωcm was used. A second prototype, Trappiste-2, was fabricated with a 0.20μm FD-SOI CMOS technology, provided by OKI Semiconductors through the SOIPIX collaboration. The OKI process provides five metal layers and high resistivity n-type substrates of 700Ωcm and 10kΩcm. Both prototypes have been used to study the problem of back gate effect. The interest of using WINFAB technology is because it provides a thicker oxide layer. The second technology, the OKI technology, provides a method to mitigate the back gate effect with a buried P-well (BPW). The first results that will be presented are based on measurements of the test structures performed at different back voltages.

The first steps were used to validate our methodology and tried to characterize the transistors used at different Back Gate. The transistor test area contains single transistors whose gate, source and drain inputs are connected to test pads. It contains seven columns of transistors representing the source tied transistors provided by the OKI process. All of the transistors have a W/L of 10μ/2μ except for the I/O n-type Depleted MOS (DMOS) transistors which are size 2μ/10μ. The parameters such as threshold voltage (VTH), mobility (μ0) and transconductance (gm) have been characterized. The method used to characterize the transistors is based on the linear-extrapolation technique in which VTH is obtained by the linear extrapolation of the I_D√(g_m). Another additional method, based on the calculation derivate is used, to validate the results obtained. These measurements have been performed at different back voltages (to deplete the sensor). The extraction of parameters is an important part of the device modeling and characterization process. Parameter calculations at two drain voltage conditions are used, 20mV and 50mV. The four calculations obtained agree with the values given by the technology.

The charge sensitive amplifiers were the first circuits tested. They were implemented in both WINFAB and OKI technologies. The amplifiers were based on a standard folded cascade core with a feedback capacitor. To aid in the circuit design and dimensioning of the transistors, a gm/Id methodology was used. This methodology provides a rapid process-independent method of dimensioning transistors. Detector and amplifier specifications are used as inputs to a dimensioning plan to determine transistor sizes. The result is then simulated in ELDO to verify the functioning of the circuit. Measurement results will be presented and discussed, as the results agree with the simulations performed.

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