Toward one Giga frames per second
- Evolution of In-Situ Storage Image Sensors -

PIXEL2012
"6th International Workshop on Semiconductor Pixel Detectors
for Particles and Imaging"
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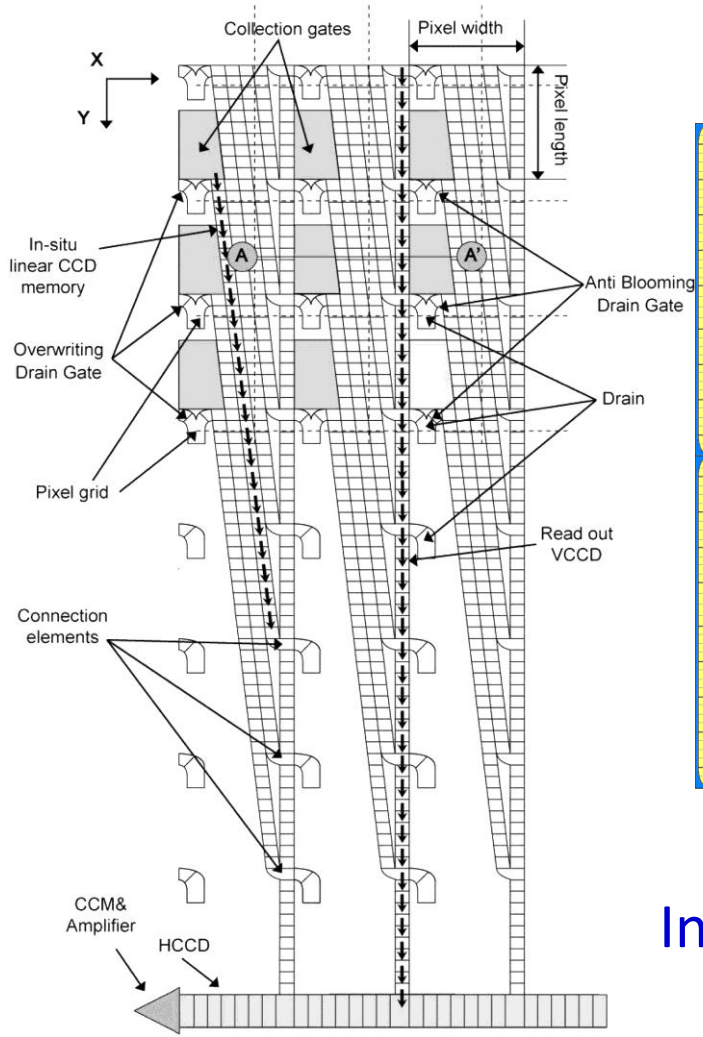
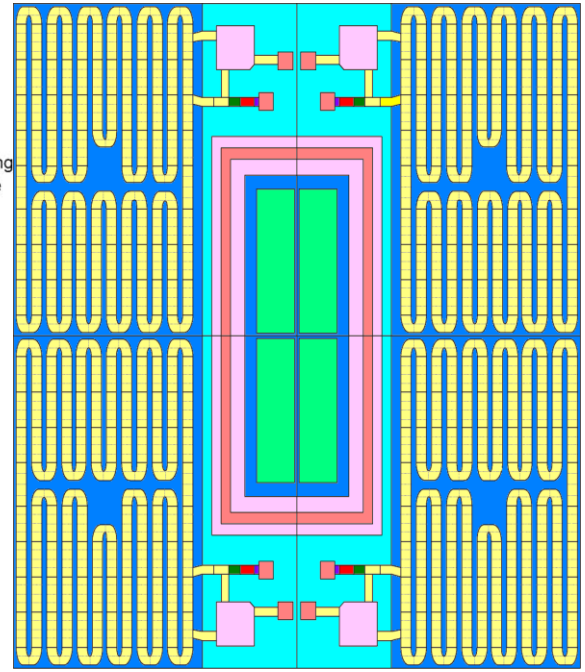
(*Speaker)

OUTLINE

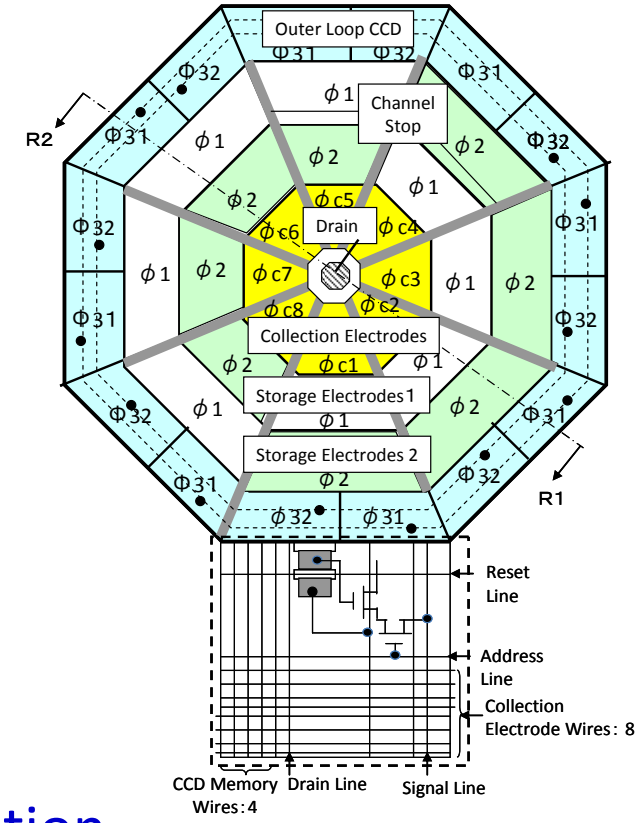
1. Review of Ultra High Speed Image Sensors Using In-Situ CCD Memory
   - Advanced BSI Technologies
   - Example of High Speed Imaging
2. New Pixel Architecture toward 1G-fps
   - Design Concept
   - Pattern Layout and Driving Sequence
3. Consideration for Possibility of 1Gfps Imaging
   - Frame Rate Limitation
   - Simulation Results
4. Summary



All-pixel parallel record
by linear slanted CCDs
achieved 16Mfps



In-pixel signal accumulation
by coiled loop CCDs
being designed



In-pixel multi-collection gates
proposed
Target: 1Gfps

In-situ CCD Storage Family

Necessity of Tetra-stratified BSI

1Mfps ISIS with FSI (Front Side Illumination) at 2001

ISIS: In-situ storage image sensor

↓

Large light shield on CCD memories → Low fill factor of 15%

↓ High sensitivity

BSI → Fill factor nearly 100% → 16Mfps at 2011

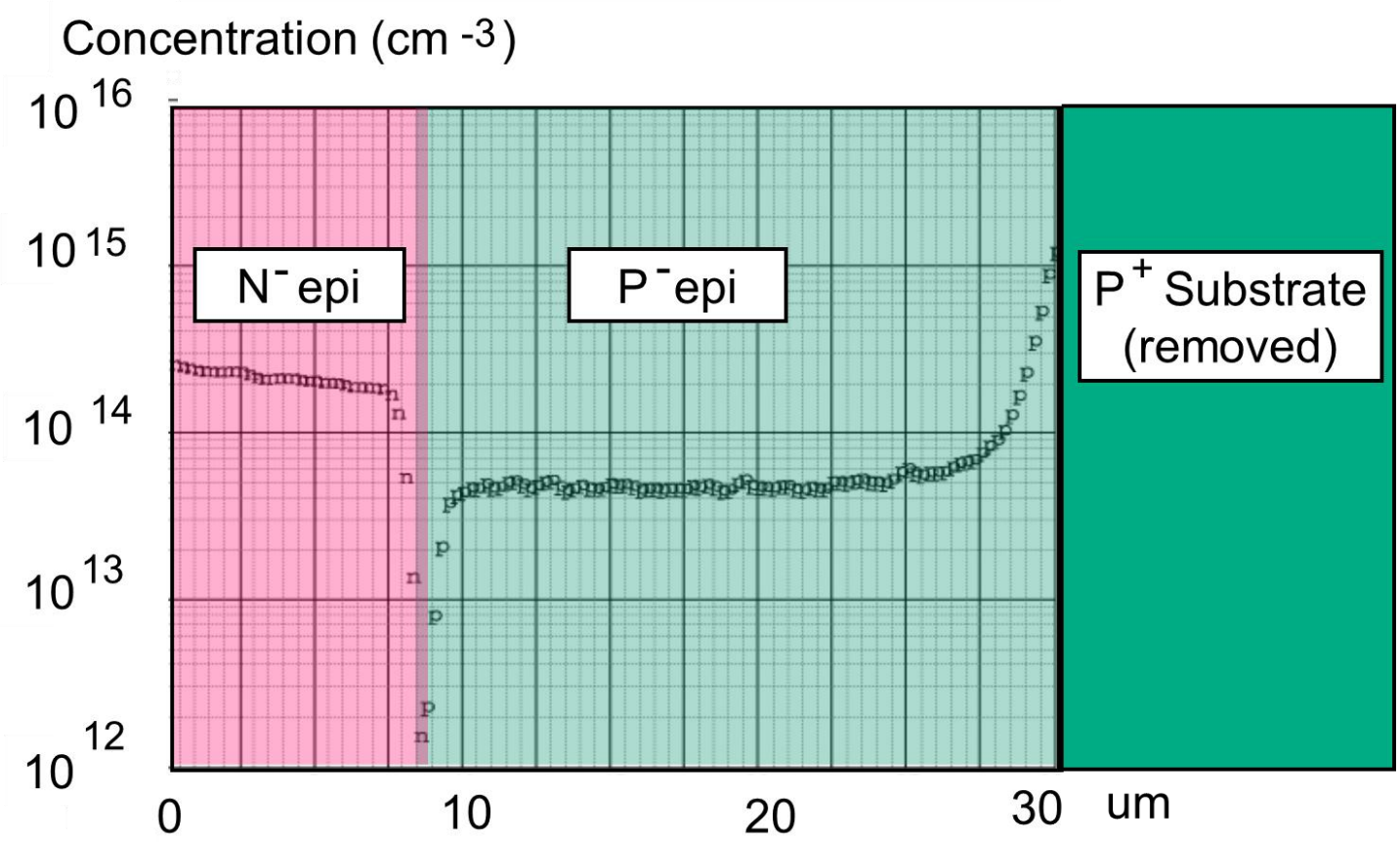
Front side memory →
- Intrusion of some incident light
- Migration of photoelectrons

↓ Best solution

Tetra-stratified (pnpn) **Thick layer** BSI

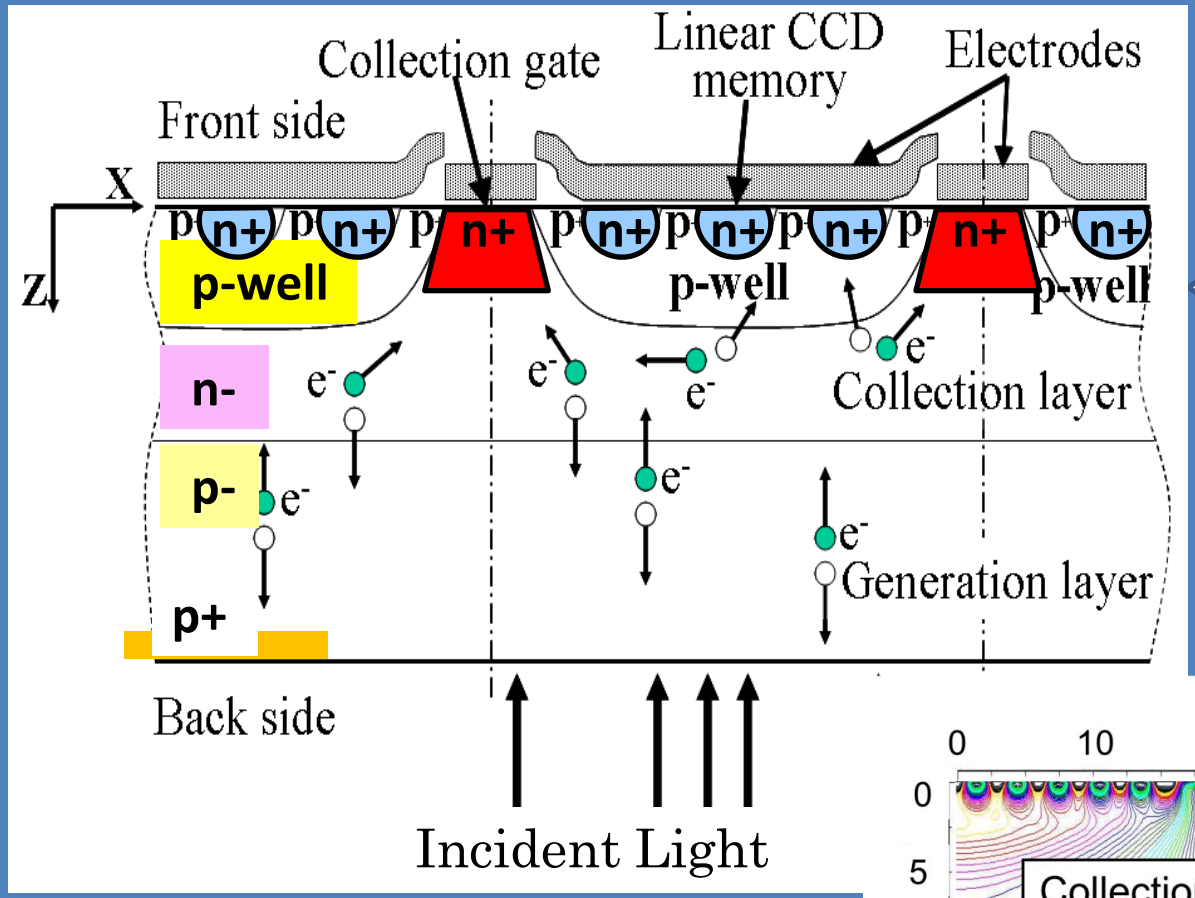
Prevents ↓ Migration of photoelectrons

Prevents ↓ Intrusion of some incident light



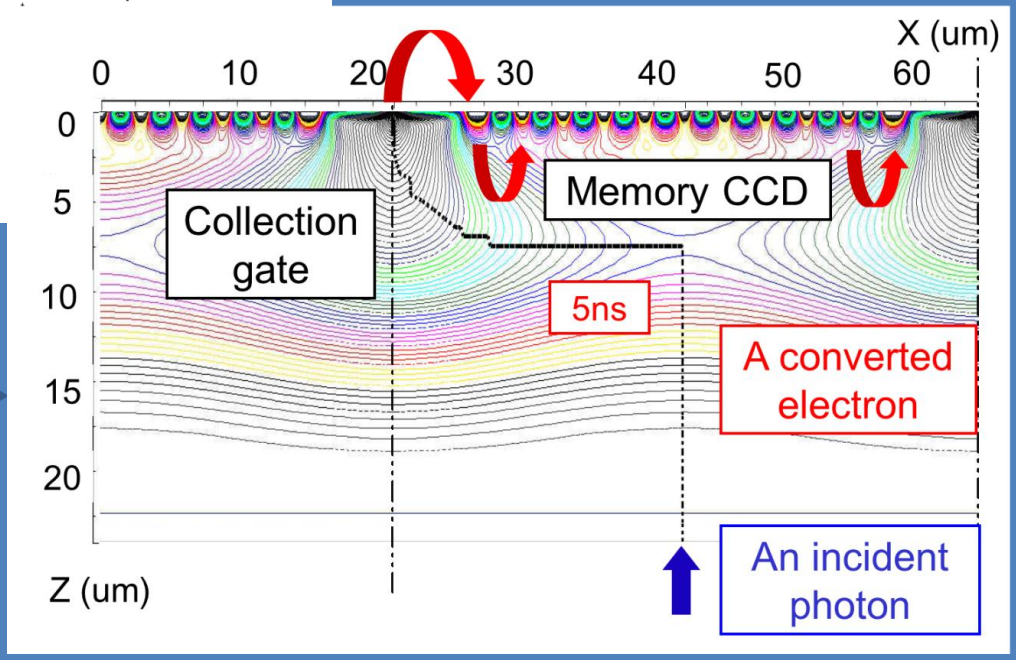
Starting Material for Tetra-stratified BSI “Double-epi Wafer”

Current recommended conditions:
p-epi concentration: $\leqq 10^{13}$ cm^{-3}
Thickness: n-epi 11um; p-epi 39um; total: 50um

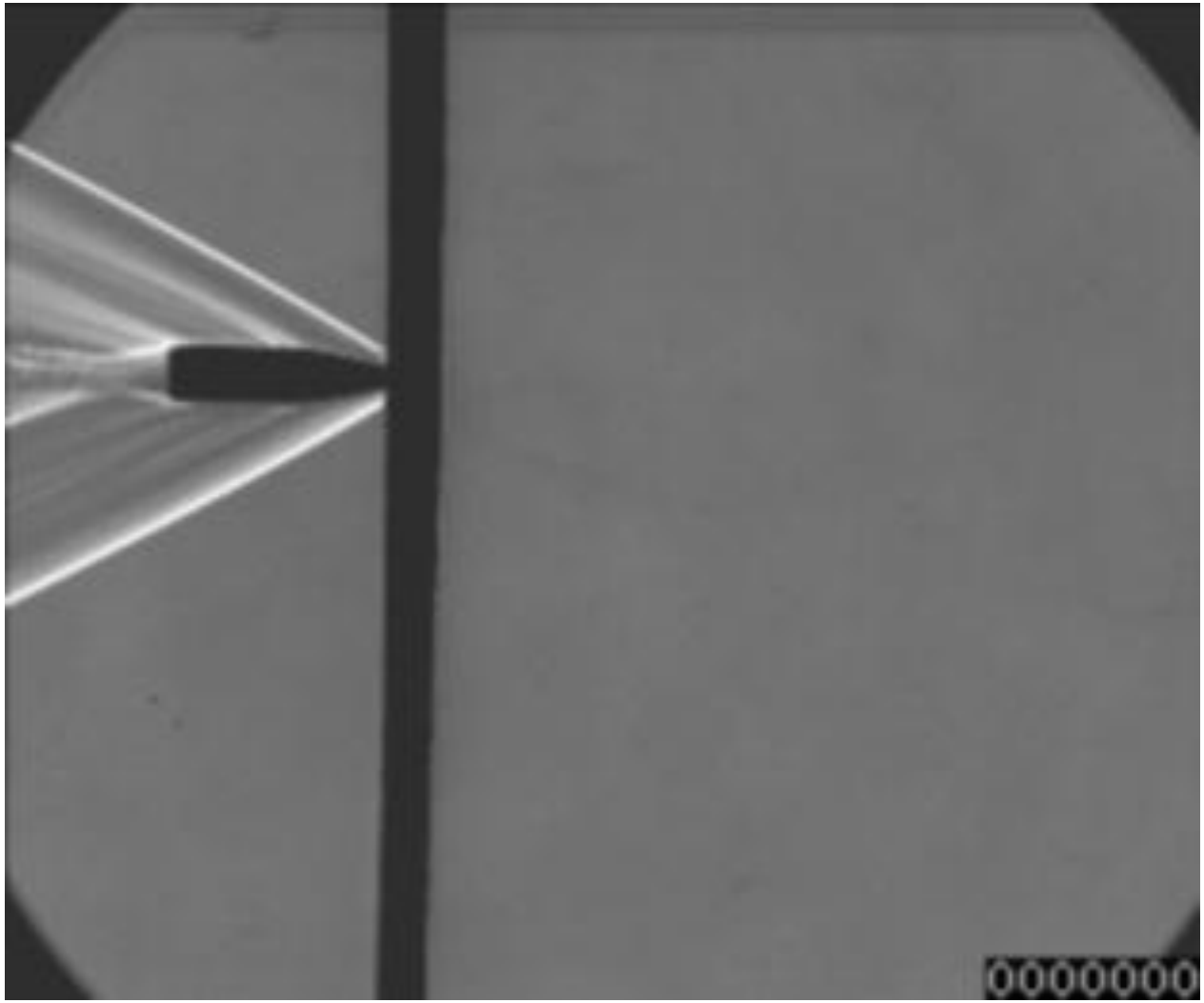


Cross-section of developed tetra-stratified BSI

Example of a potential contour



Examples of Ultra High Speed Imaging

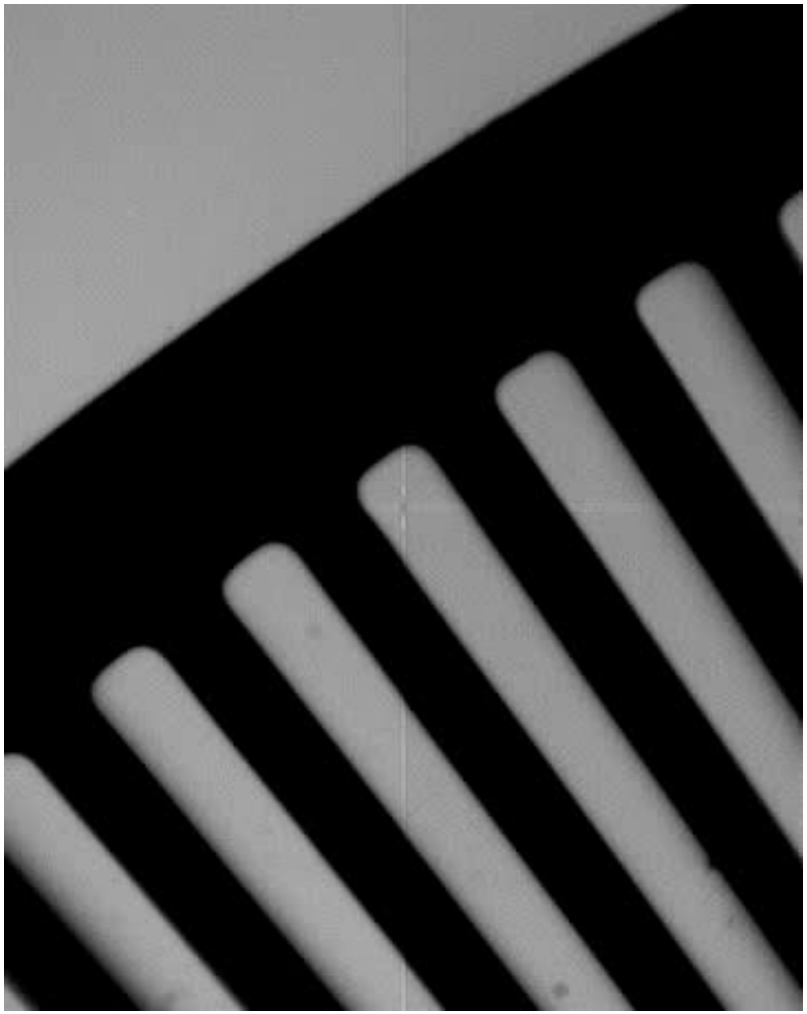


Bullet shot by ISIS-V2 (500kfps, 86kpixels)

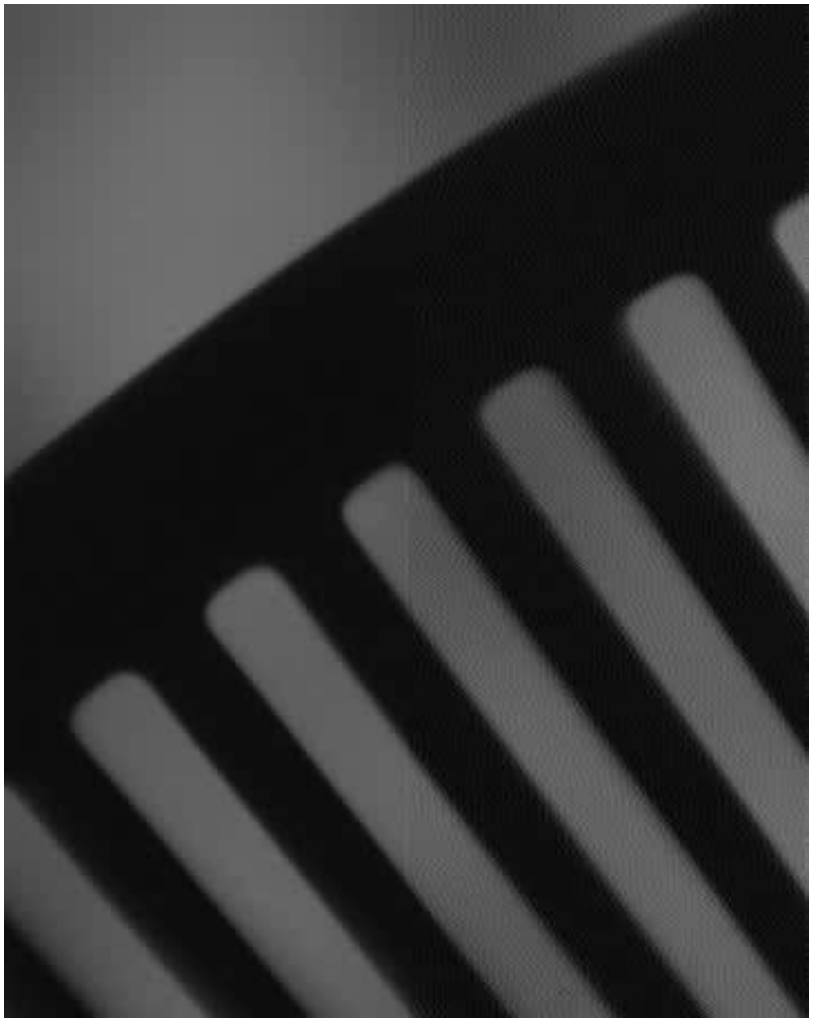
*By courtesy of Prof. Kleine

Thunderbolt (experiment) shot by ISIS-V4
(1Mfps, 300kpixel, Color)

*By courtesy of NHK



1Mfps



16Mfps

Laser chopper (6,000rpm) shot by
ISIS-V16 (165kpixel BSI)

Ultimate High Speed Imaging

General imaging

(1) Charge collection process:

It requires a short time.

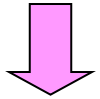
(2) Charge transfer process:

It requires a little short time.

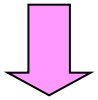
(3) Signal readout process:

It requires a long time.

By using analog memories directly connected to pixels, **current high speed imaging** has been done without the signal readout process. So it consists of (1) charge collection process and (2) charge transfer process.



If the imaging can be done only by the charge collection process, the ultimate high speed imaging will be achieved!!

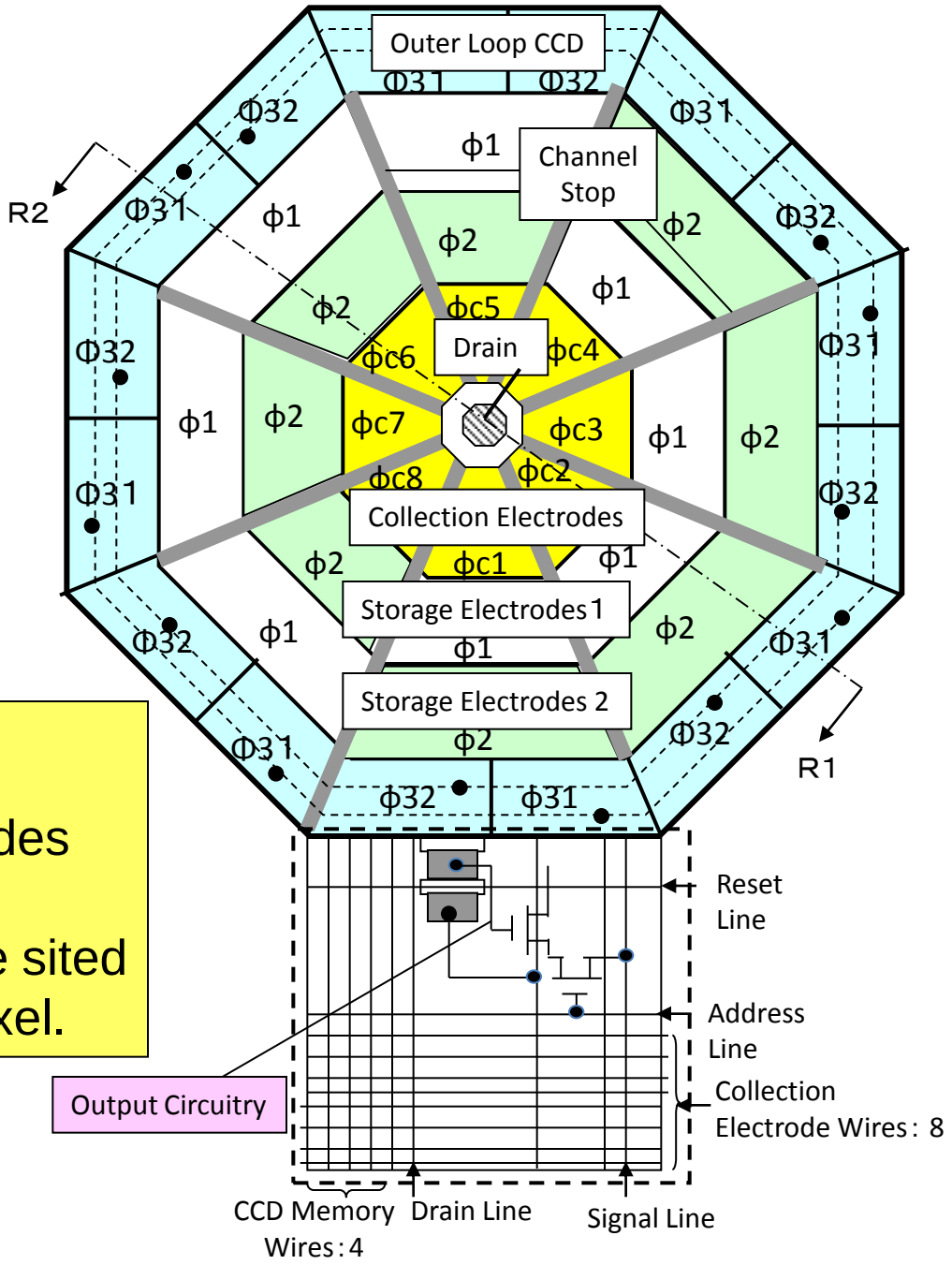


Solution (Proposed)

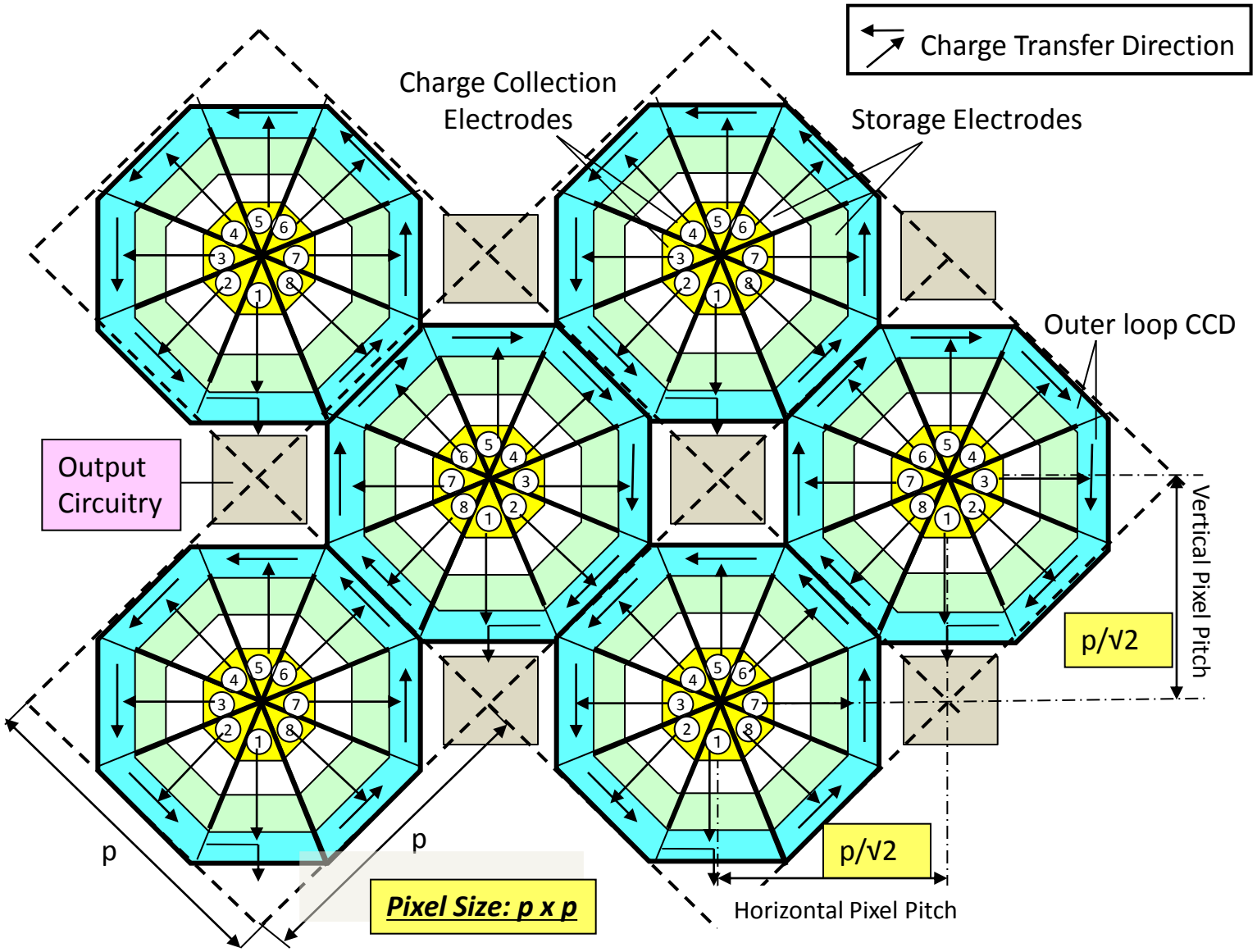
New architecture of in-pixel multi-collection gates

Key technologies

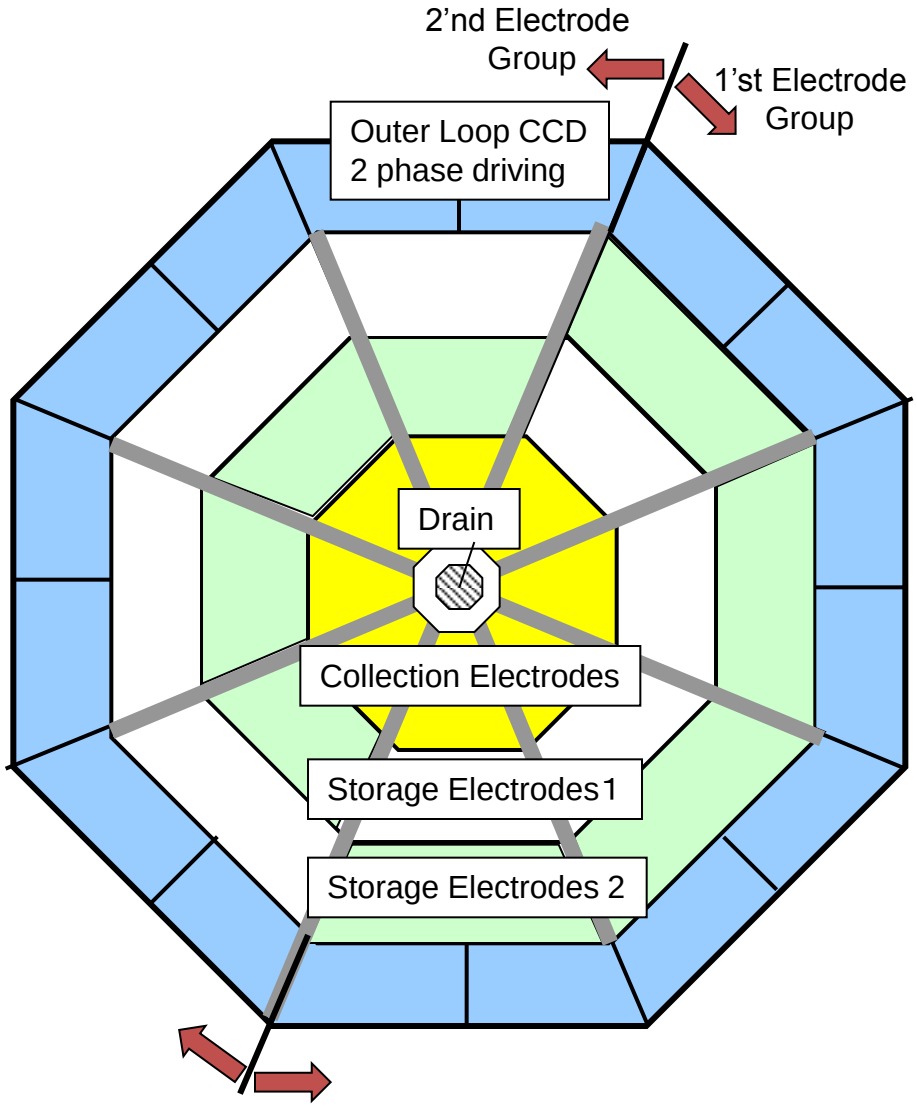
(1) Numbers of collection electrodes are in a pixel.
(2) All of collection electrodes are sited on the central region in the pixel.



New Pixel Layout

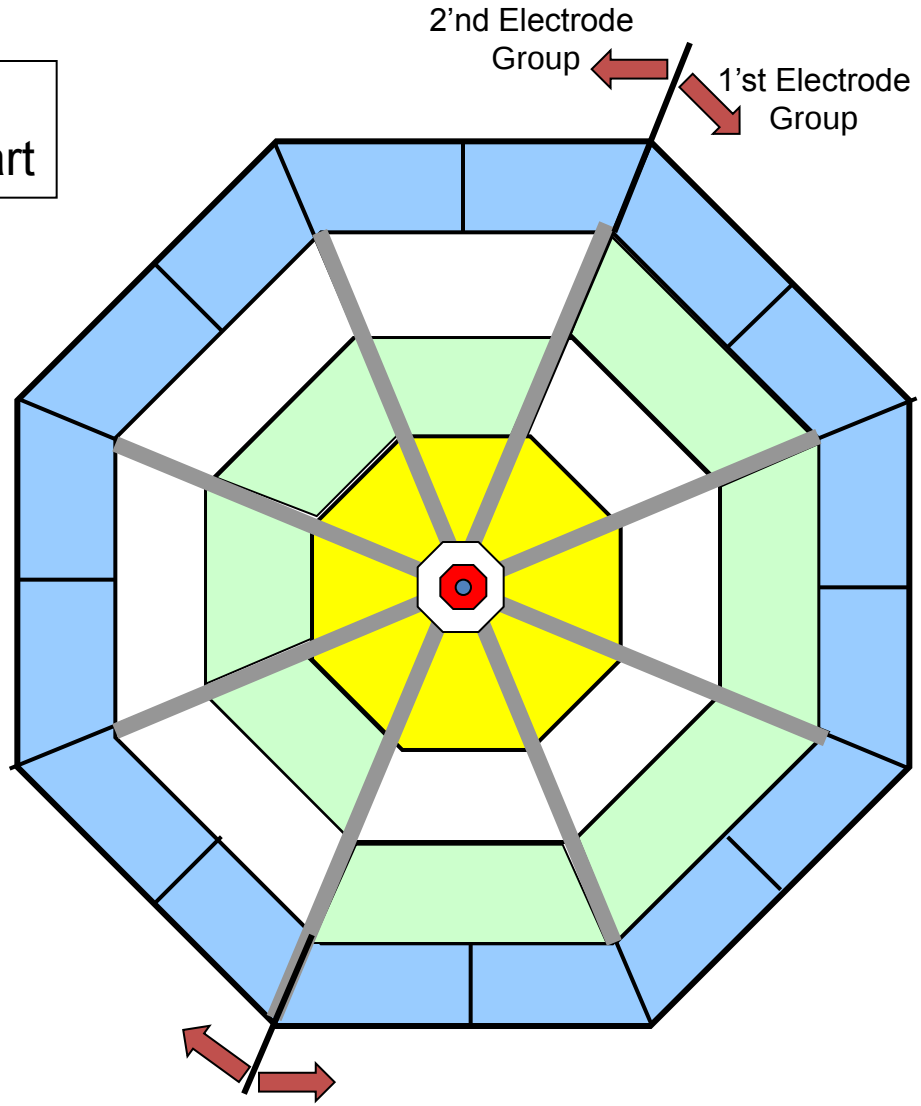


An Example of Pixel Arrangement (Pixel Interleaved Array)

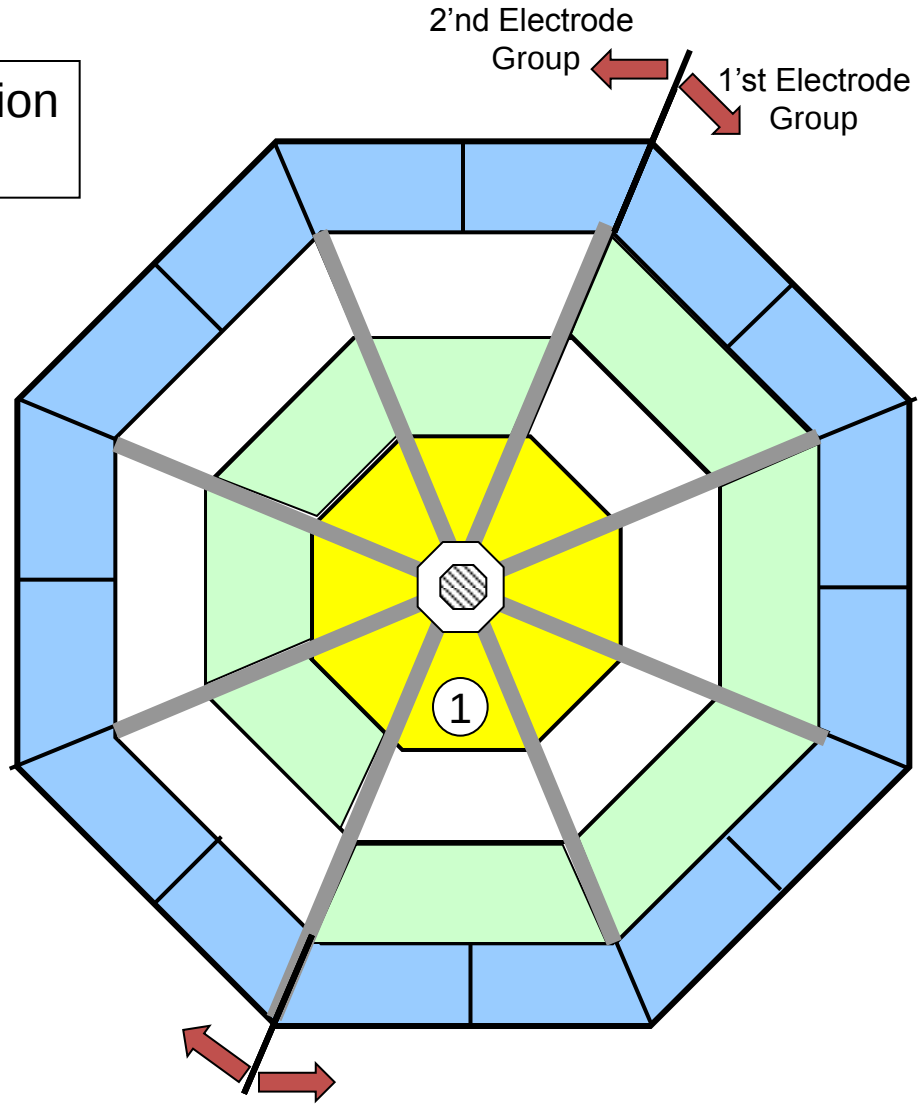


Principle of heightening an imaging speed by the in-pixel multi-collection gates

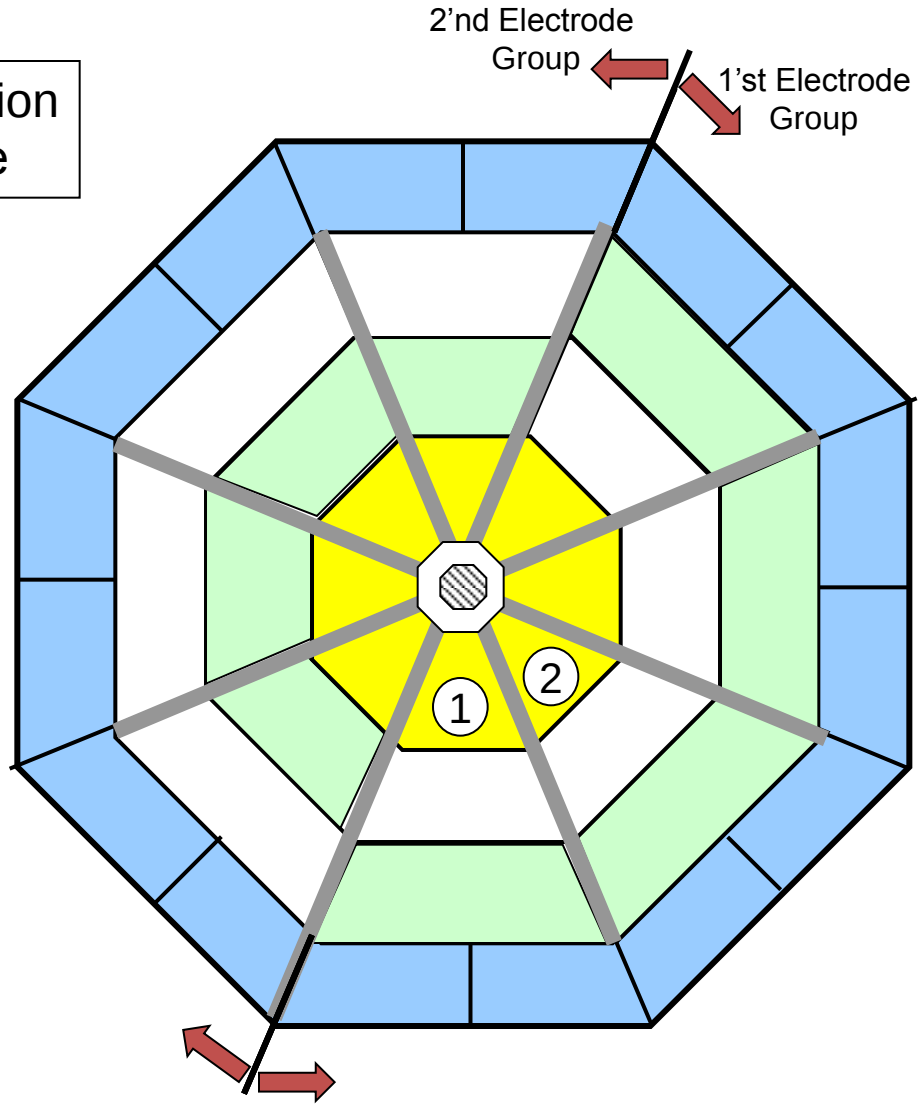
Global Reset
→ Imaging Start



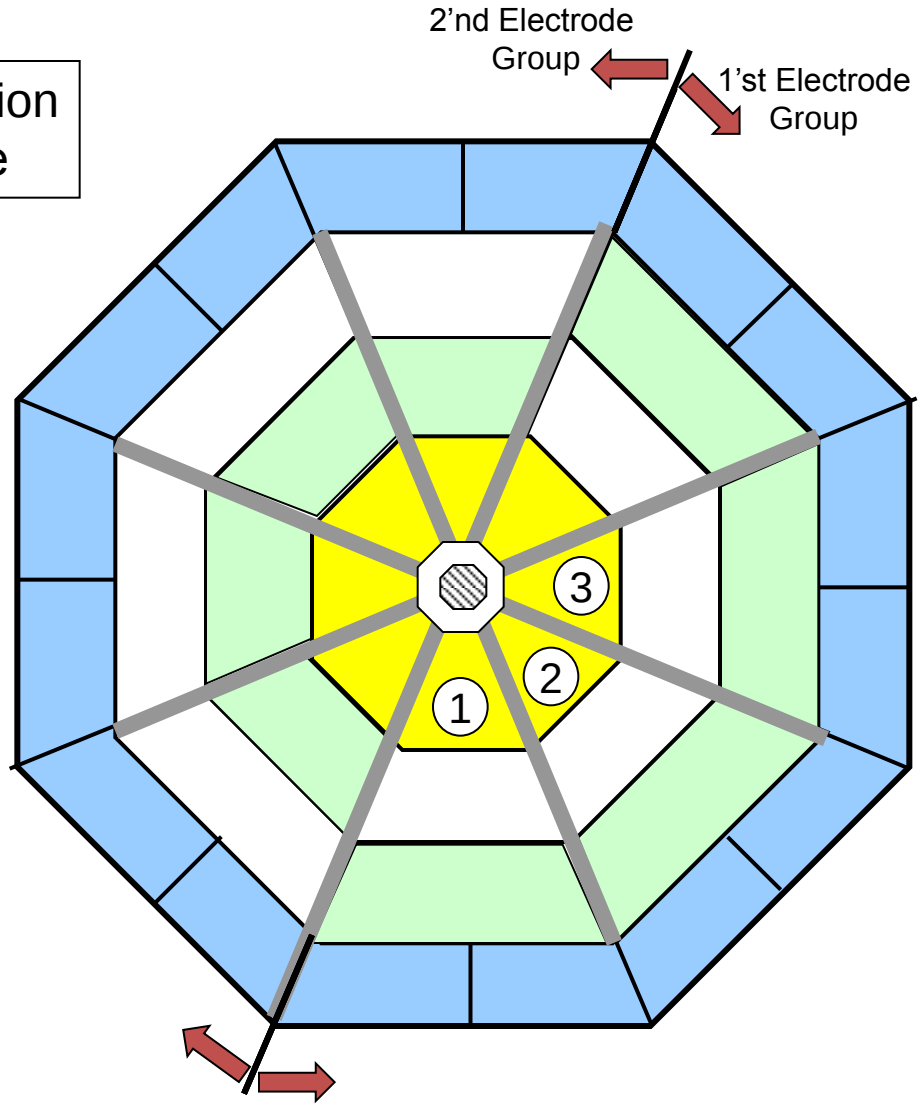
Charge collection of 1’st frame



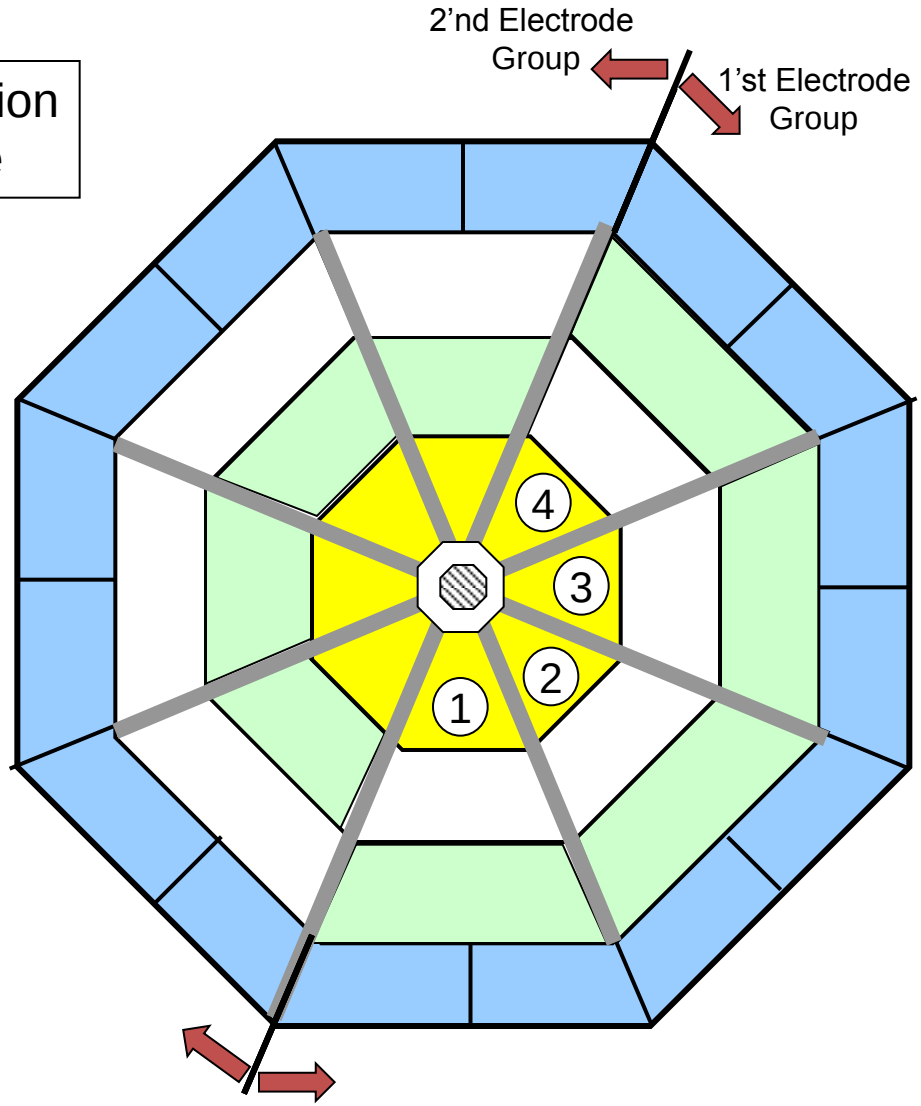
Charge collection of 2’nd frame



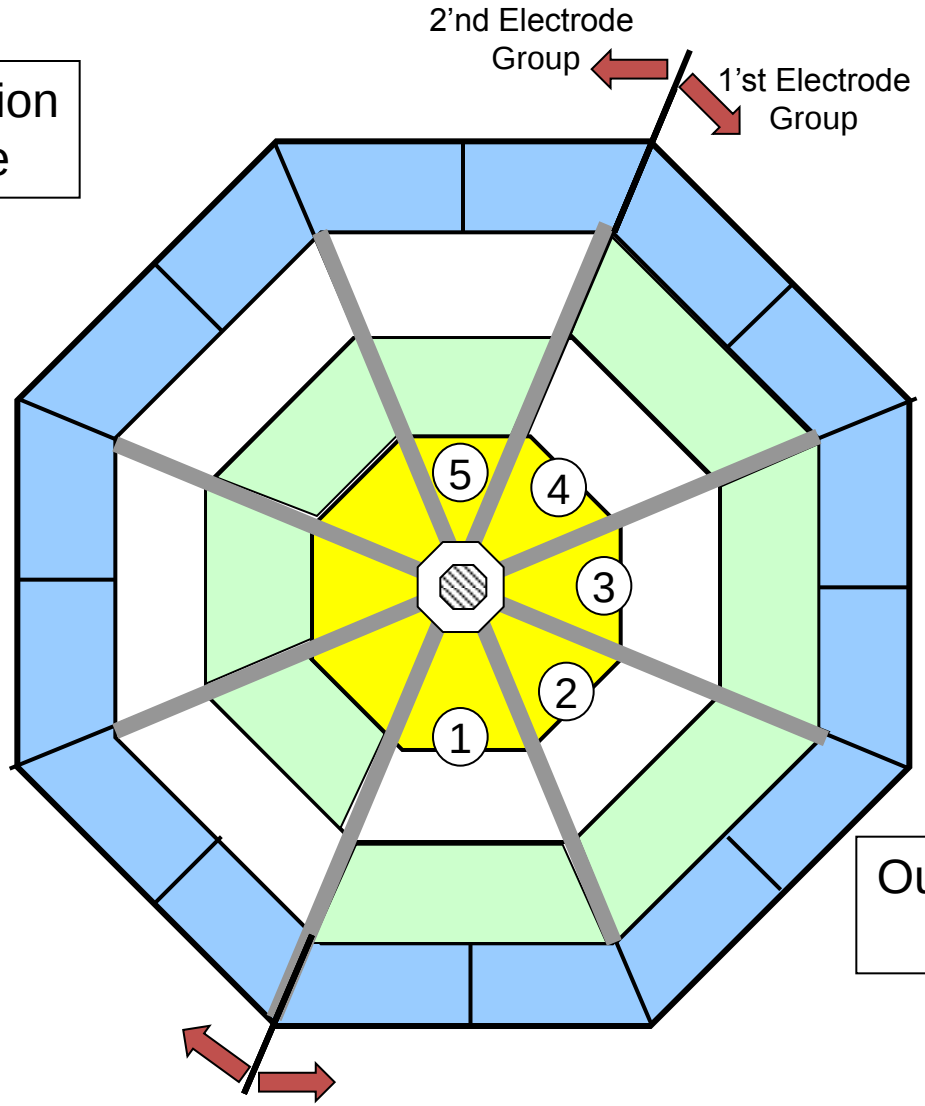
Charge collection of 3’rd frame



Charge collection of 4-th frame

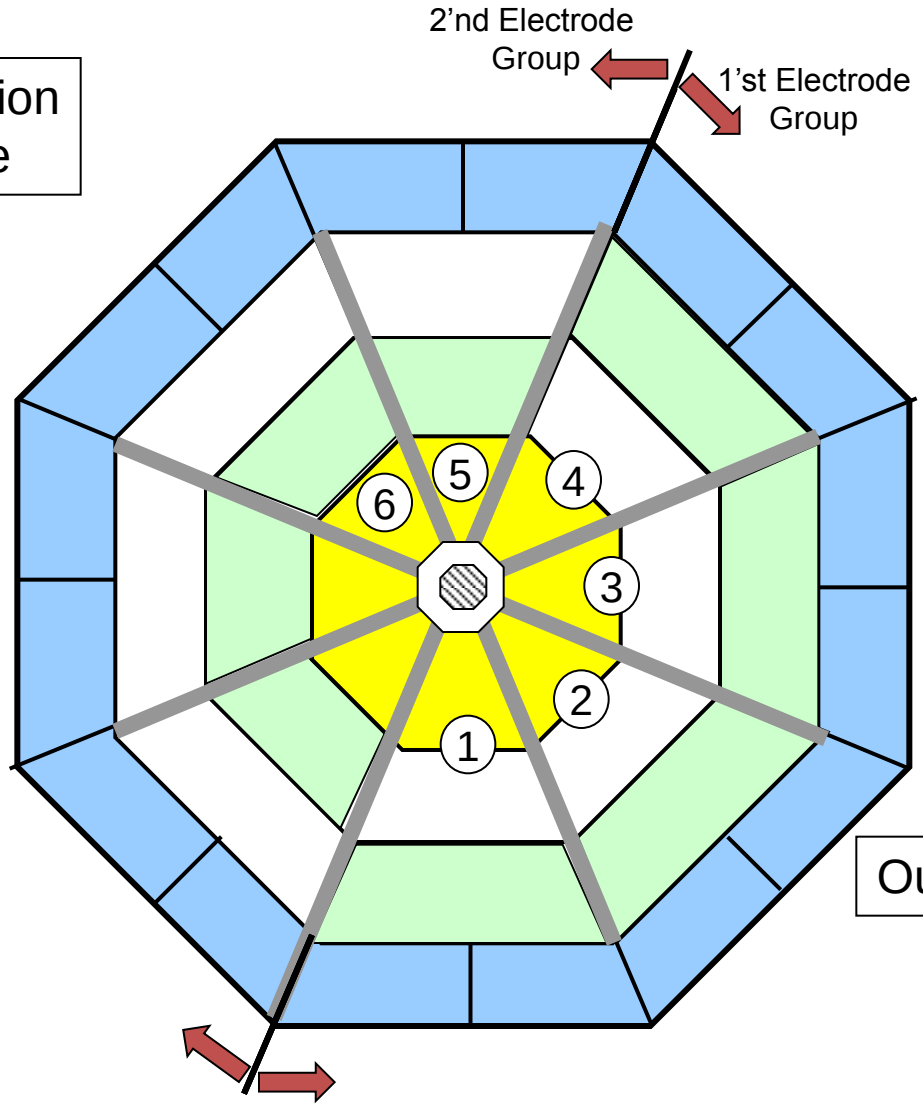


Charge collection
of 5-th frame



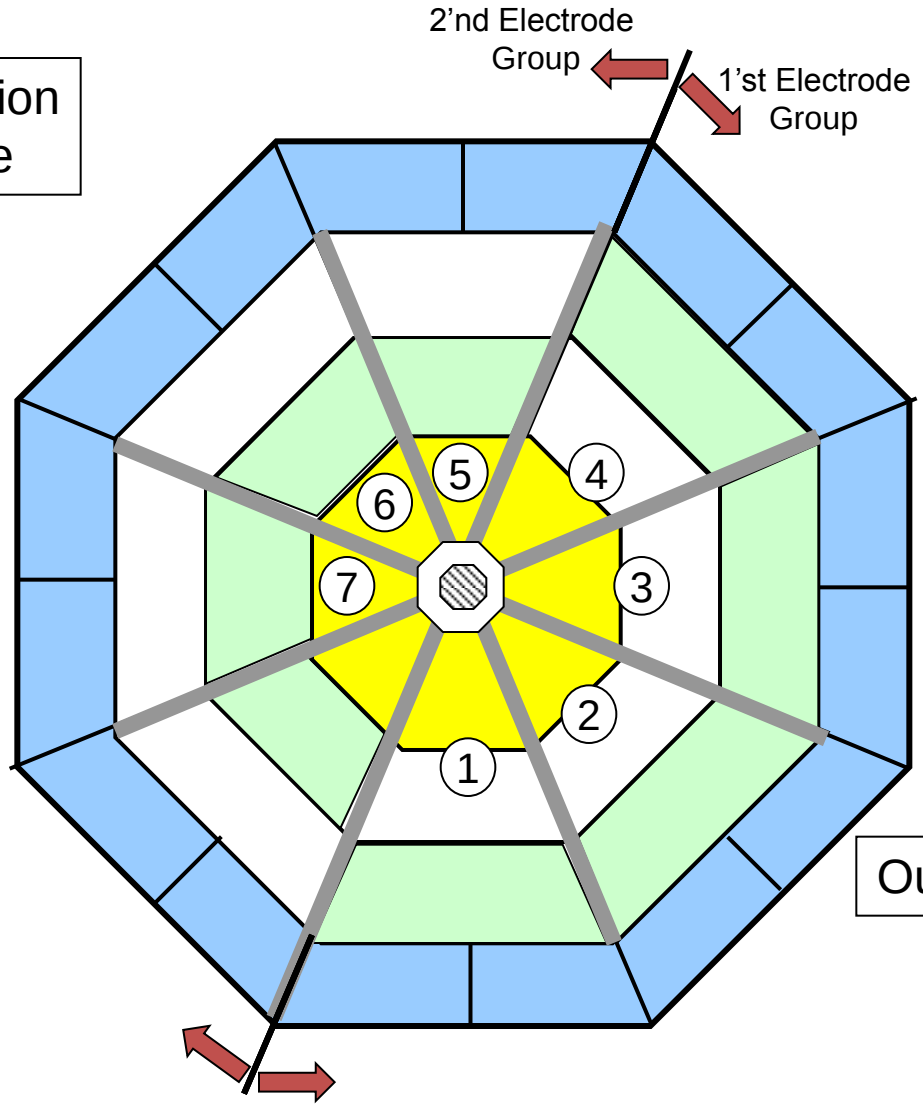
Outward transfer 1
→ Started

Charge collection of 6-th frame



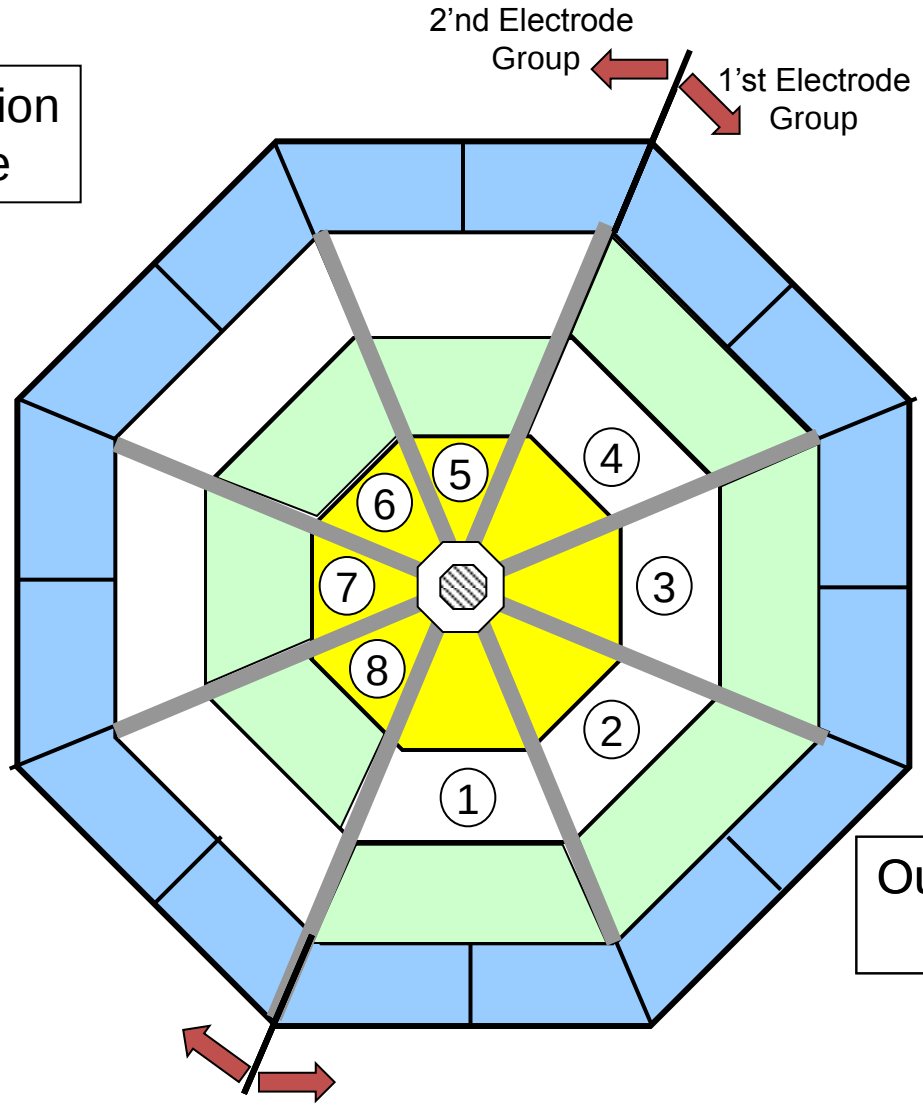
Outward transfer 1

Charge collection of 7-th frame



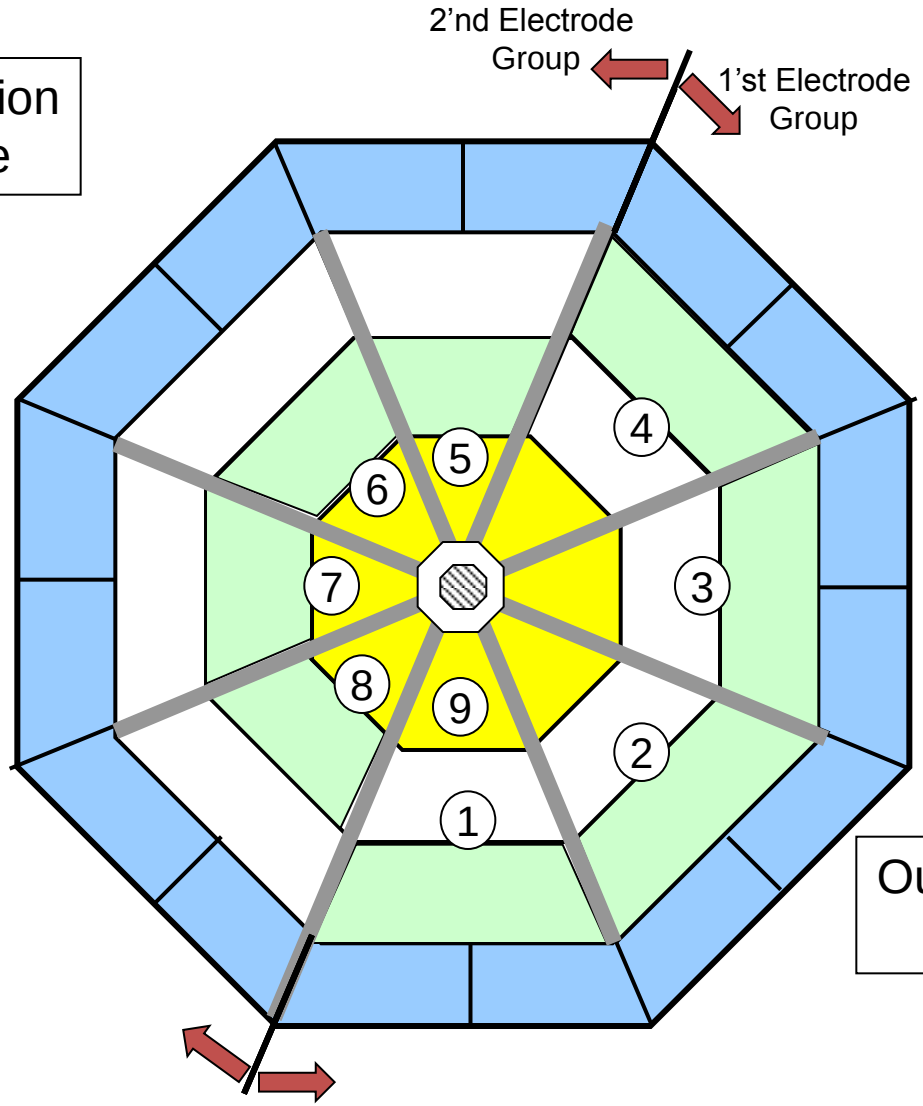
Outward transfer 1

Charge collection of 8-th frame



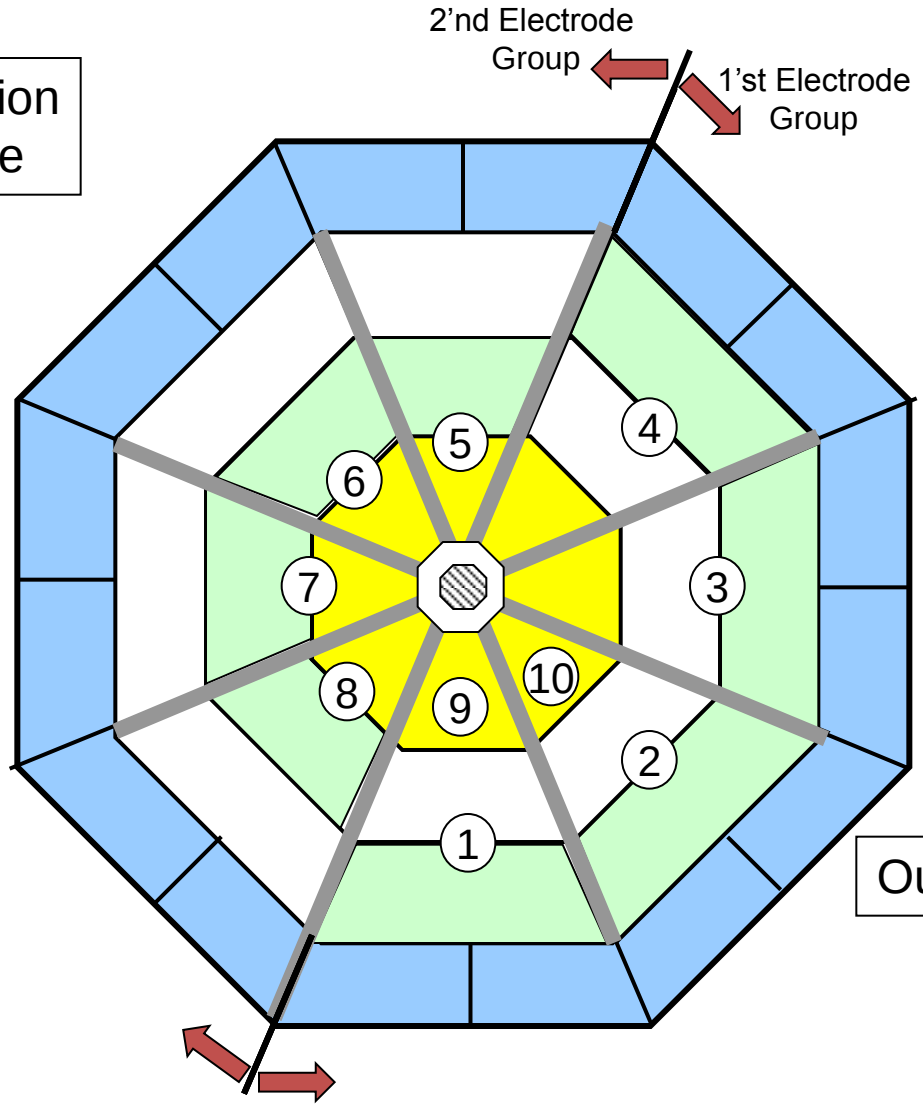
Outward transfer 1 → Finished

Charge collection of 9-th frame



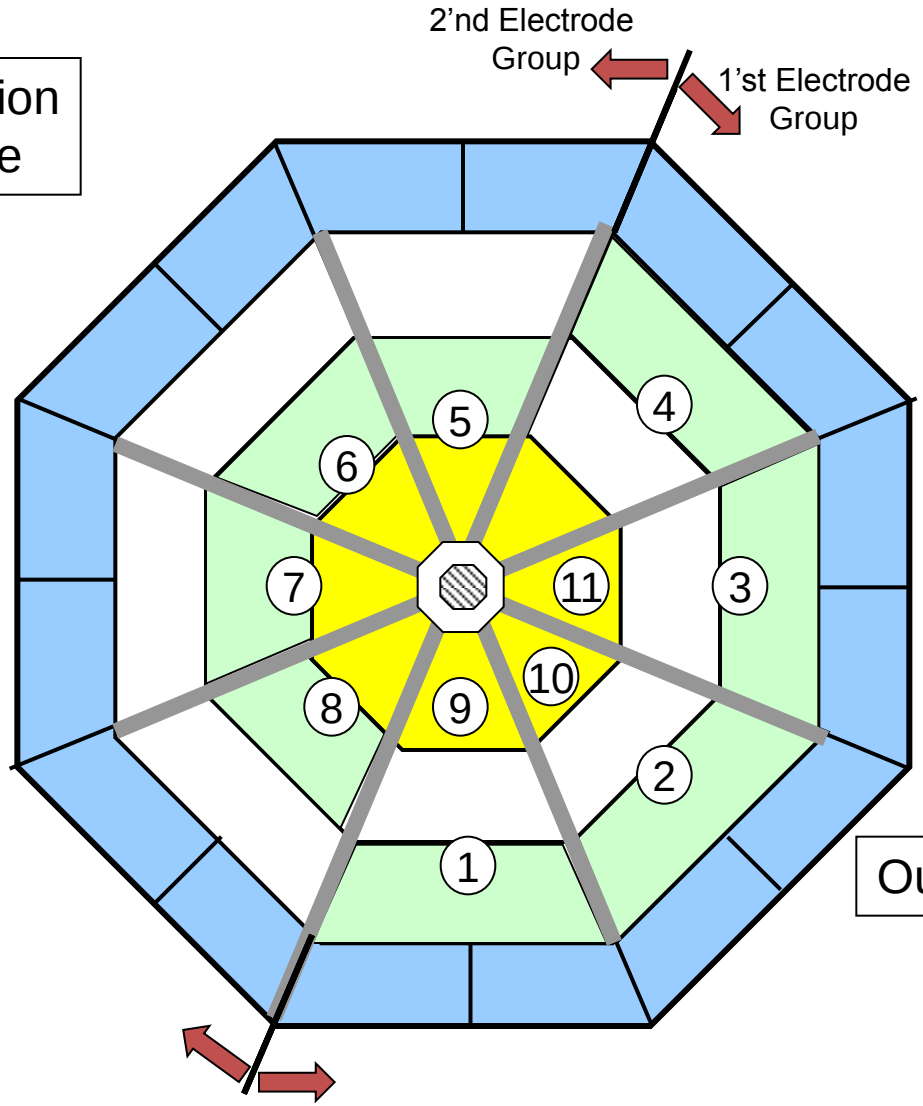
Outward transfer 2 → Started

Charge collection of 10-th frame



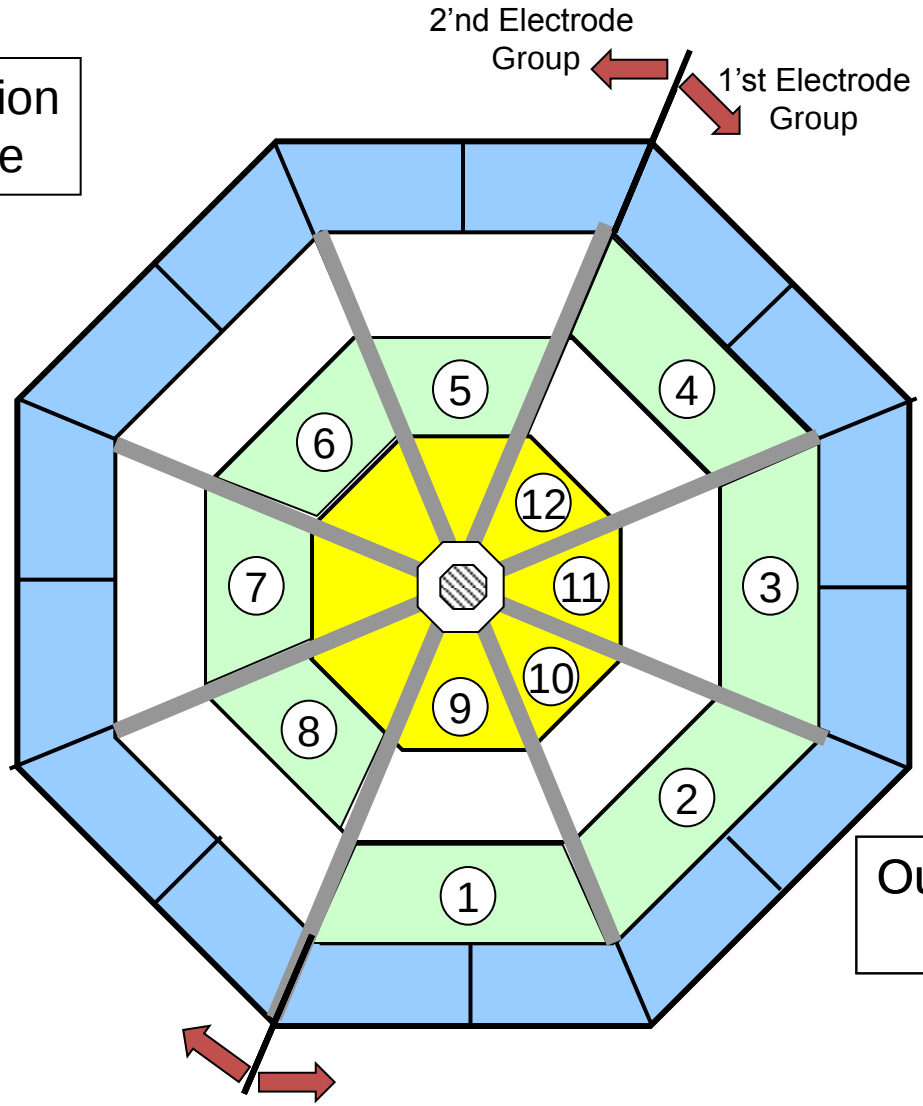
Outward transfer 2

Charge collection of 11-th frame



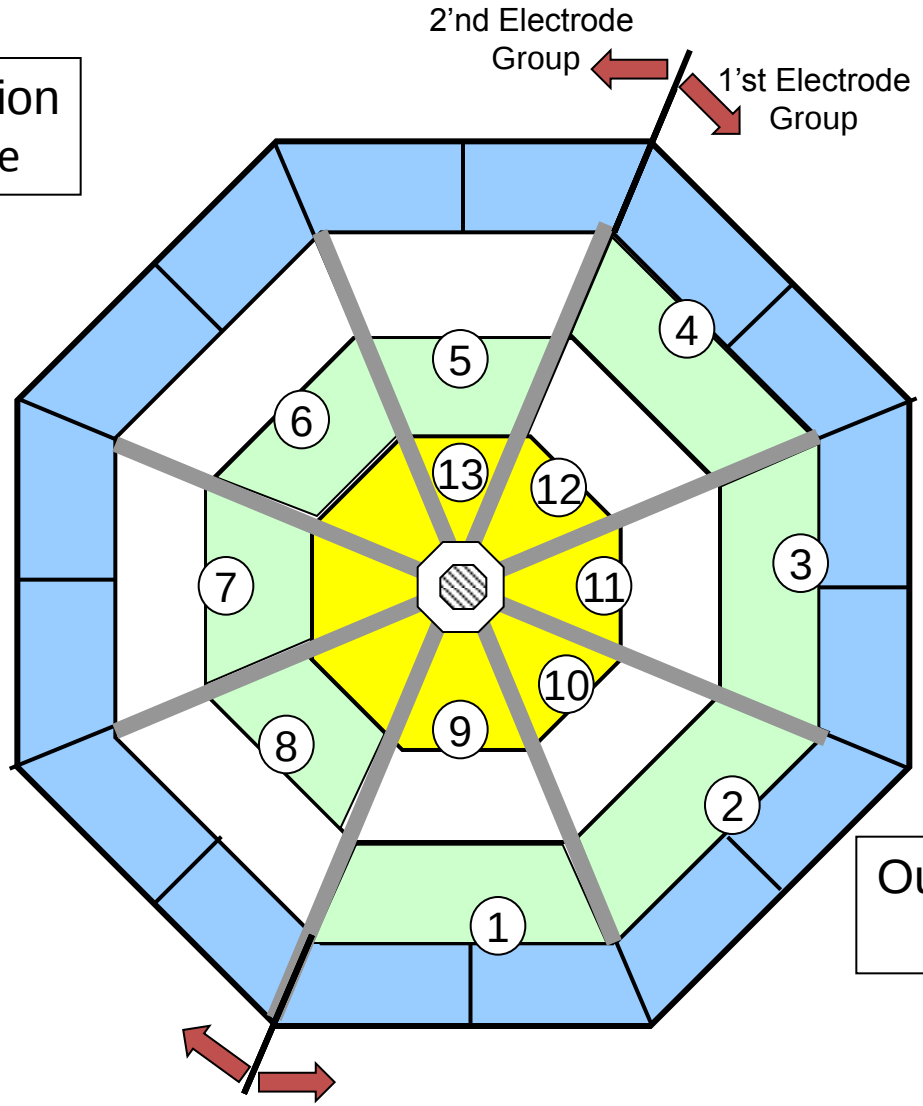
Outward transfer 2

Charge collection of 12-th frame



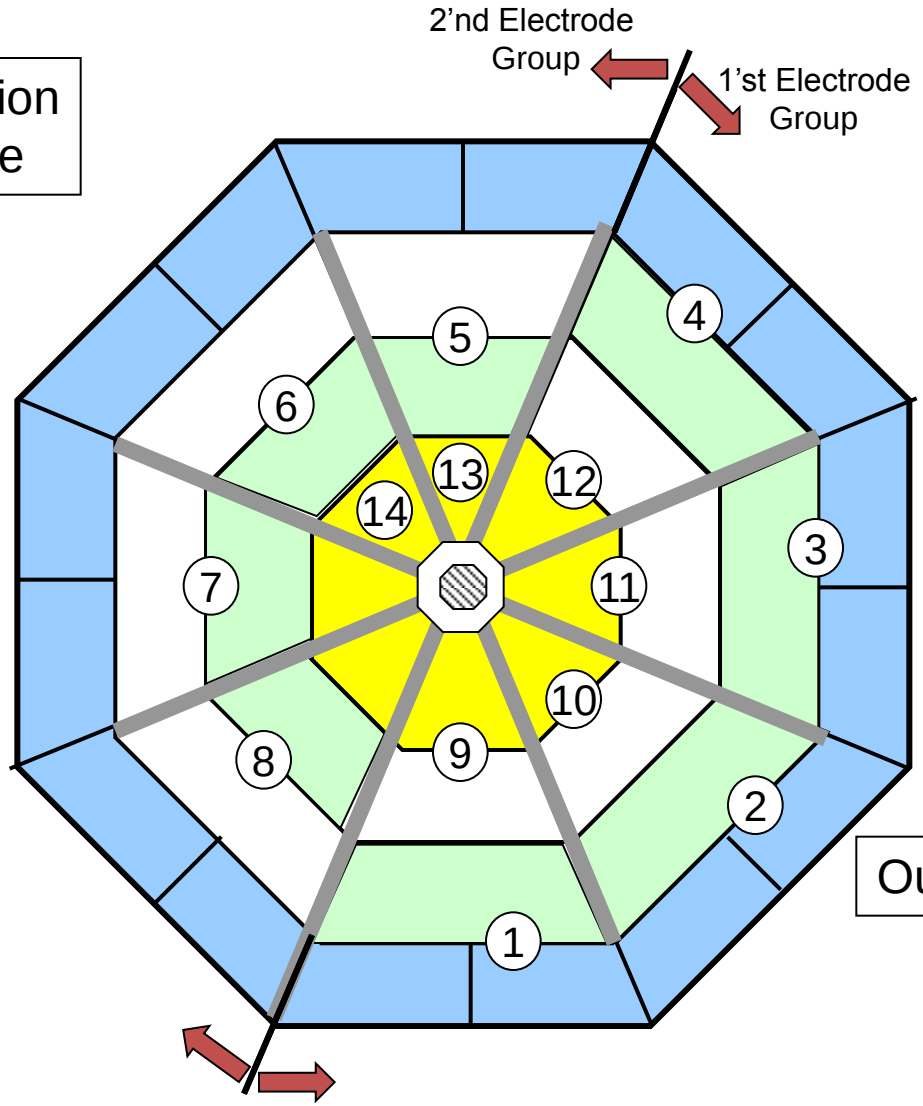
Outward transfer 2
→ Finished

Charge collection
of 13-th frame



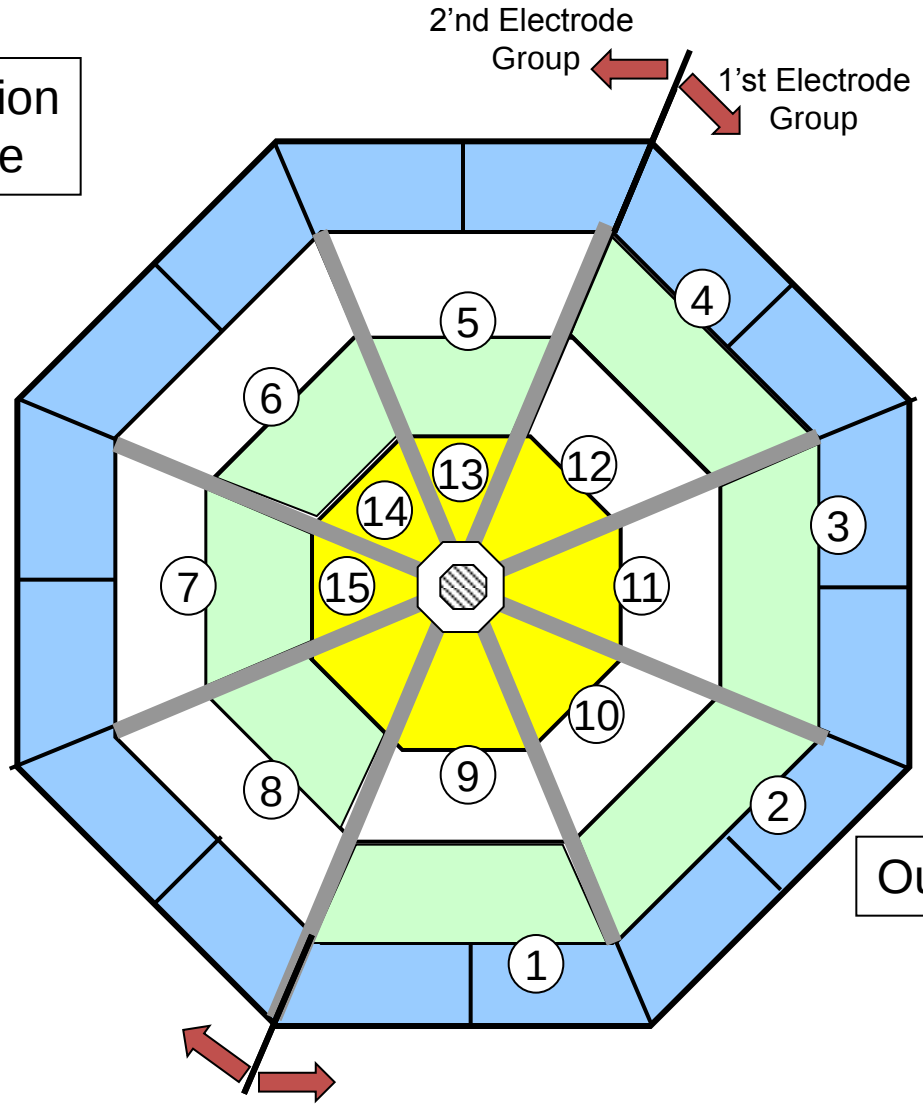
Outward transfer 3
→ Started

Charge collection of 14-th frame



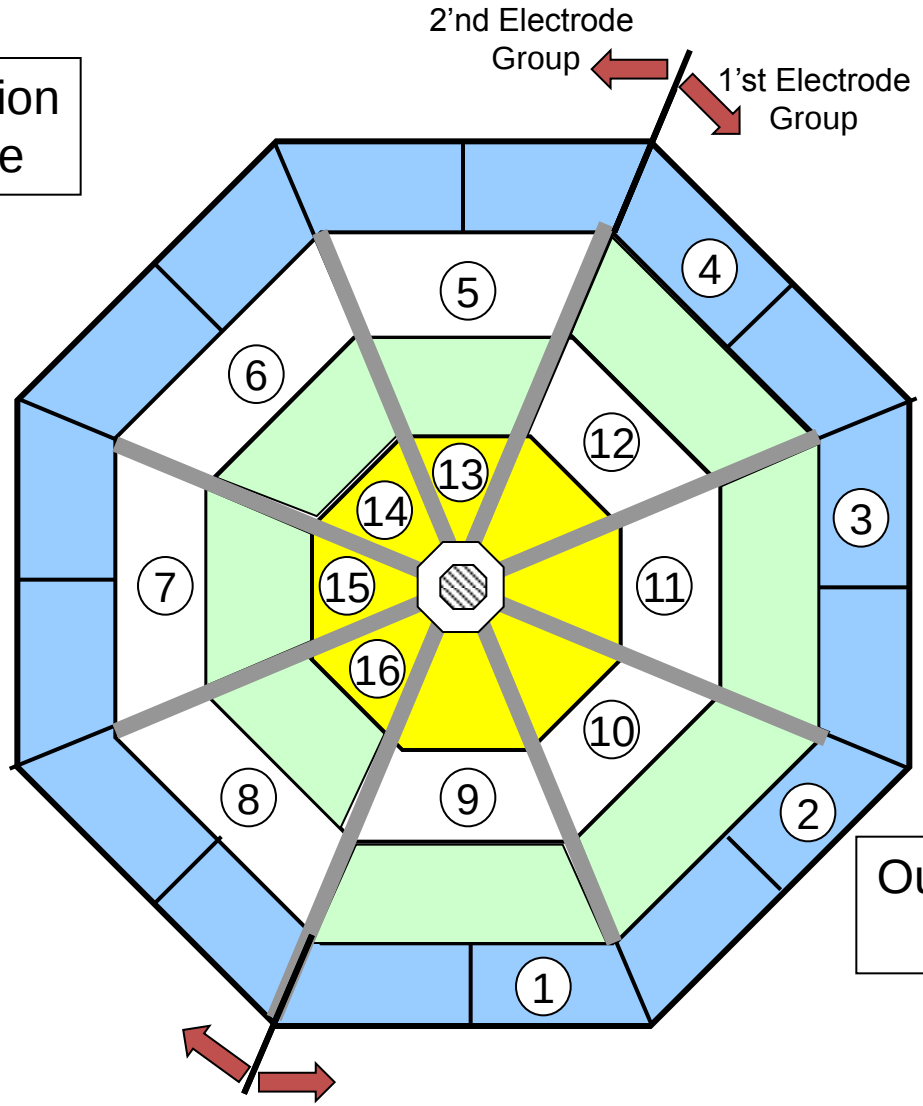
Outward transfer 3

Charge collection of 15-th frame



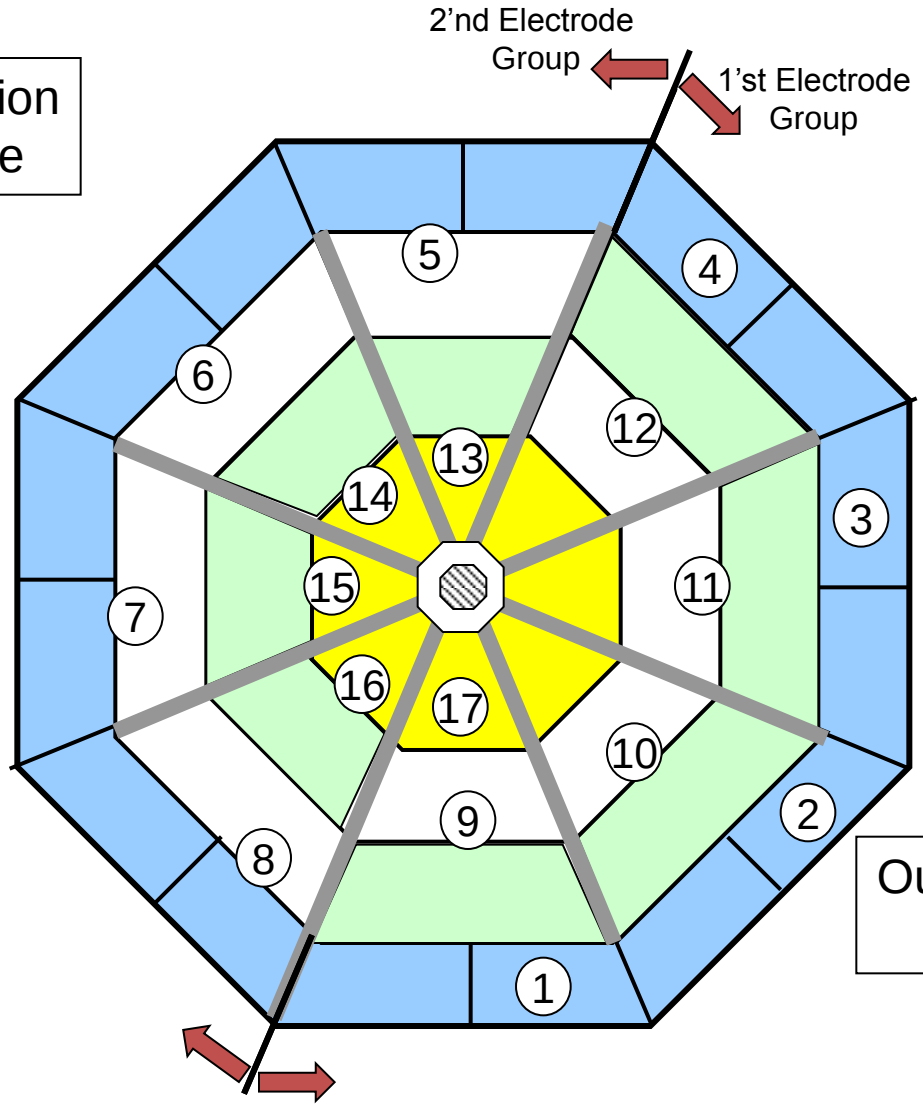
Outward transfer 3

Charge collection of 16-th frame



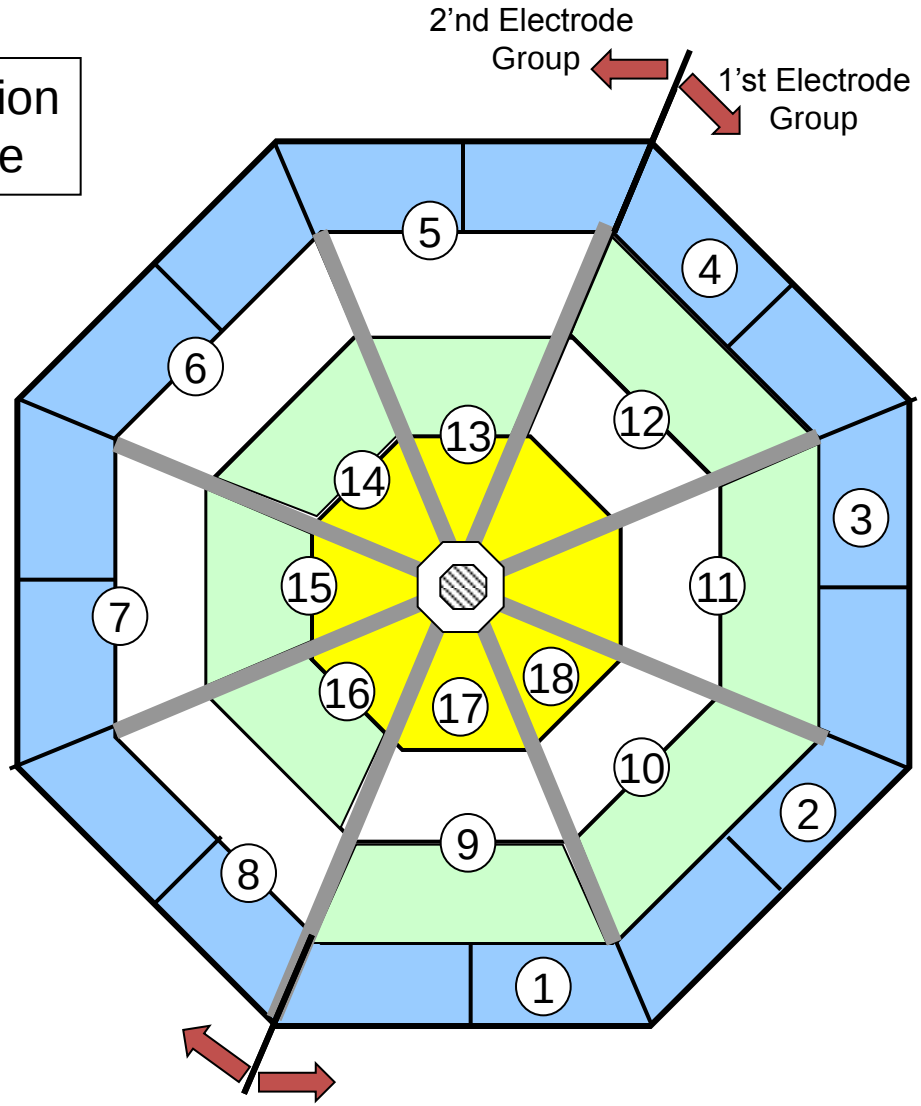
Outward transfer 3
→ Finished

Charge collection of 17-th frame

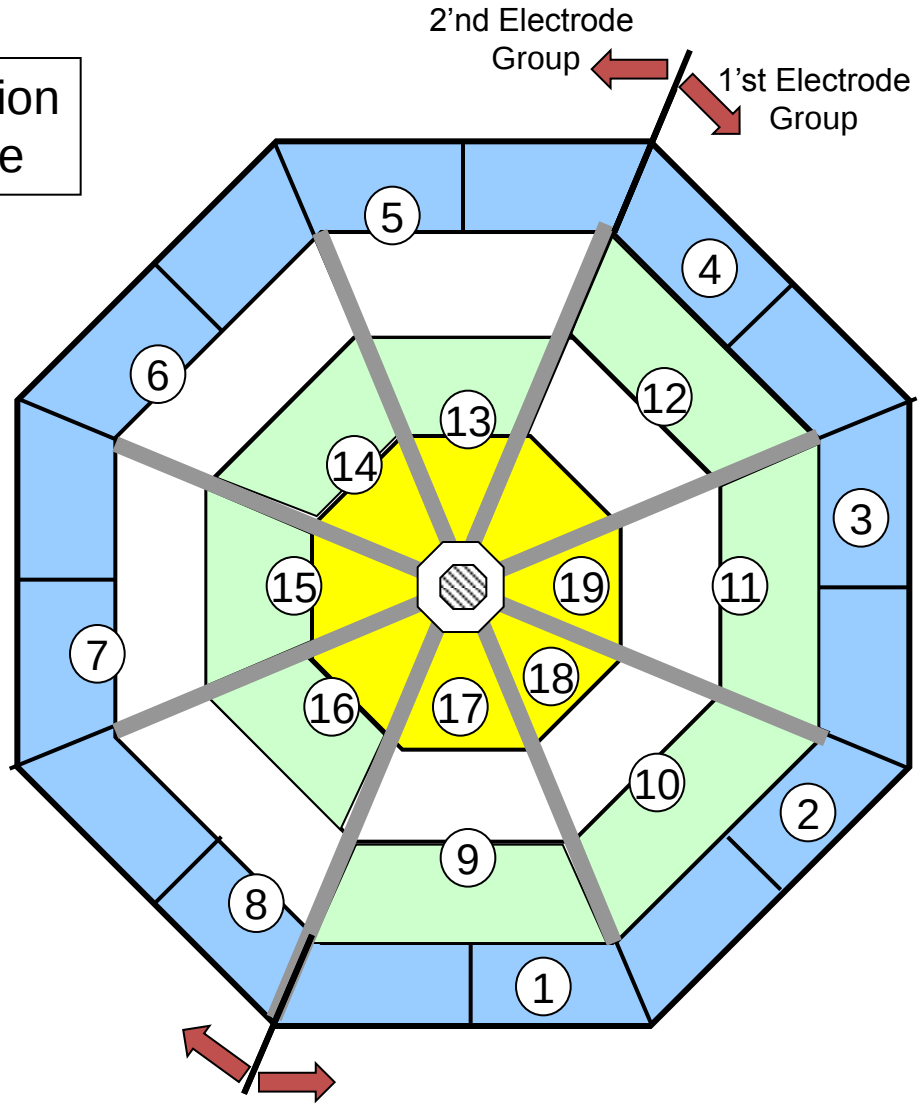


Outward transfer 4 → Started

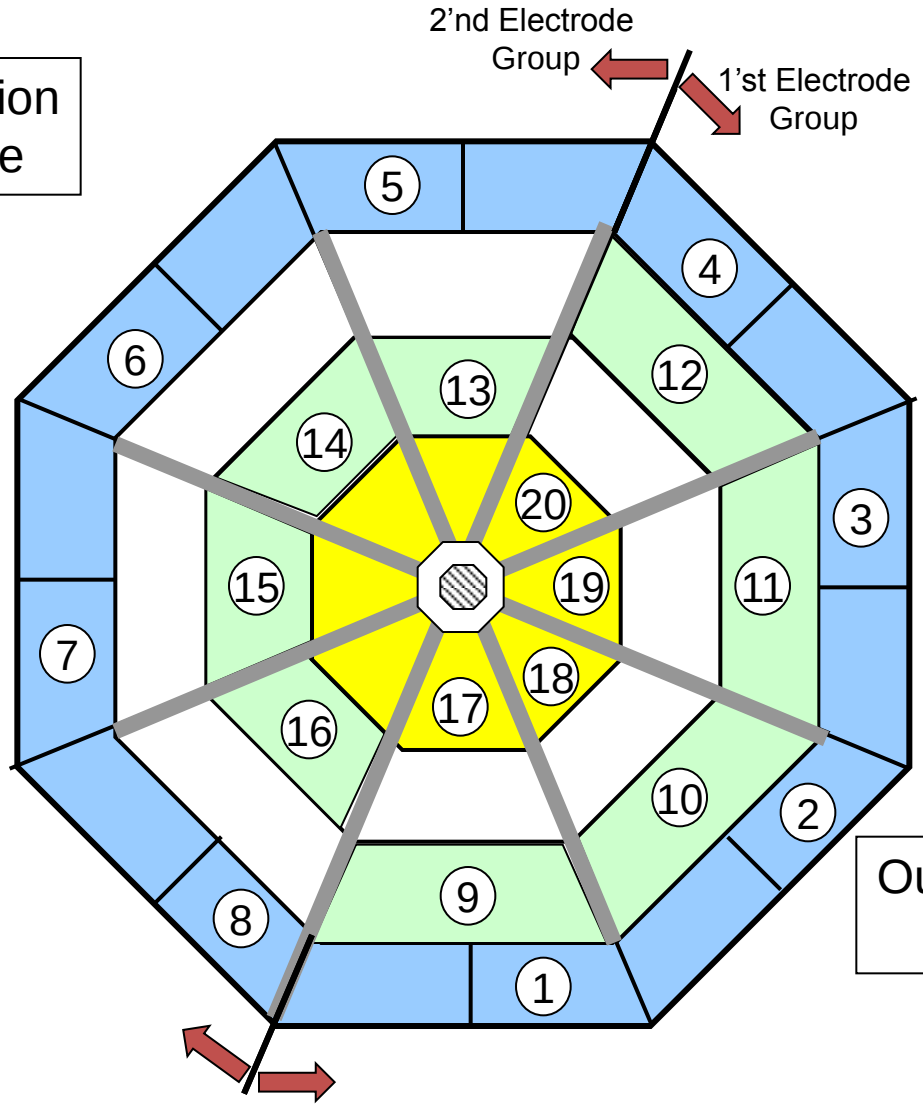
Charge collection of 18-th frame



Charge collection of 19-th frame

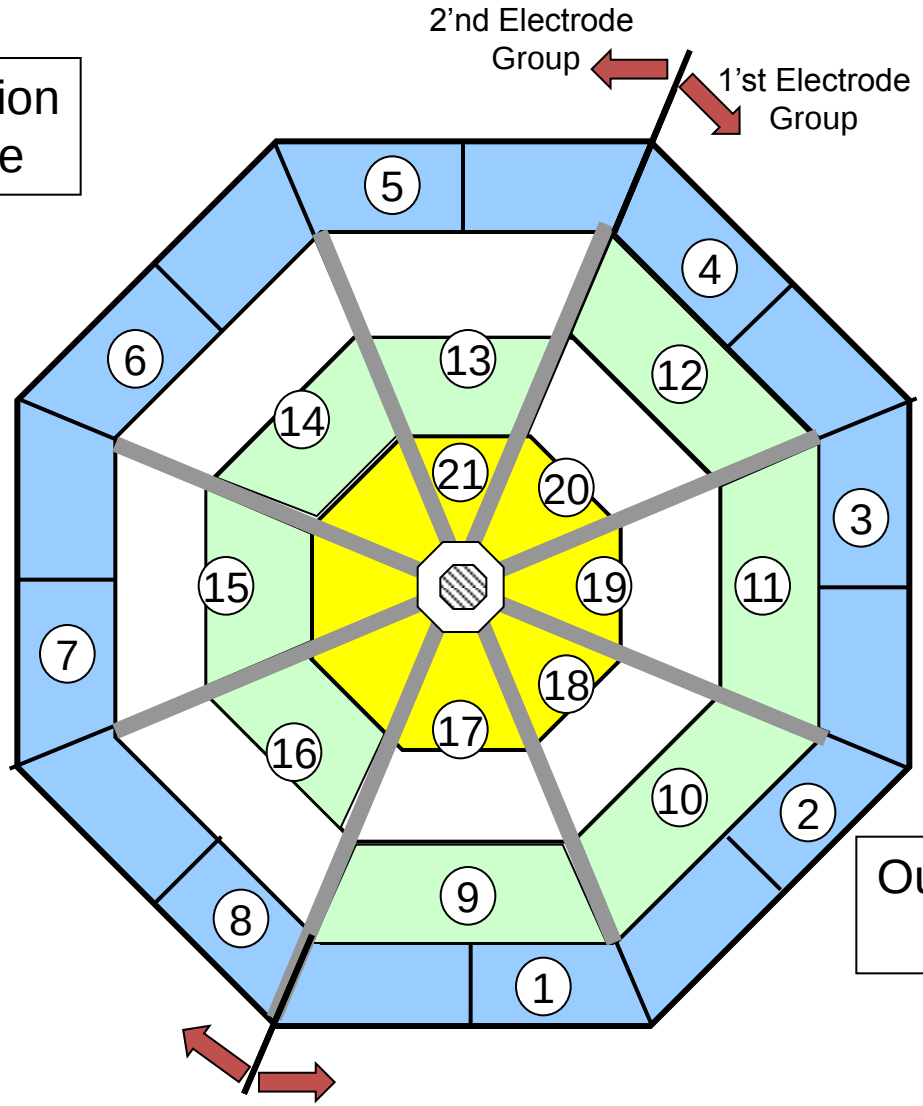


Charge collection of 20-th frame



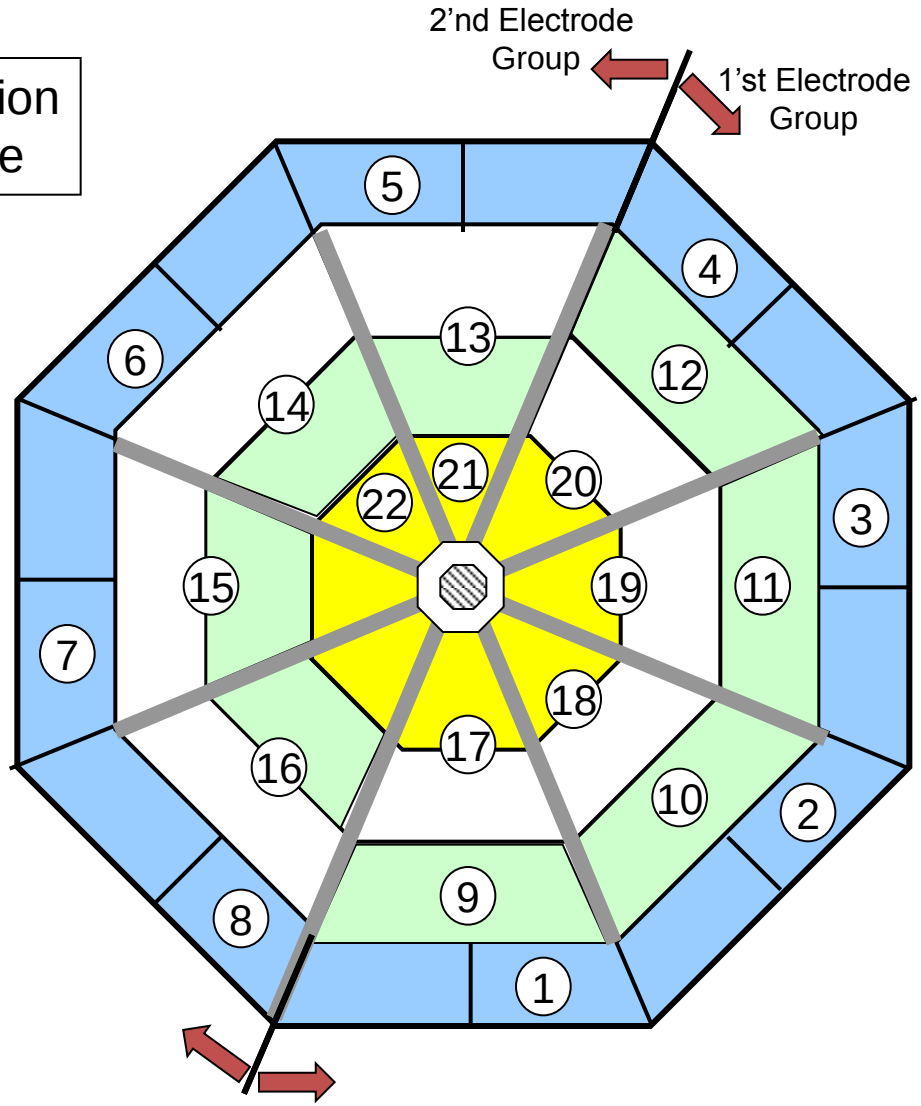
Outward transfer 4
→ Finished

Charge collection of 21-th frame

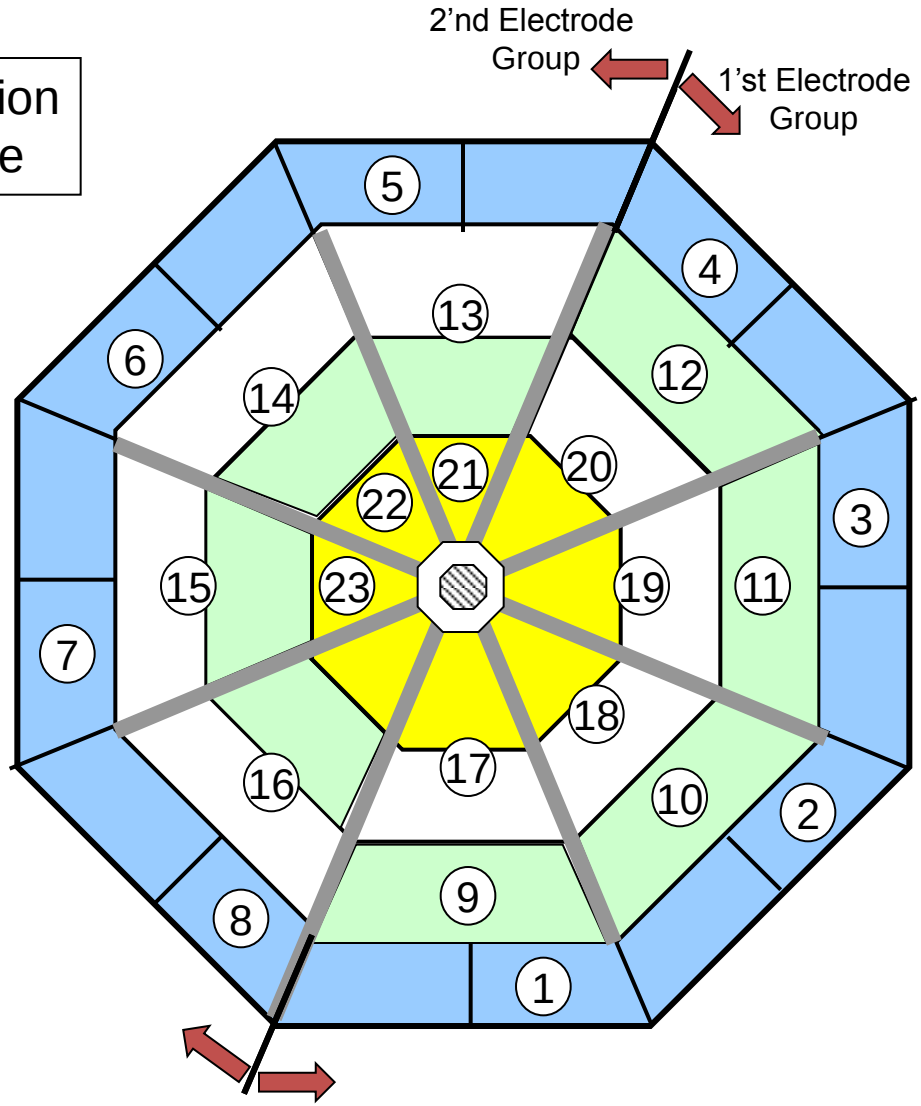


Outward transfer 5 → Started

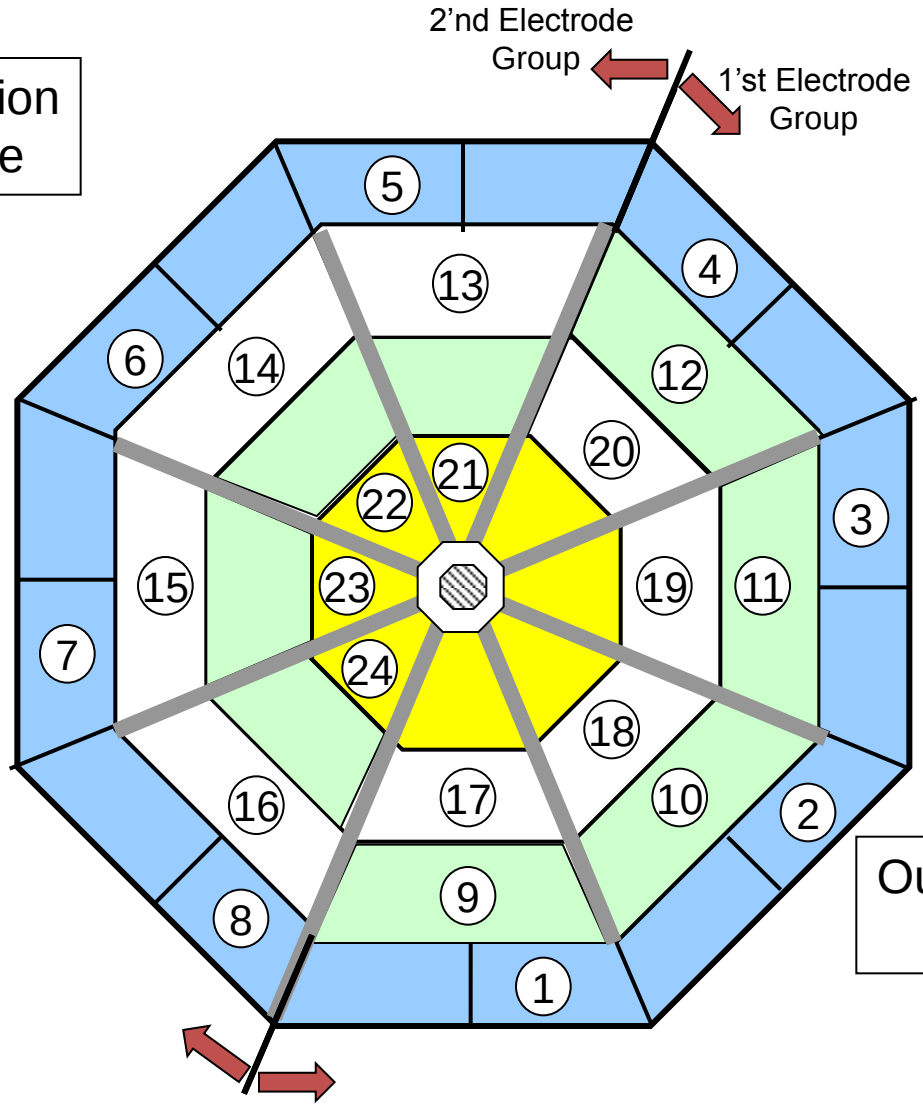
Charge collection of 22-th frame



Charge collection of 23-th frame

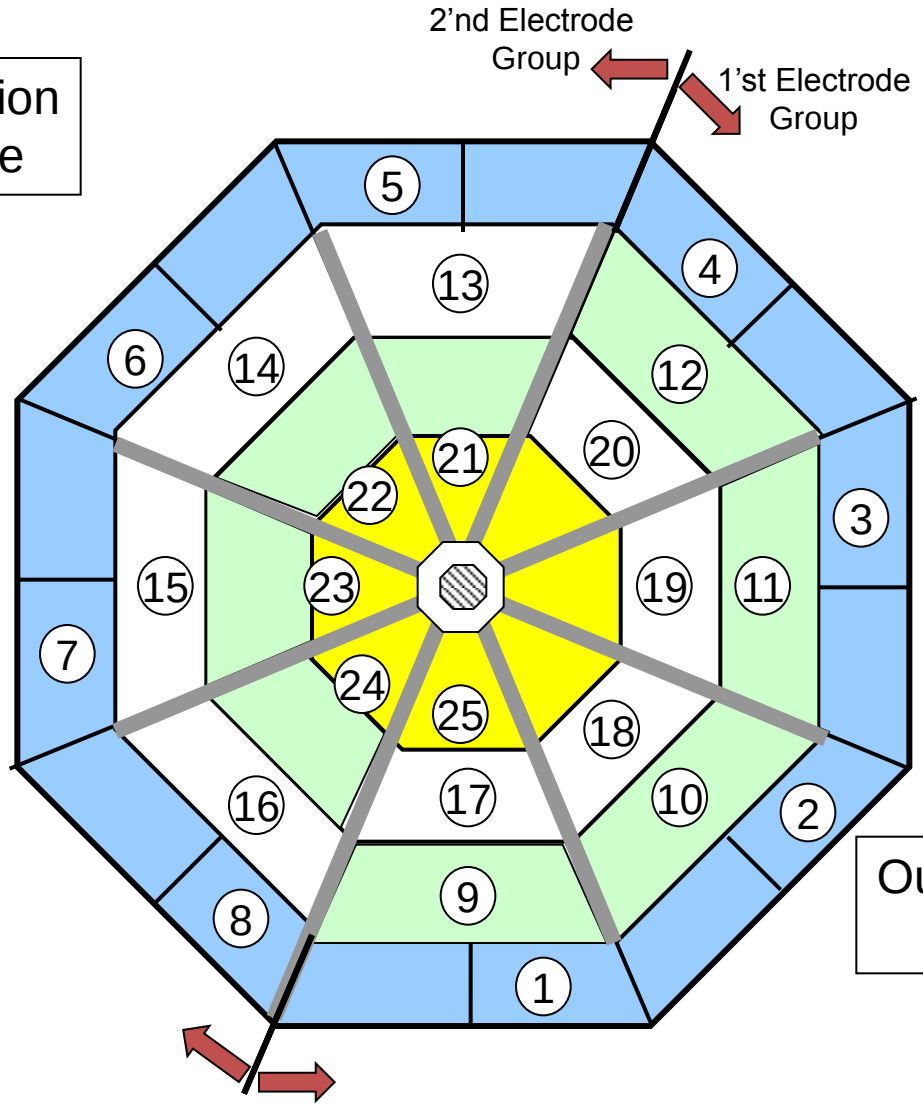


Charge collection of 24-th frame



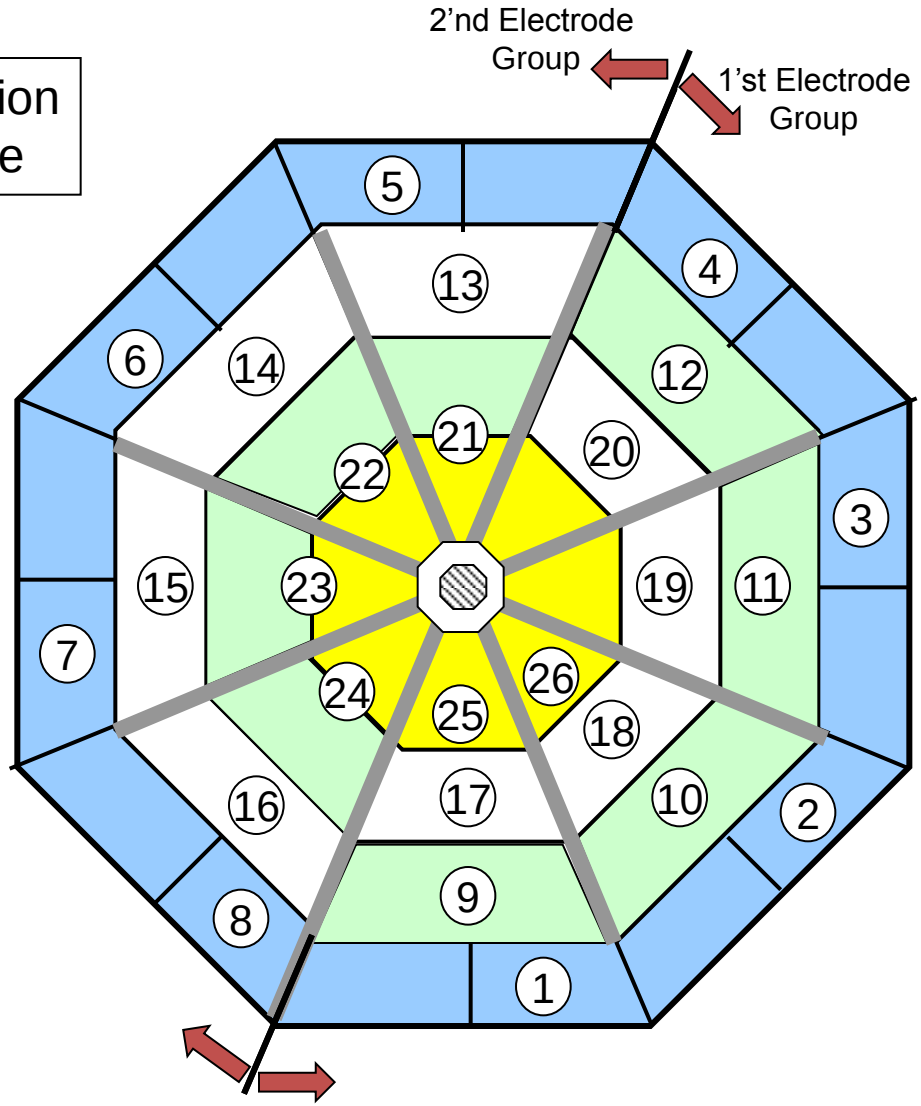
Outward transfer 5 → Finished

Charge collection of 25-th frame

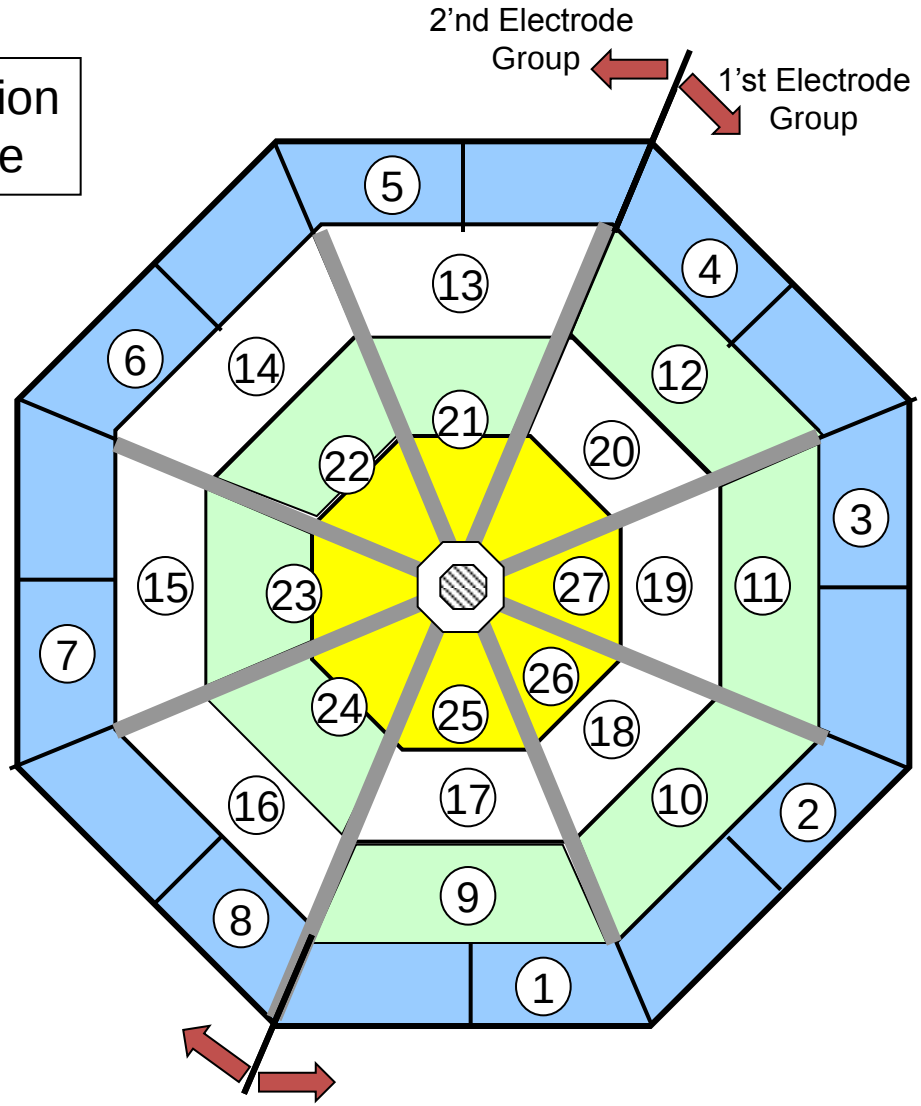


Outward transfer 6 → Started

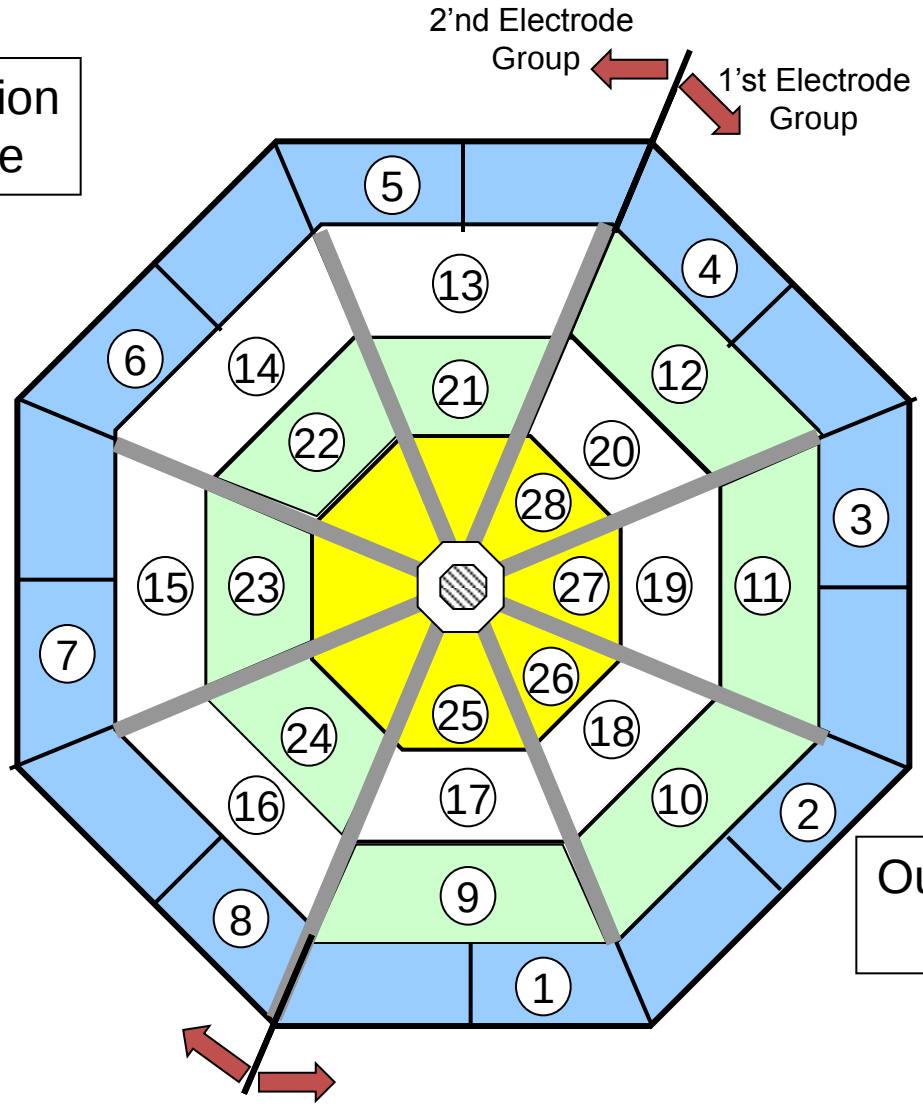
Charge collection of 26-th frame



Charge collection of 27-th frame

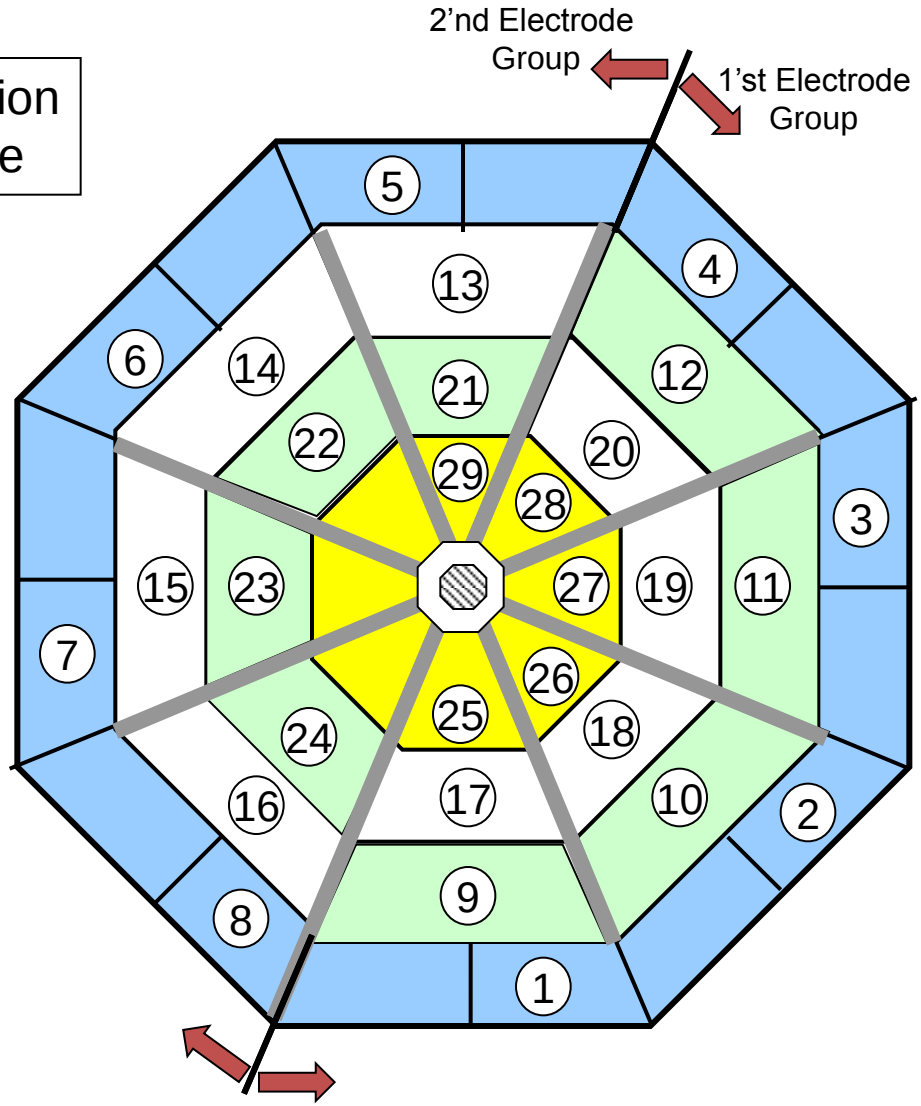


Charge collection of 28-th frame

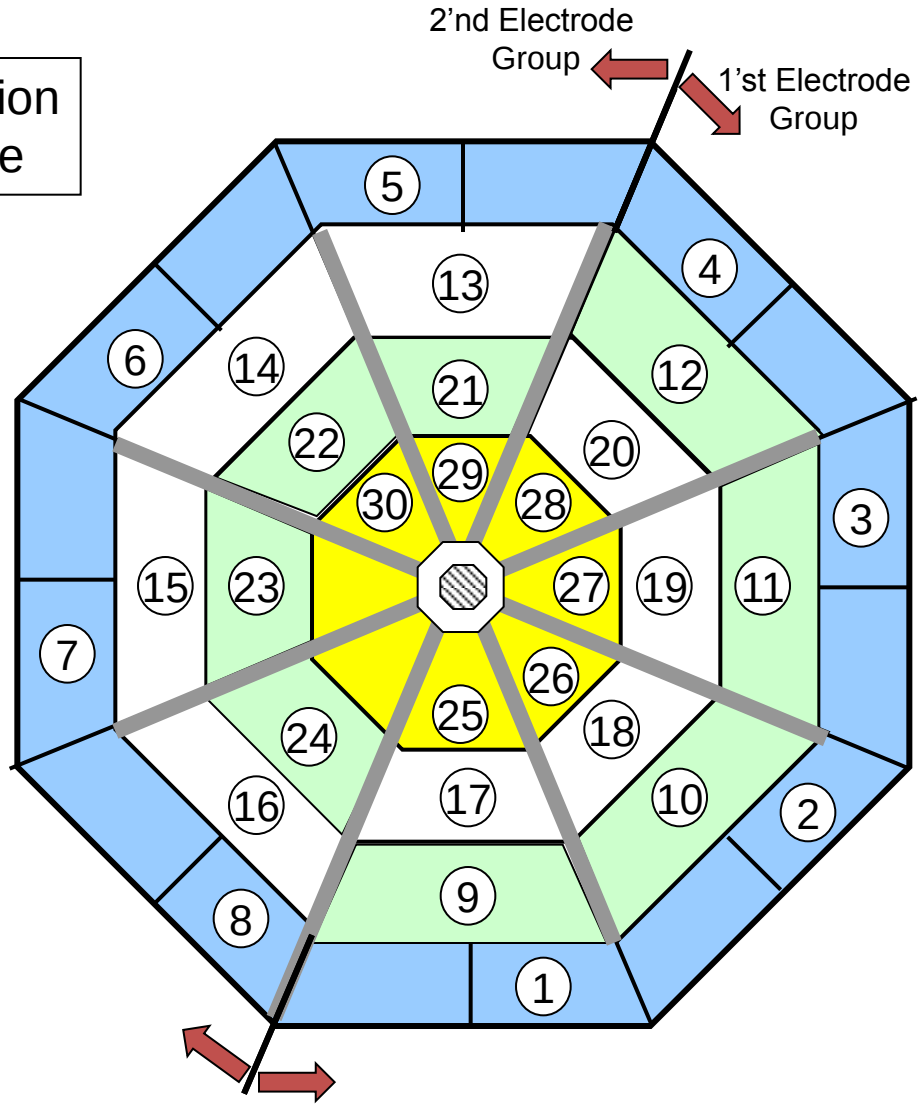


Outward transfer 6 → Finished

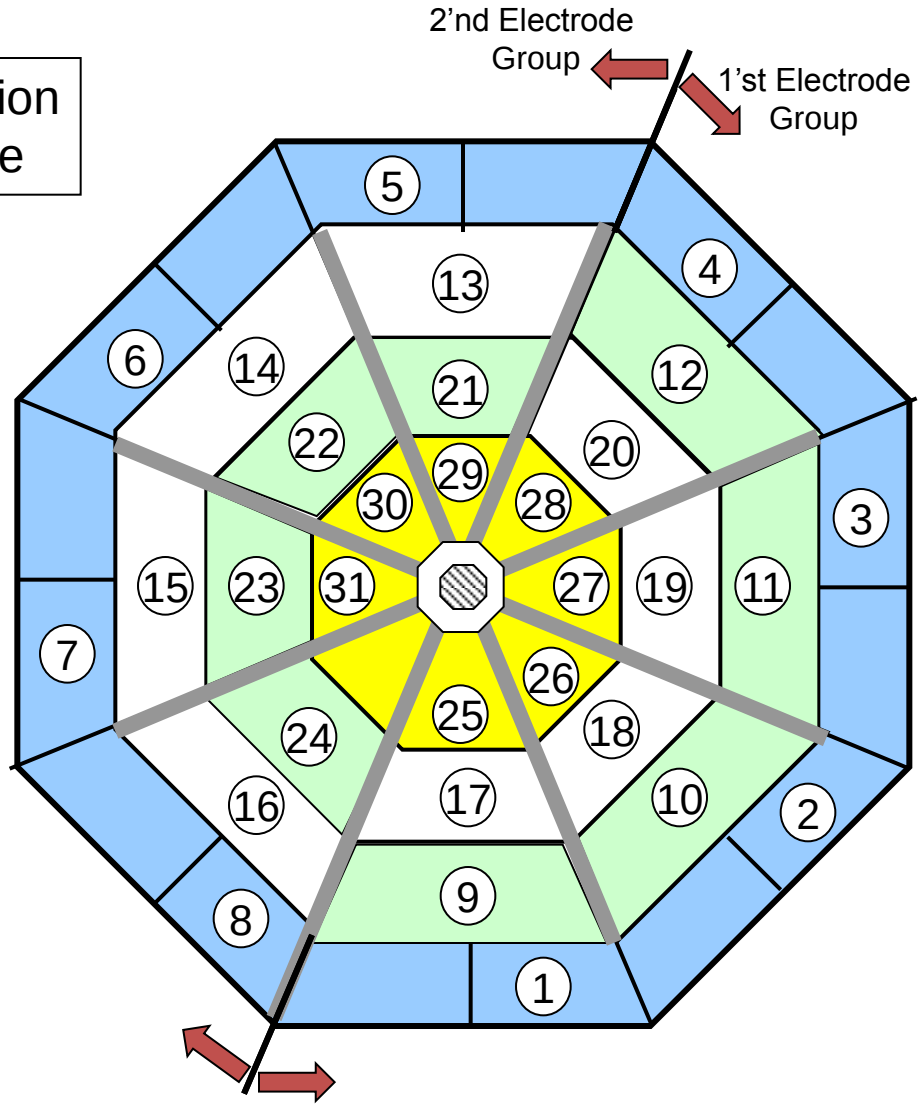
Charge collection of 29-th frame



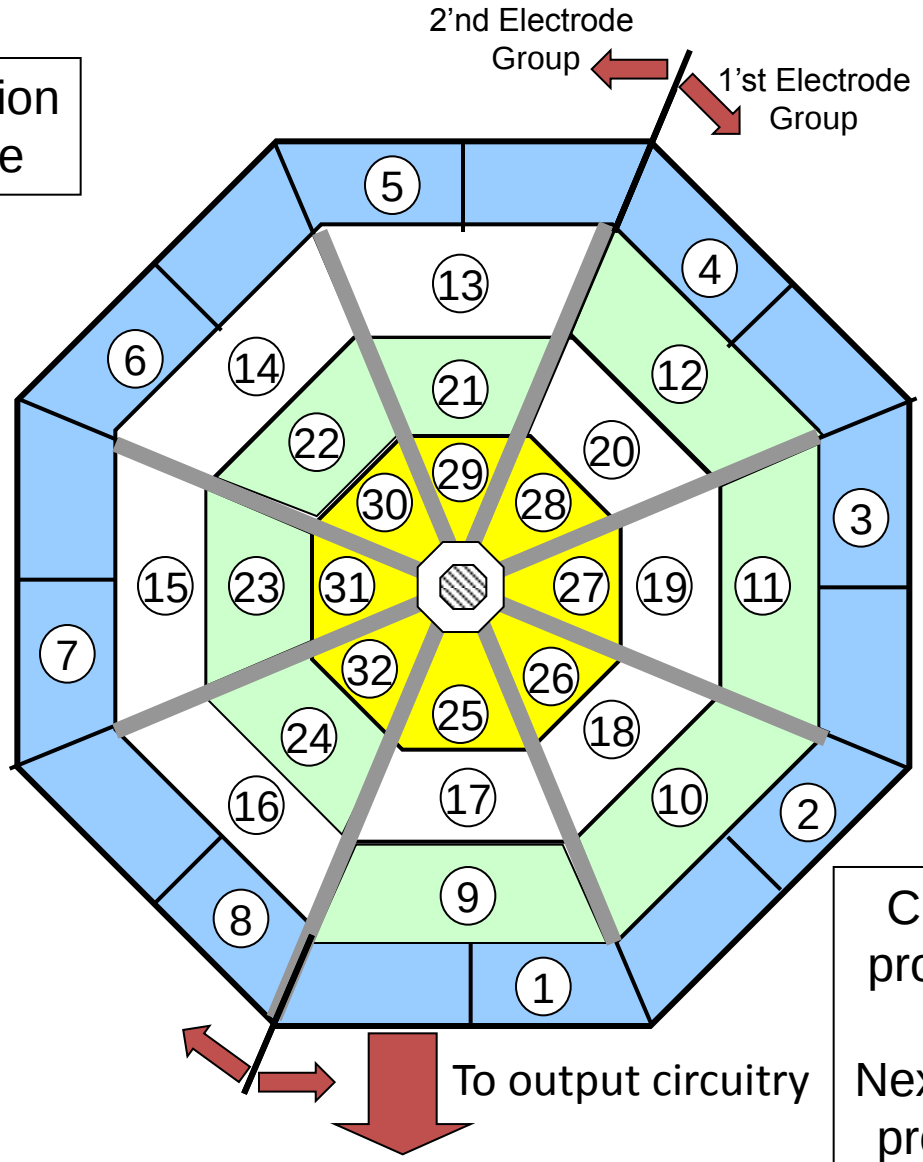
Charge collection of 30-th frame



Charge collection of 31-th frame

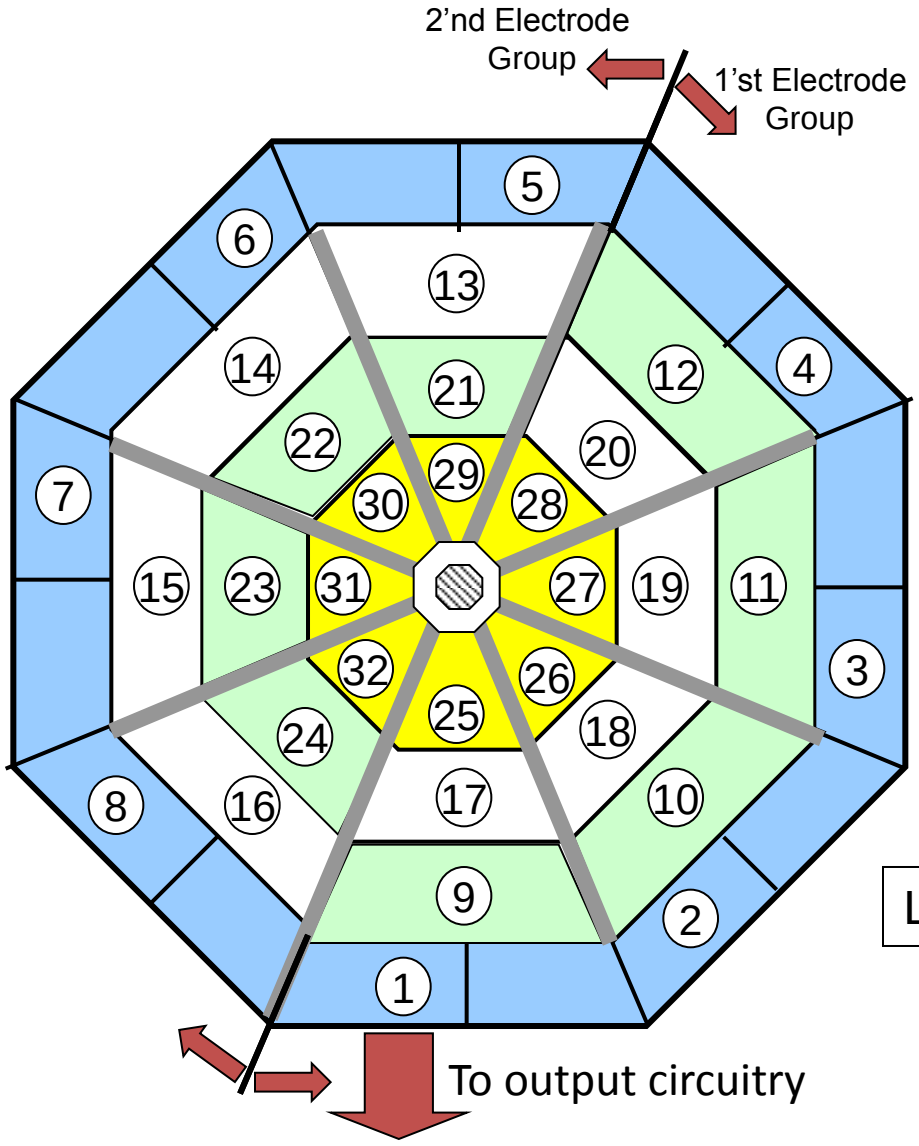


Charge collection of 32-th frame

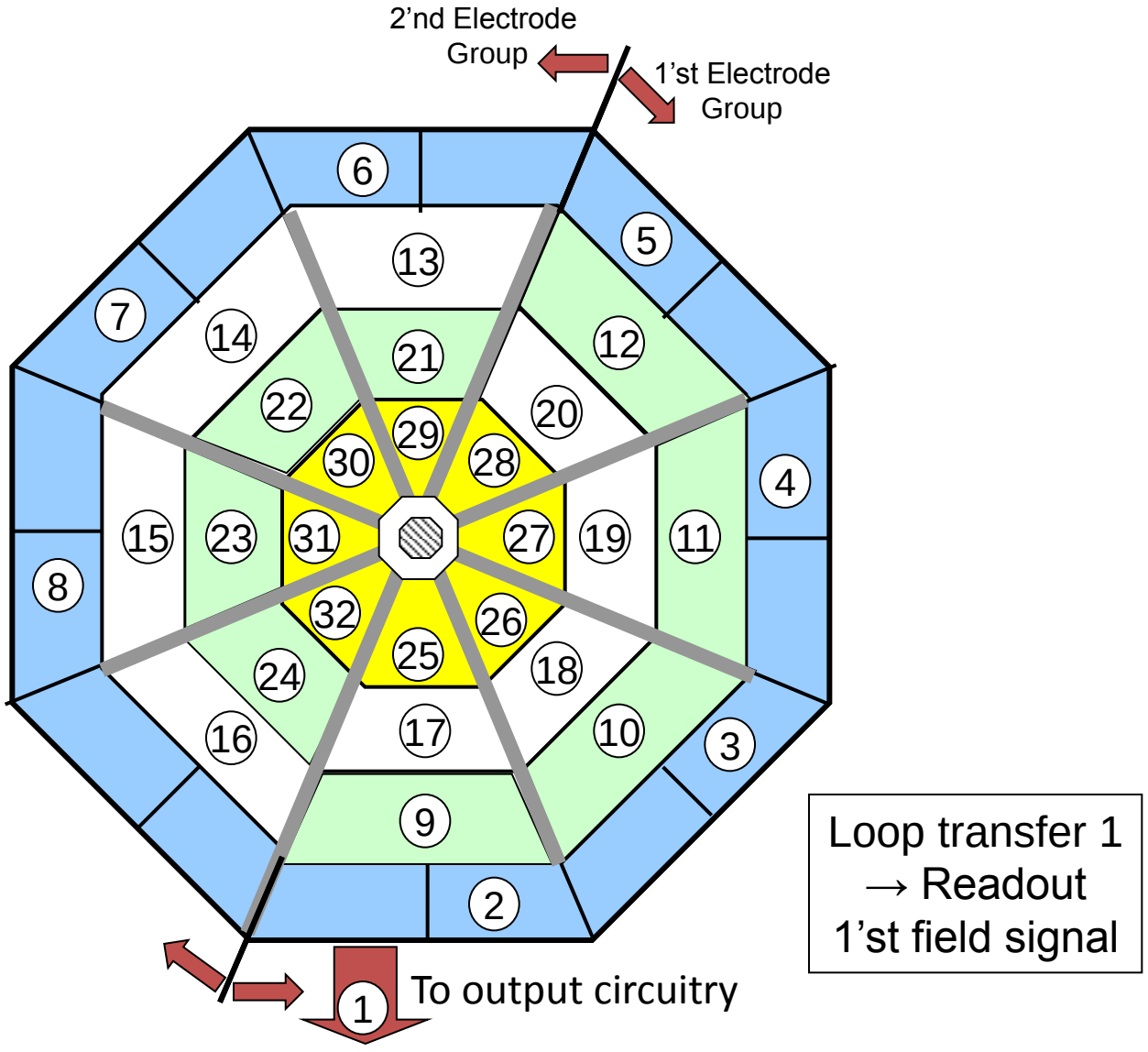


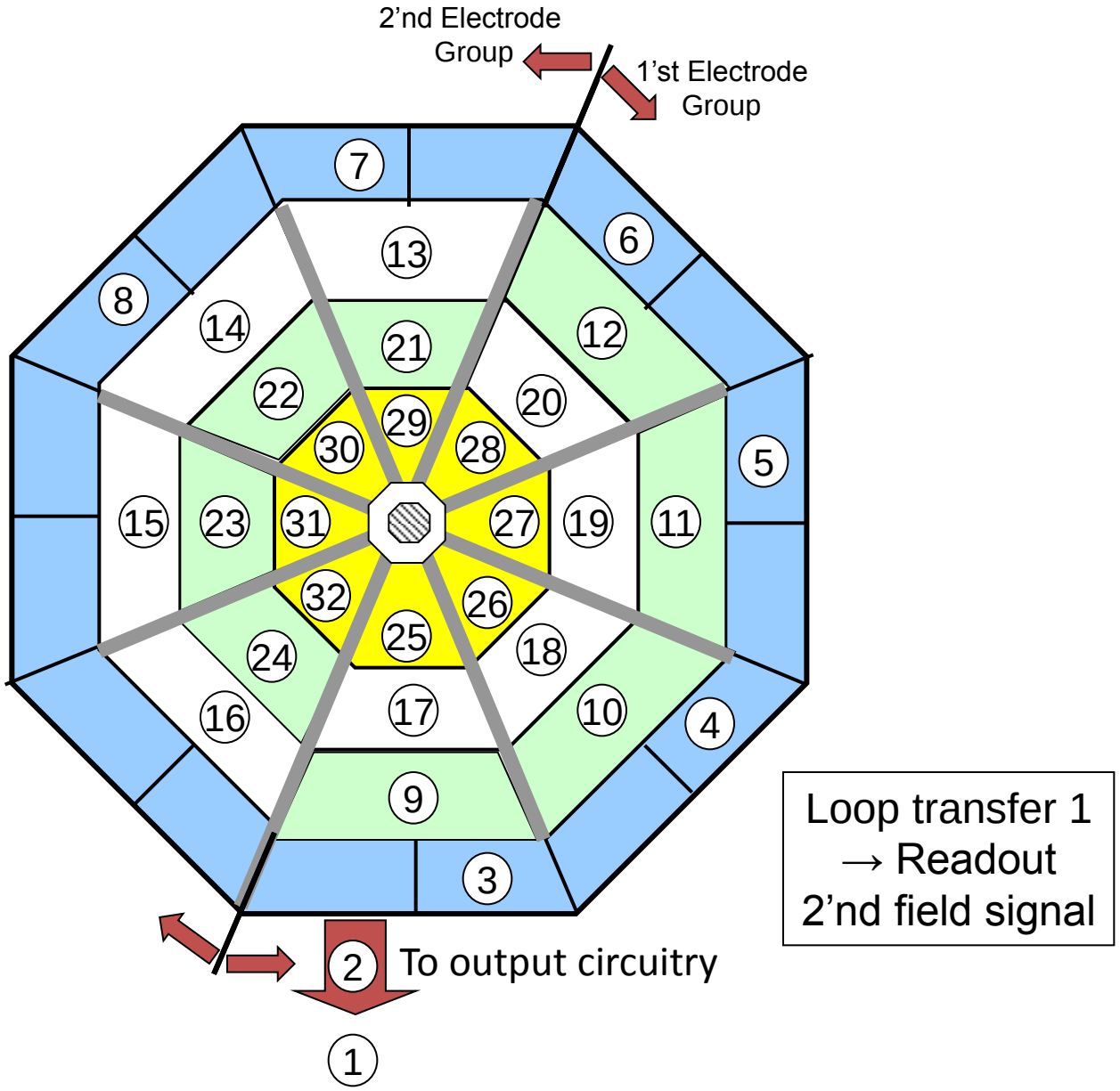
Charge collection process is finished.

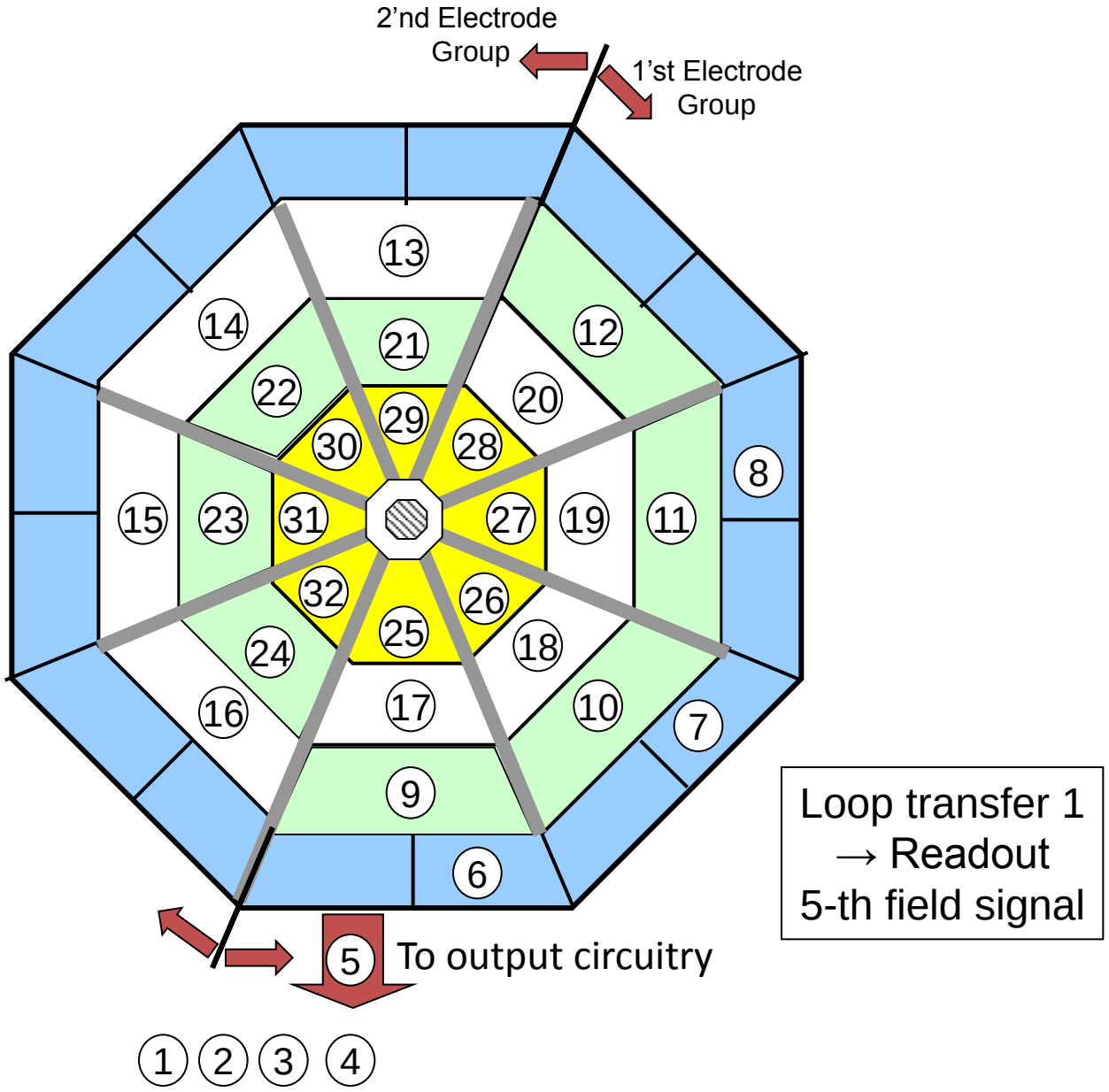
Next charge readout process is started.

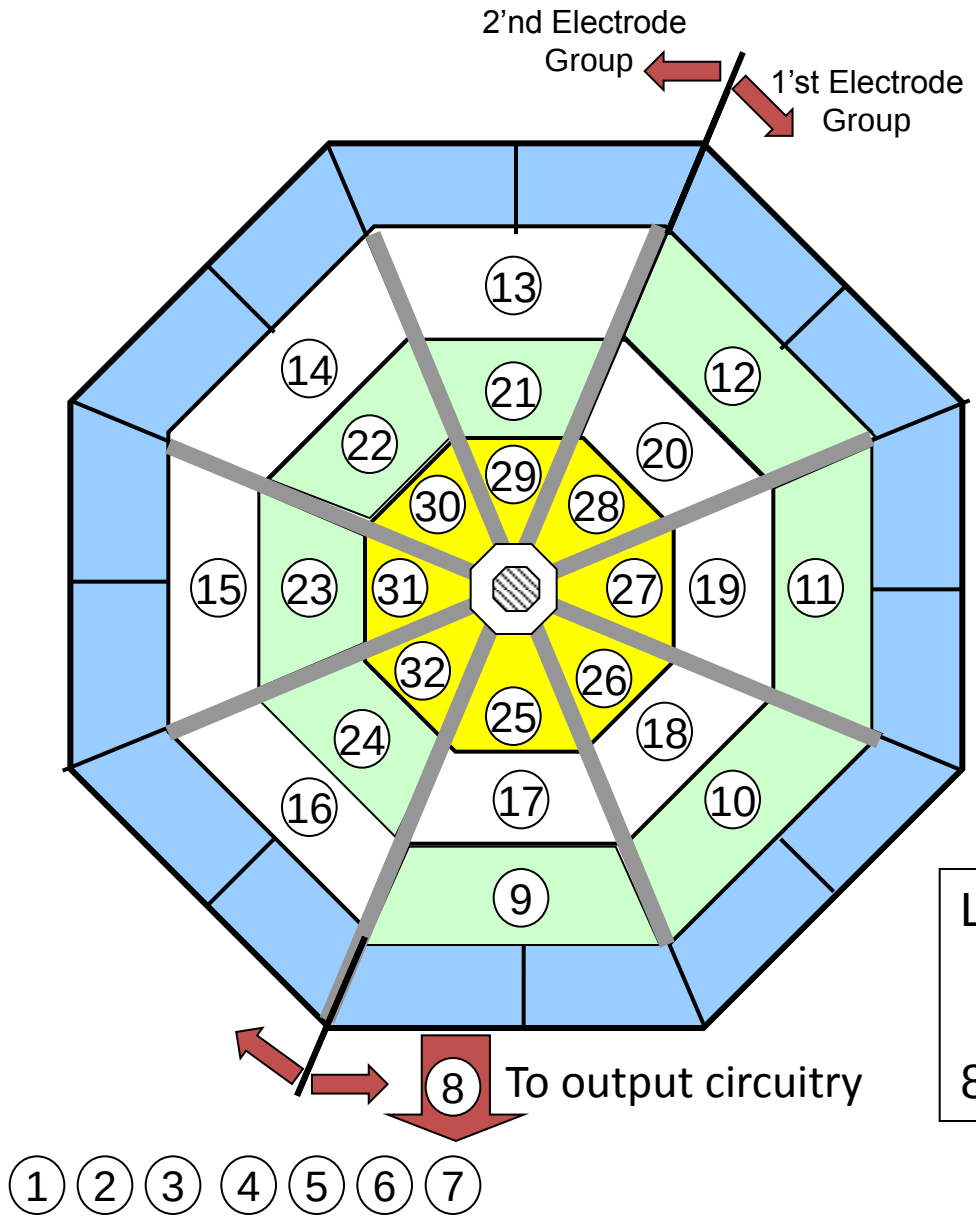


Loop transfer 1

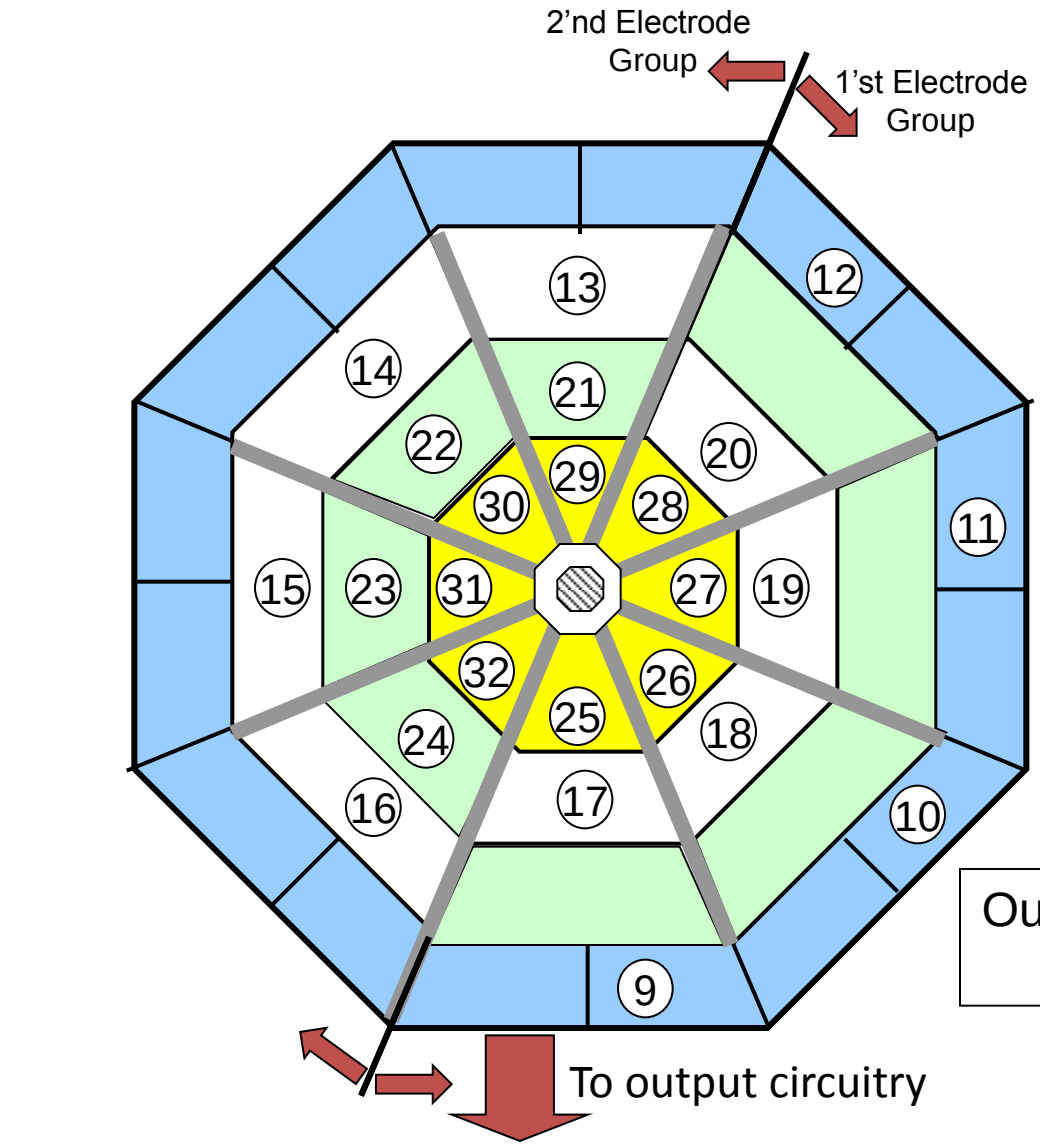

2’nd Electrode Group
1’st Electrode Group
6
5
13
7
14
21
12
22
20
29
30
28
4
15
23
31
27
19
11
8
32
26
25
24
18
16
17
10
3
9
2
1
To output circuitry
Loop transfer 1
→ Readout
1’st field signal


2’nd Electrode Group
1’st Electrode Group
7
13
6
8
14
21
12
22
20
29
30
28
5
15
23
31
27
19
11
32
26
25
24
18
16
17
10
4
9
3
2
To output circuitry
1
Loop transfer 1
→ Readout
2’nd field signal

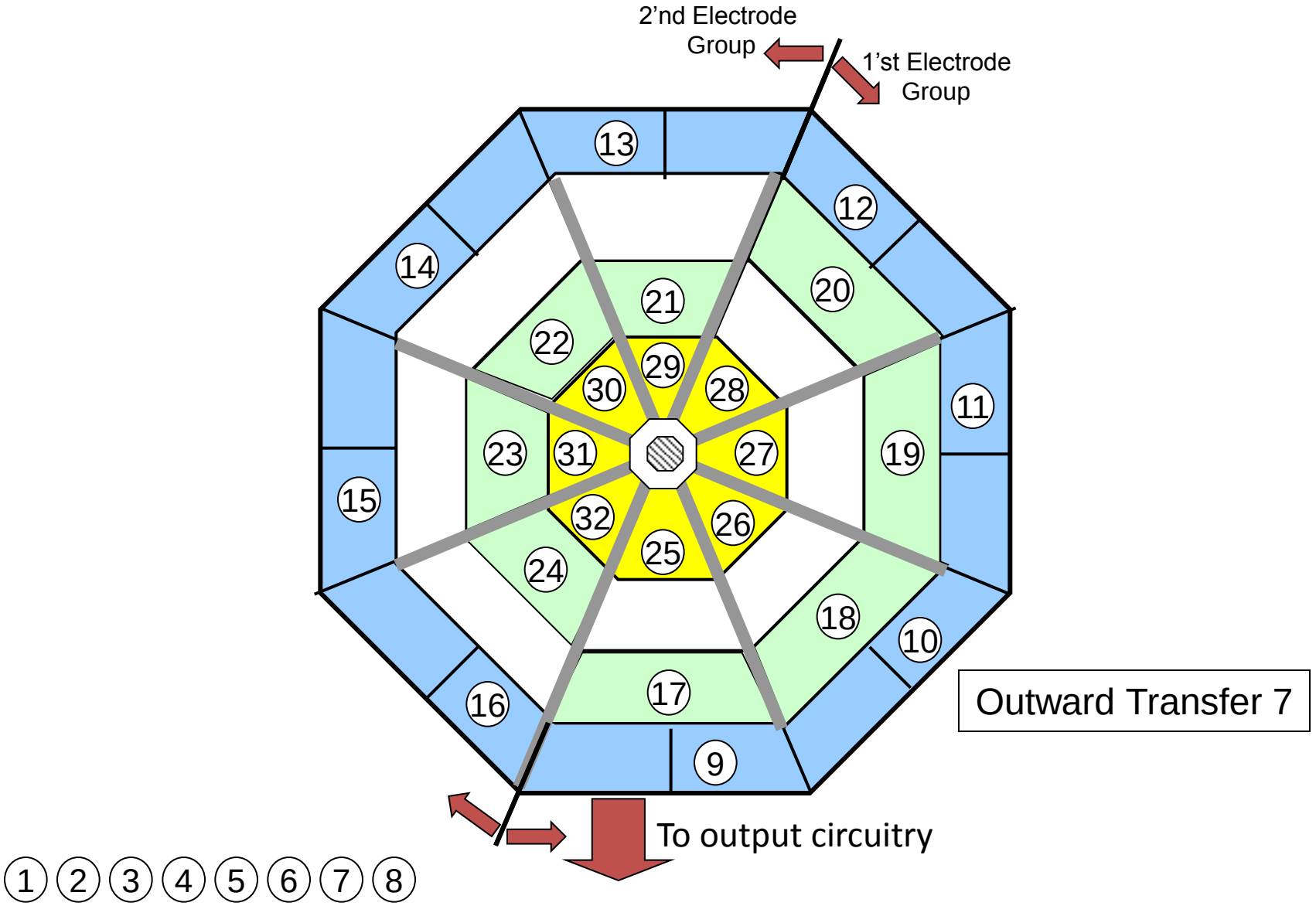

2’nd Electrode Group
1’st Electrode Group
13
14
21
12
22
20
29
30
28
8
15
23
31
27
19
11
32
26
25
24
18
16
17
10
7
9
6
5
To output circuitry
1
2
3
4
Loop transfer 1
→ Readout
5-th field signal

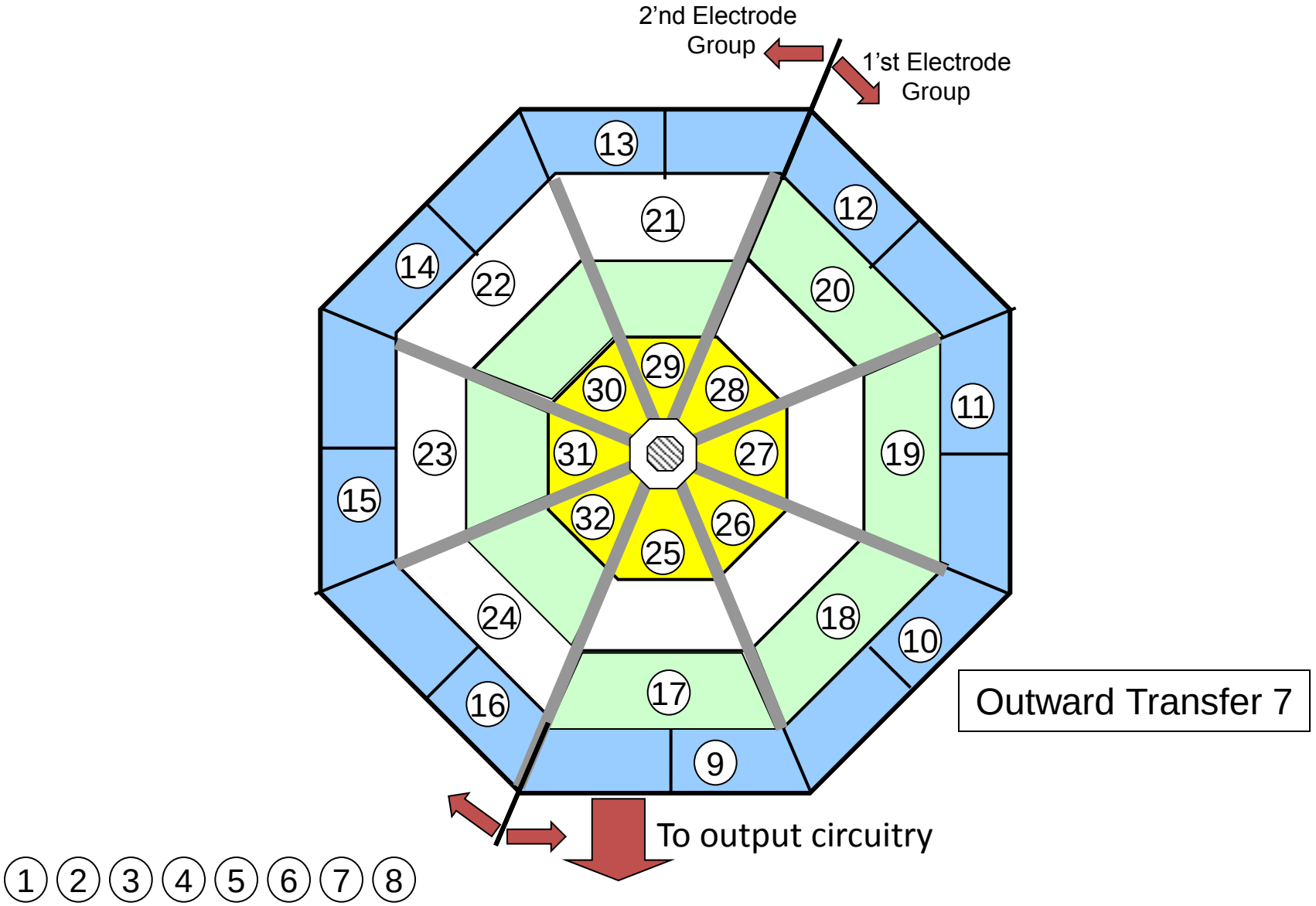


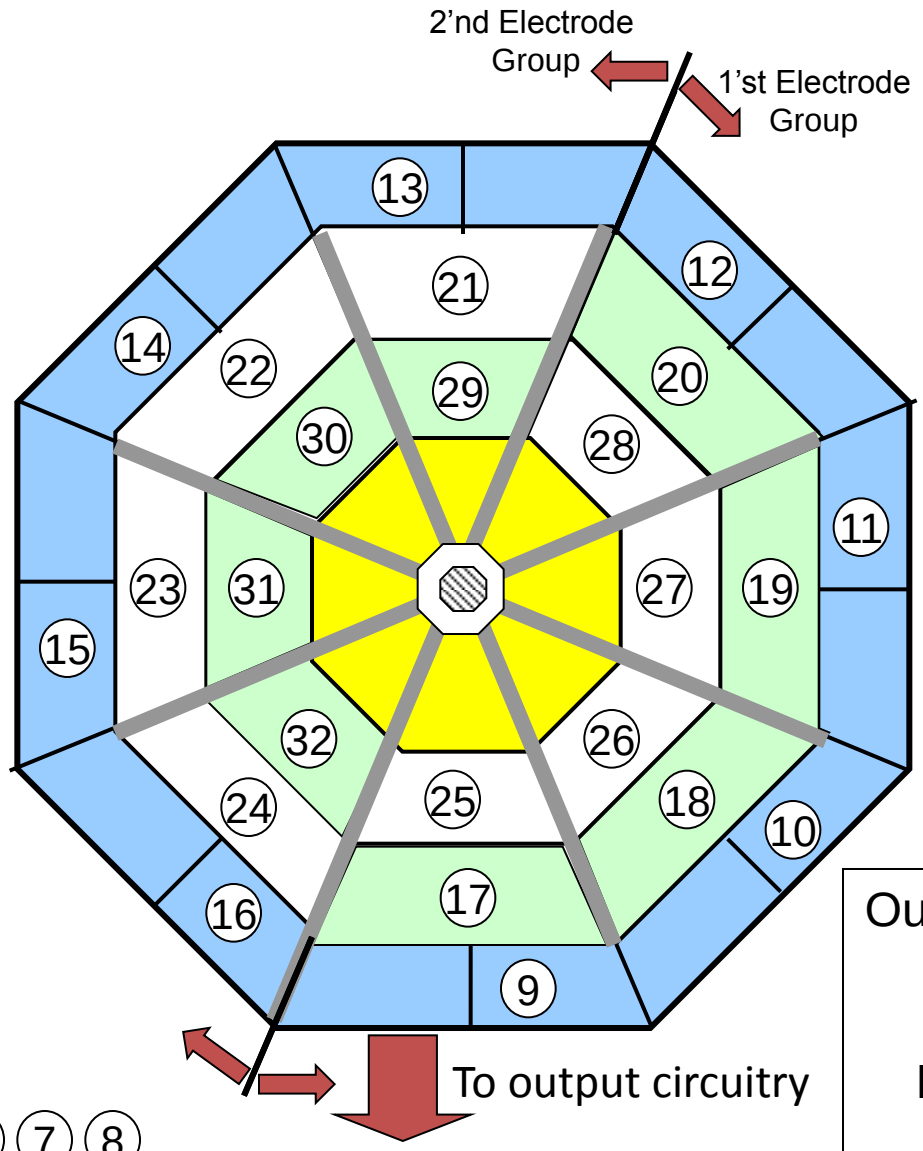
Loop transfer 1
is finished
→ Readout
8-th field signal



Outward Transfer 7 is started.


2’nd Electrode Group
1’st Electrode Group
13
12
14
20
21
22
29
30
28
11
23
31
27
19
15
32
26
25
24
18
10
17
16
9
To output circuitry
Outward Transfer 7
1
2
3
4
5
6
7
8

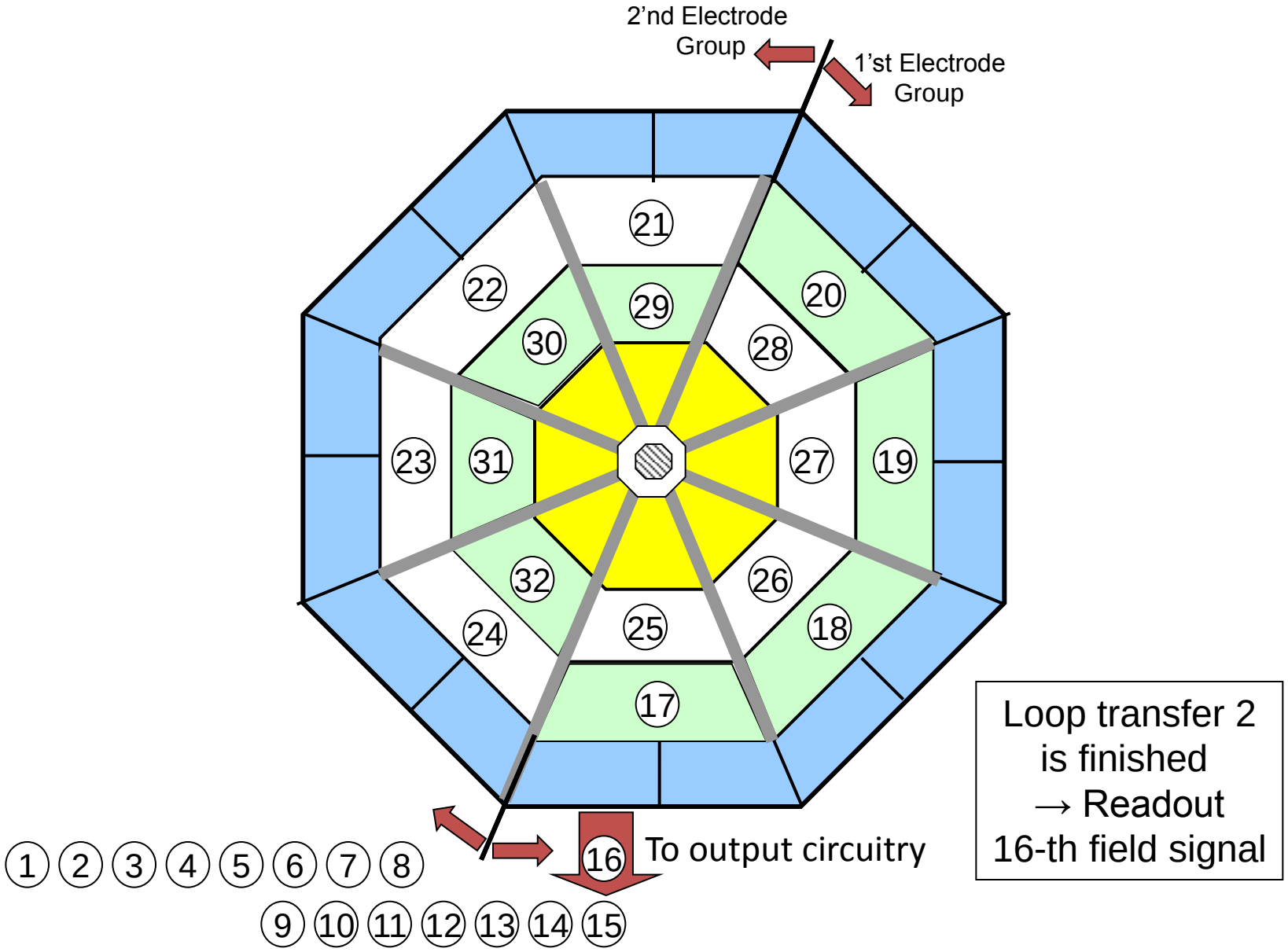

2’nd Electrode Group
1’st Electrode Group
13
12
21
14
22
20
29
30
28
11
23
31
27
19
15
32
26
25
24
18
10
17
16
9
To output circuitry
Outward Transfer 7
1
2
3
4
5
6
7
8

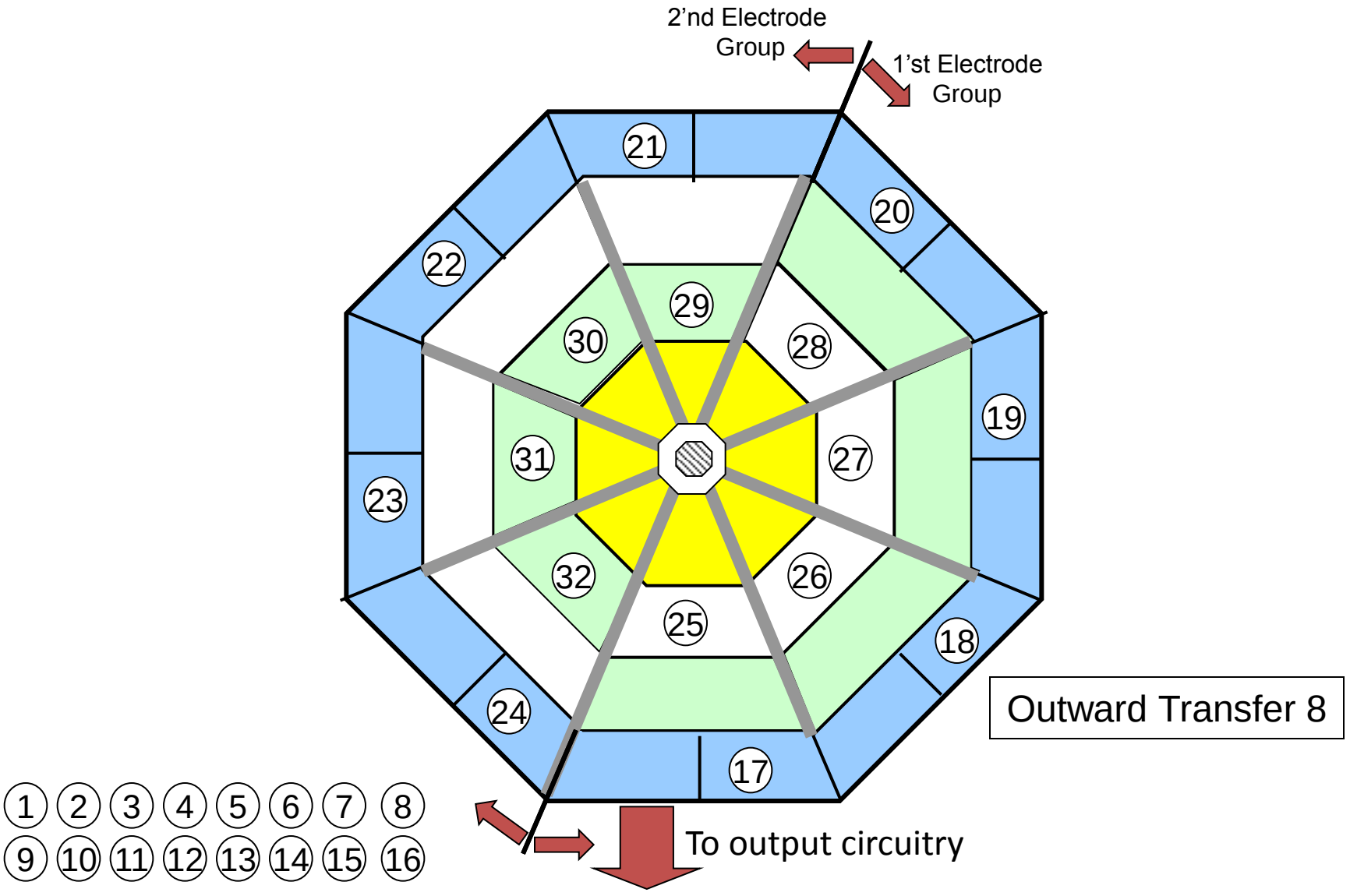


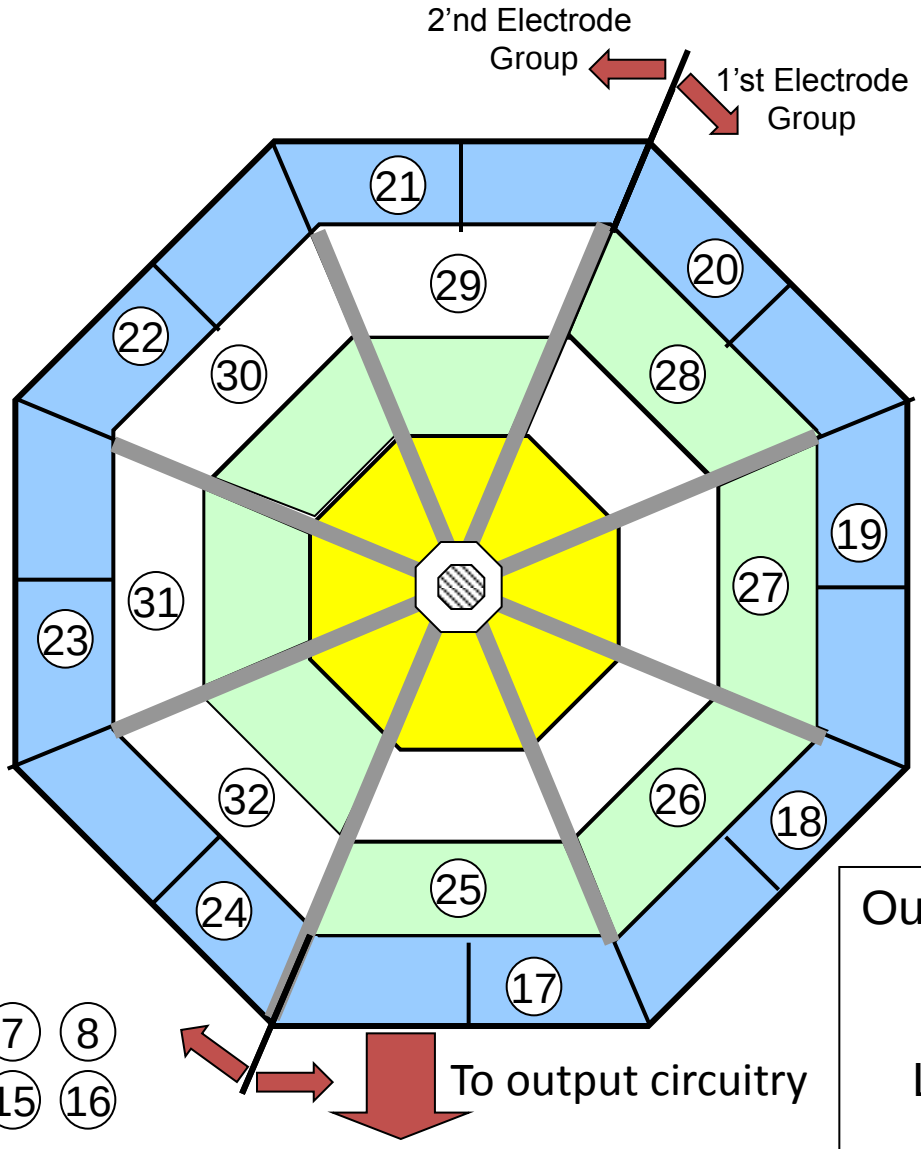
Outward Transfer 7 is finished.

Loop transfer 2 is started.

1 2 3 4 5 6 7 8


2’nd Electrode Group
1’st Electrode Group
21
22
29
20
30
28
23
31
27
19
32
26
24
25
18
17
16
To output circuitry
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
Loop transfer 2 is finished
→ Readout 16-th field signal

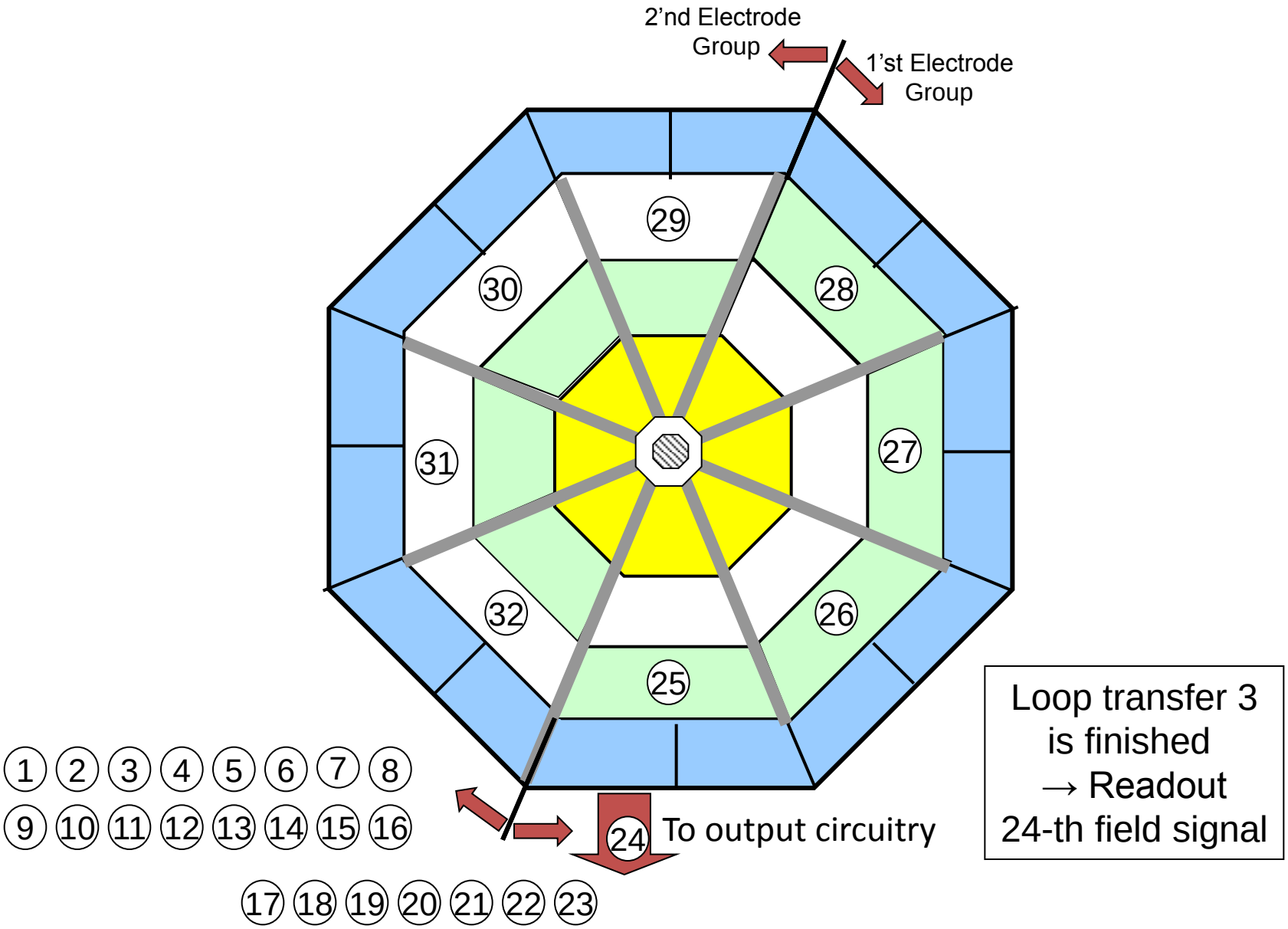

2’nd Electrode Group
1’st Electrode Group
21
20
22
29
30
28
19
31
27
23
32
26
25
18
24
17
To output circuitry
1 2 3 4 5 6 7 8
9 10 11 12 13 14 15 16
Outward Transfer 8

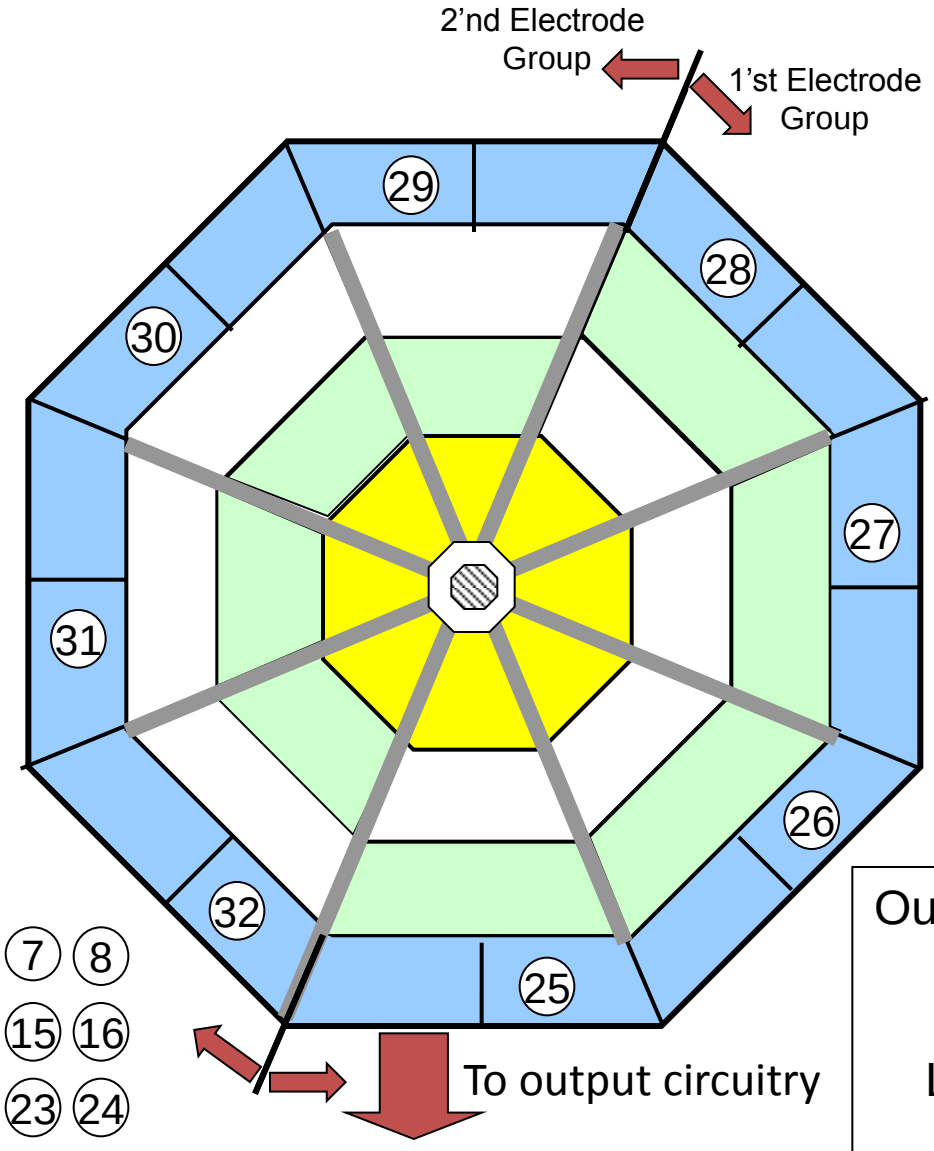


1 2 3 4 5 6 7 8
9 10 11 12 13 14 15 16

Outward Transfer 8 is finished.

Loop transfer 3 is started.

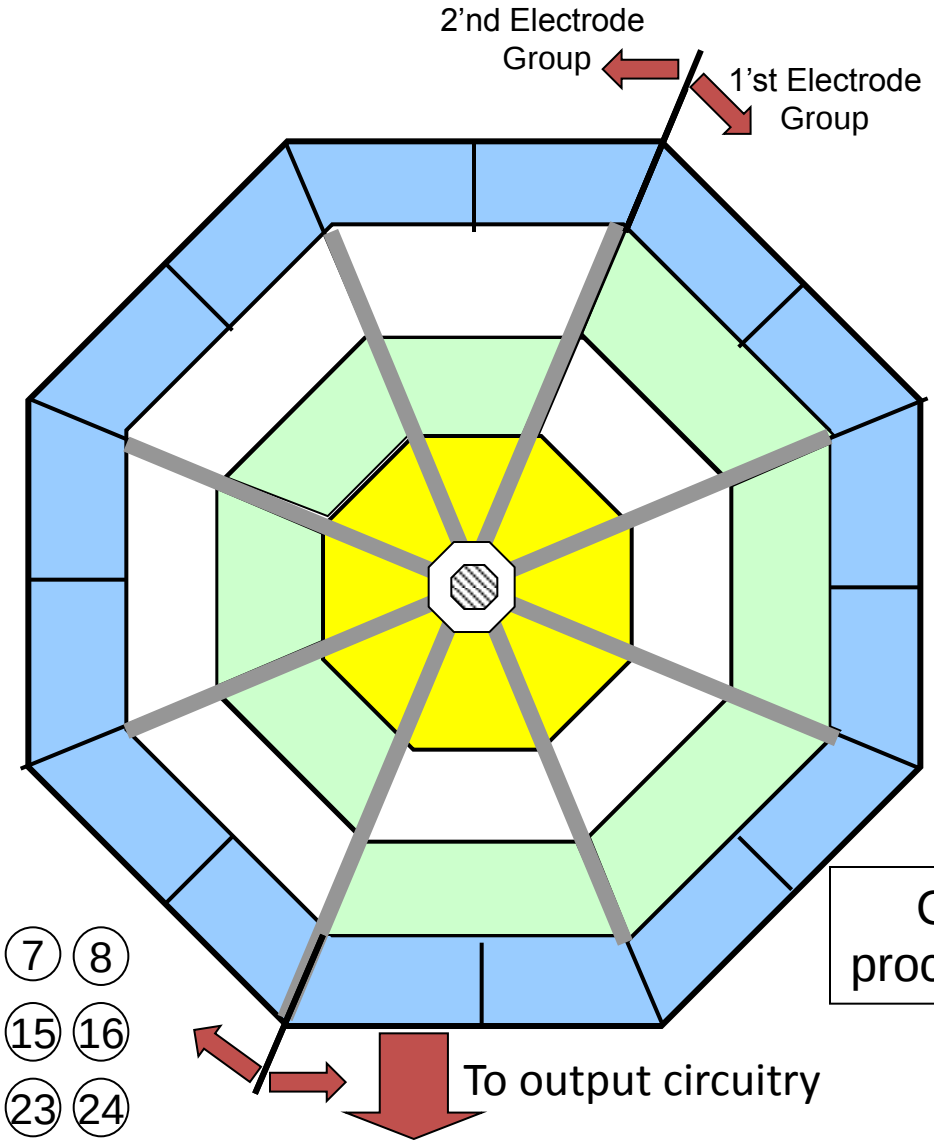

2’nd Electrode Group
1’st Electrode Group
29
30
28
31
27
32
26
25
24
To output circuitry
1 2 3 4 5 6 7 8
9 10 11 12 13 14 15 16
17 18 19 20 21 22 23
Loop transfer 3 is finished → Readout 24-th field signal



1 2 3 4 5 6 7 8
9 10 11 12 13 14 15 16
17 18 19 20 21 22 23 24

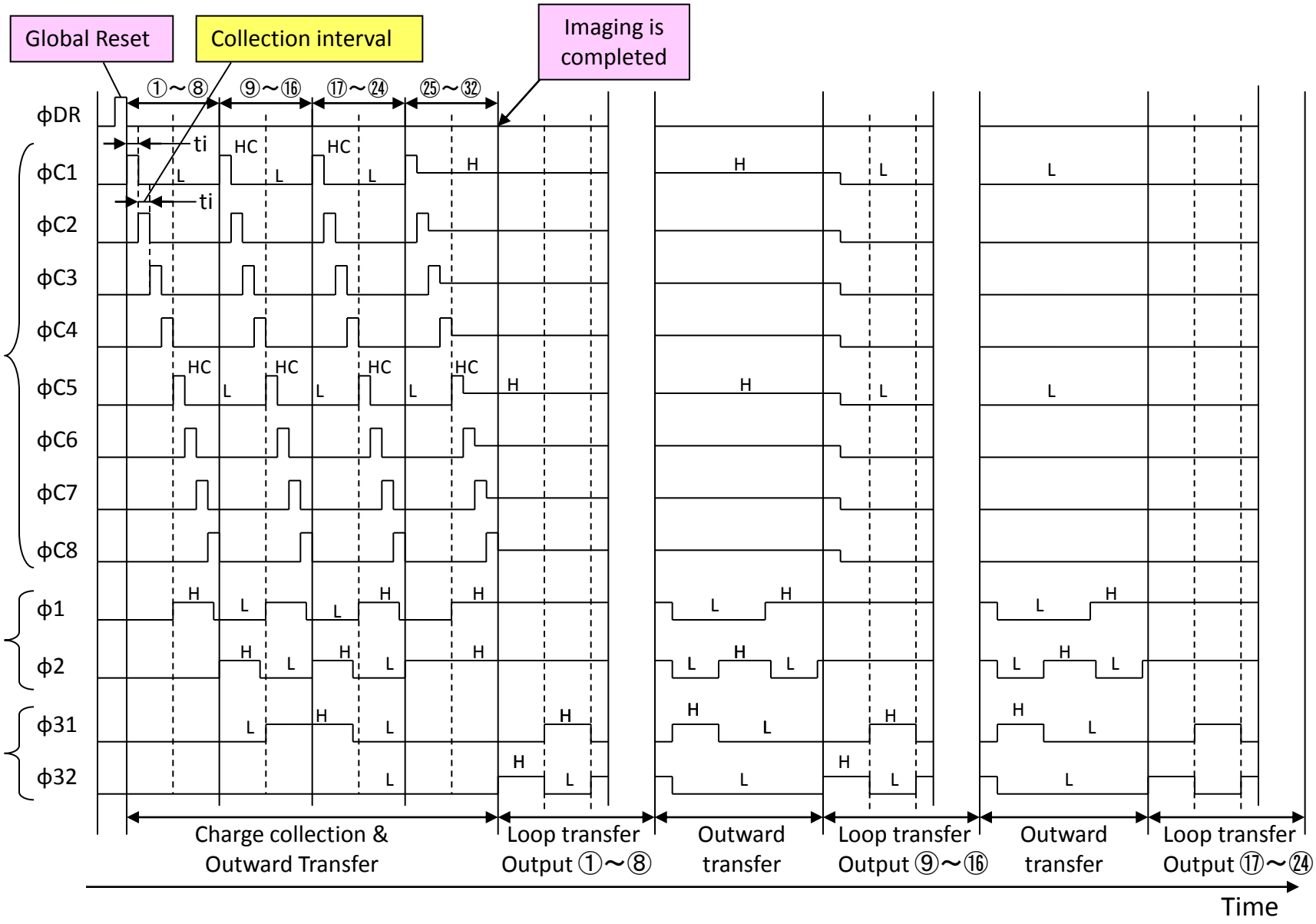
Outward Transfer 9 is finished.

Loop transfer 4 is started.

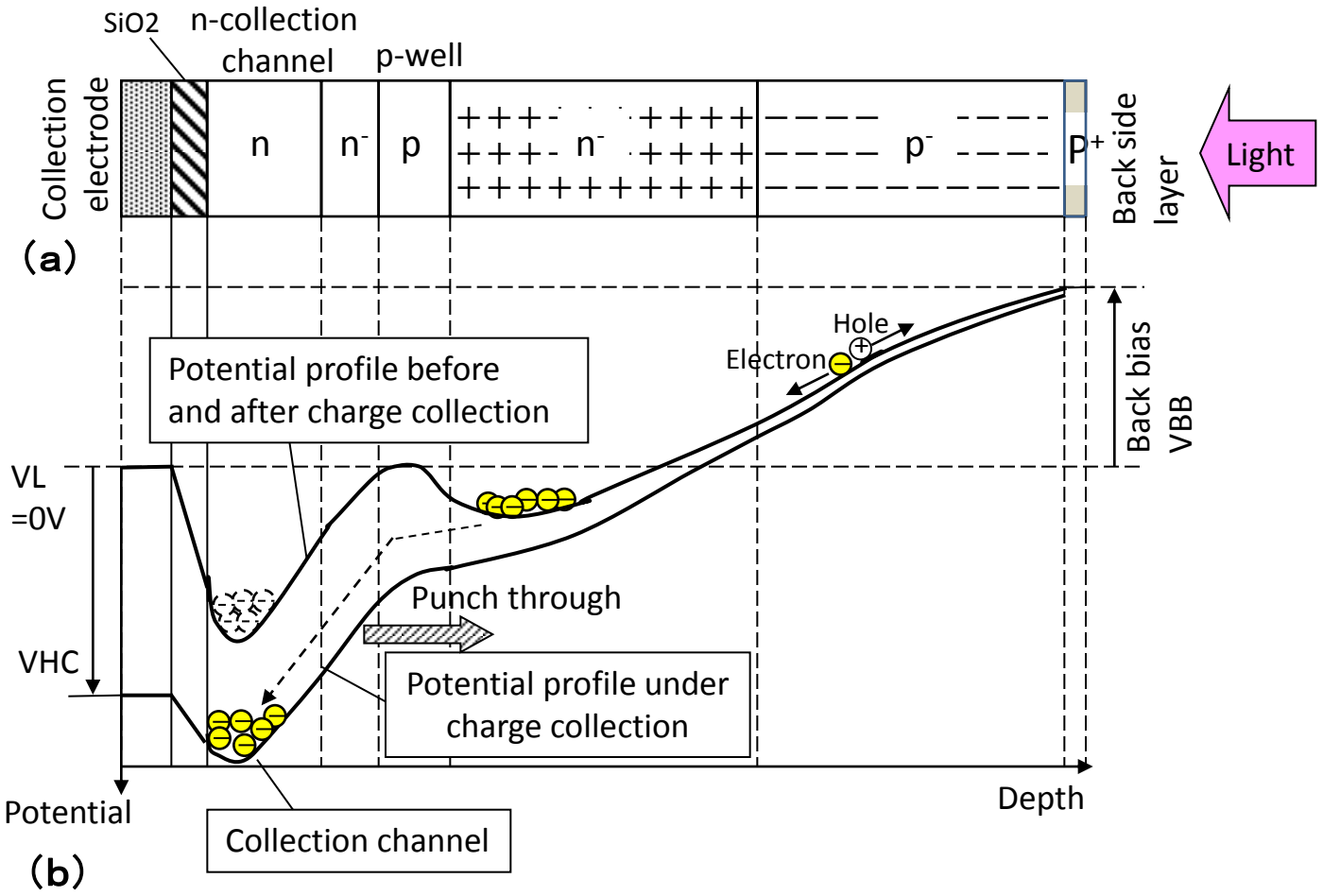


Charge readout process is completed.

1 2 3 4 5 6 7 8
9 10 11 12 13 14 15 16
17 18 19 20 21 22 23 24
25 26 27 28 29 30 31 32



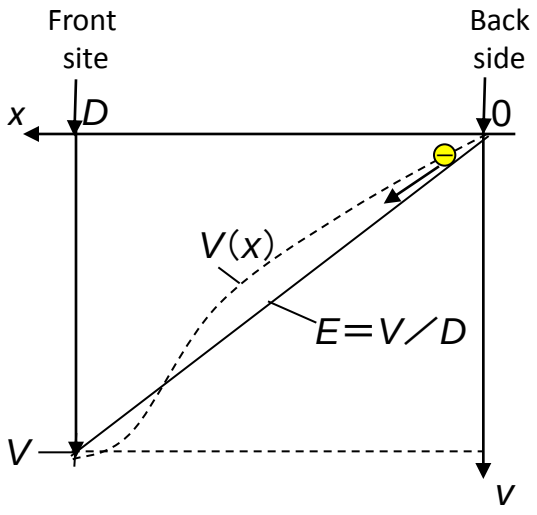
Timing Chart of New Pixel Clocking



Charge Collection Mechanism

（a）One Dimensional Si-Bulk Structure,（b）Potential Profile

Frame Rate Limitation



Electron travel time t_c from back side to front side (charge collection site) through distance D is given by

$$t_c = \int_0^D 1 / \mu E(x)\, dx, \qquad (1)$$

where $E(x)$ is an electric field in a Si bulk, μ is electron mobility in the bulk.
If the electric field $E(x)$ is ideally constant as $E = V / D$,

$$t_c = D / \mu E = D^2 / \mu V, \qquad (2)$$

where V is the potential difference between the back side and the front side.
t_c will be a criterion of the minimum charge collection time which is roughly the minimum frame interval t_i.

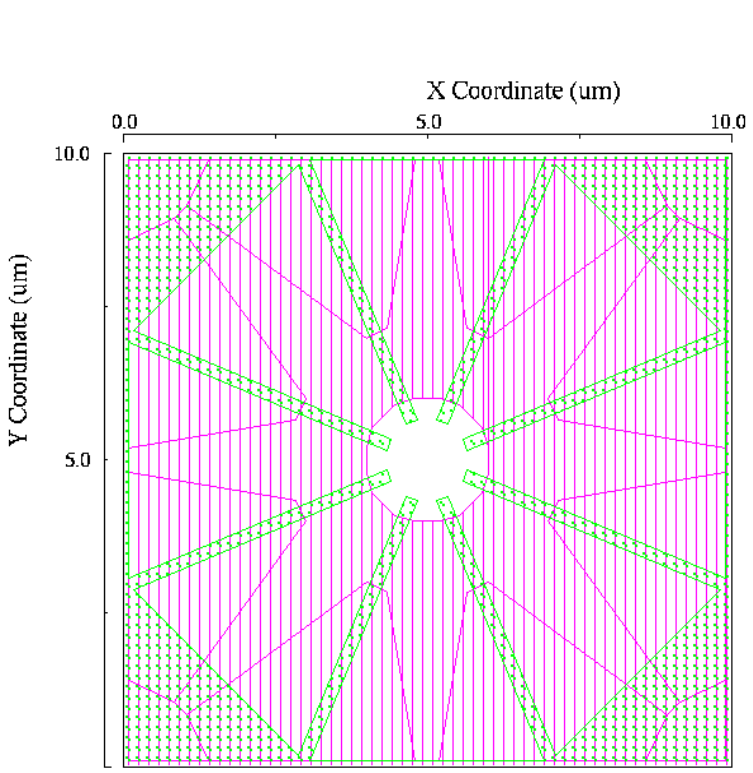
Practical examples

Case 1. μ＝1350 [cm²/Vsec],
D＝30 [μm], V＝10 [V]
→ $t_i \fallingdotseq 6.7 \times 10^{-10}$ (sec) corresponds 1.5 Gfps.

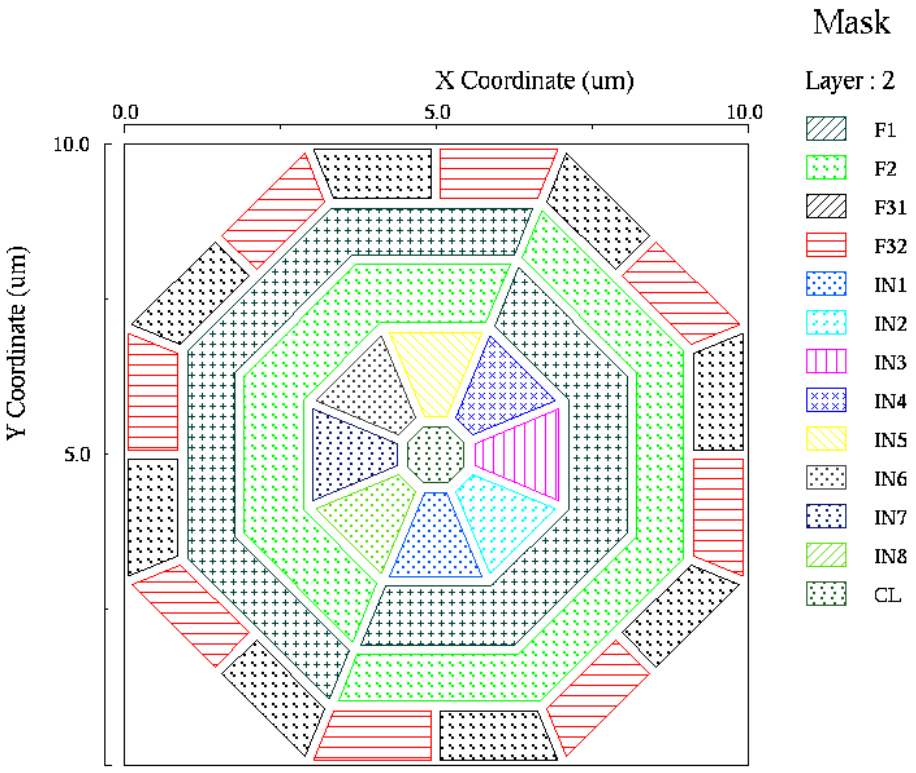
Case 2. D＝50 [μm], V＝30 [V]
→ $t_i \fallingdotseq 6.2 \times 10^{-10}$ (sec) corresponds 1.6 Gfps

Actually, the high speed limitation will be near 1Gfps.

A Proposed Pixel Pattern Layout for 3-Dimentional Simulation



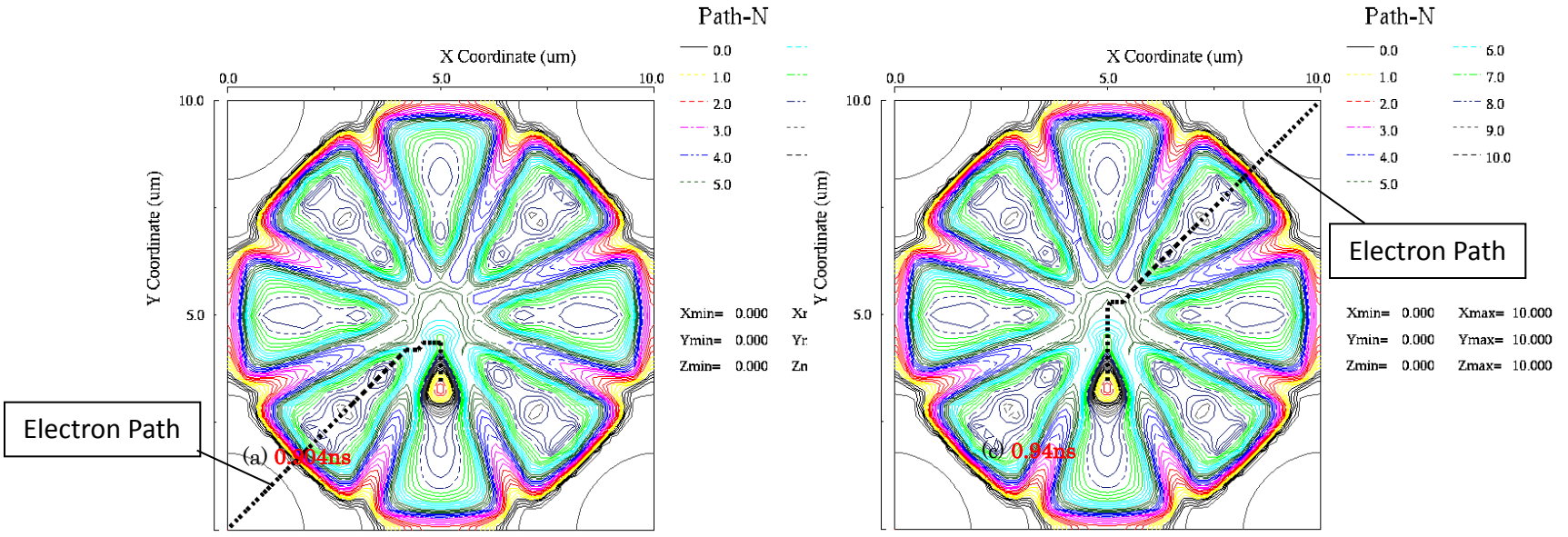
(a) Si Bulk



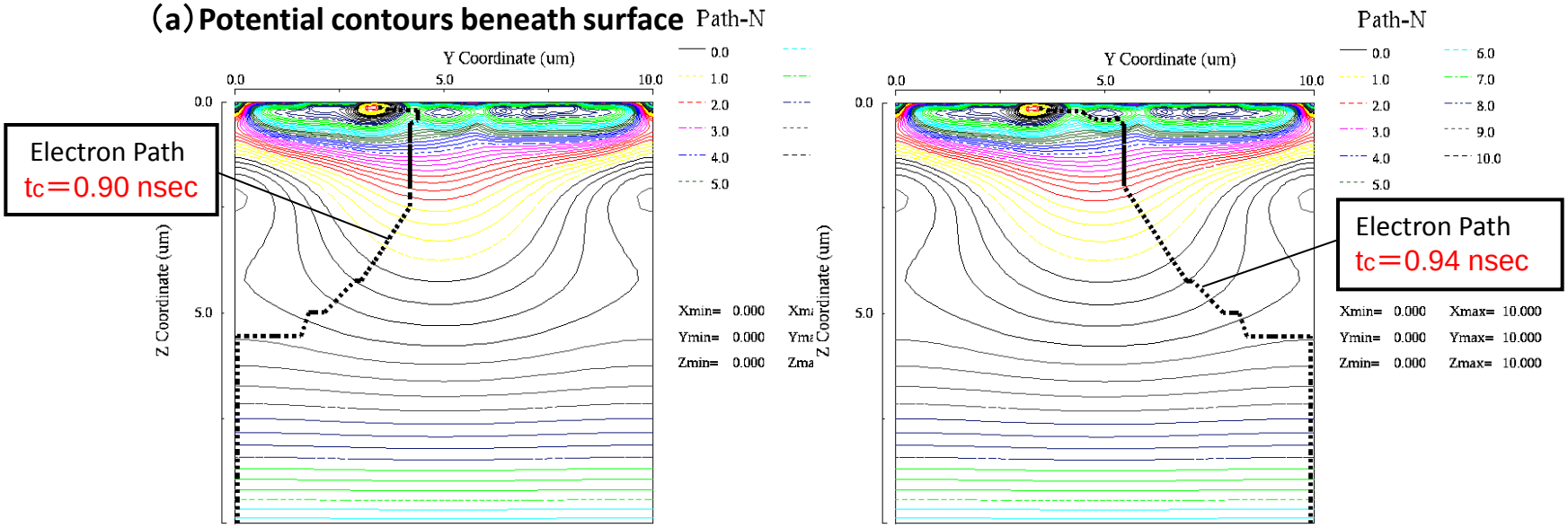
(b) Electrodes

Fig 1. Mask data: (a) Channel stop and p-well; (b) Poly-Si electrodes.
Voltage condition (with respect to p-well voltage):
-VIN1 = +10V
-VIN2 = VIN3 = ... = VIN8 = +2V
-VF1 = VF2 =VF31 = VF32 = -2V
-VCL = -10V
-VBACK = -25V

3-Dimensional Simulation Results for Charge Collection



(a) Potential contours beneath surface



(b) Potential contours in cross section

Summary

- New pixel architecture of the in-pixel multi-collection gates has been introduced to achieve 1Gfps imaging.
  The key technologies are followings.

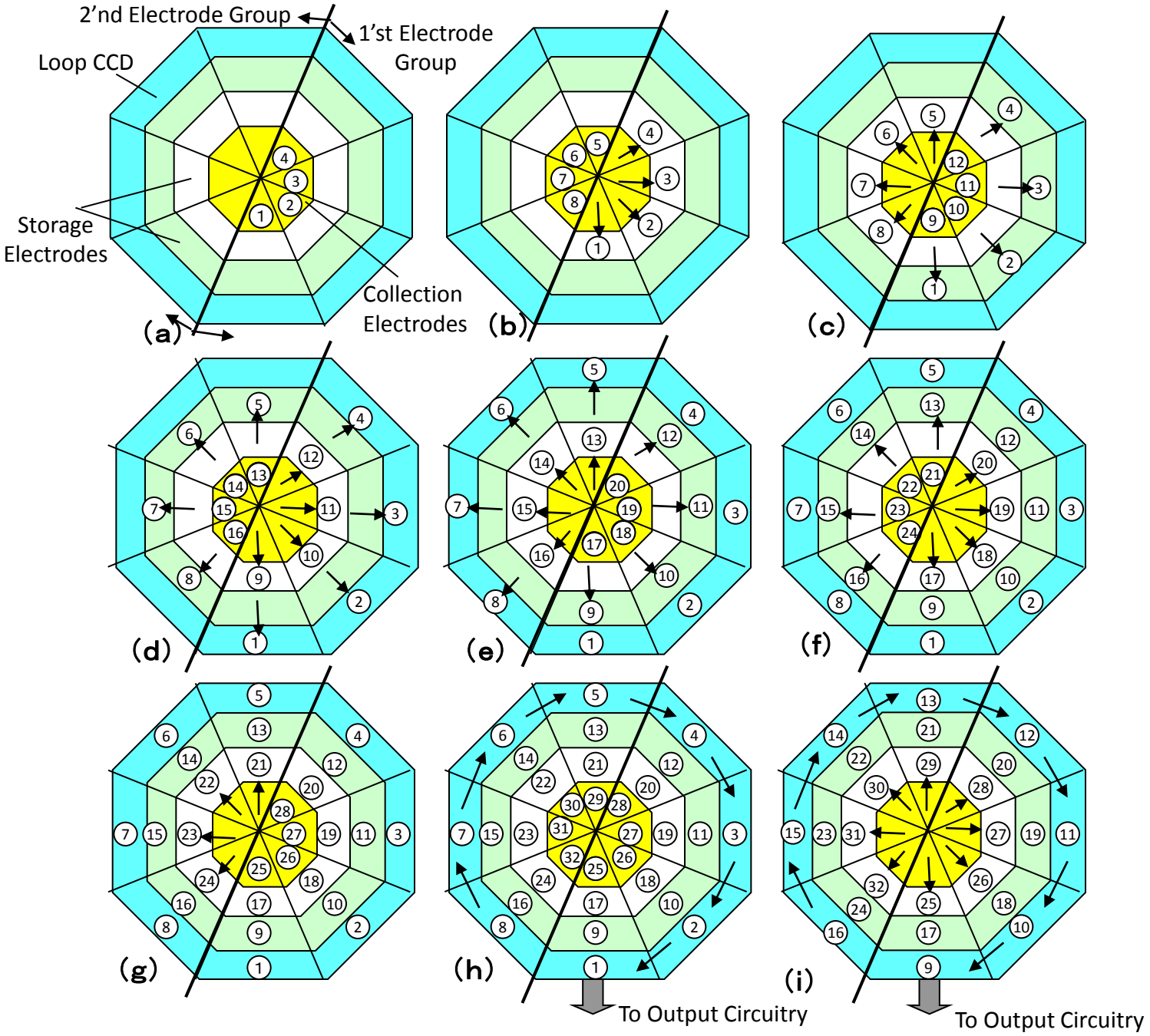
  (1) Plural collection electrodes are composed in a pixel.
  It makes possible that the frame rate is determined only by the charge collection time.

  (2) All of collection electrodes are sited on the central region in the pixel.
  It can optimize potential profile to gather all photoelectrons quickly, and heightens the frame rate.

- Simulation results mean that the maximum frame rate can achieve theoretically to 1Gfps with using the proposed technology.

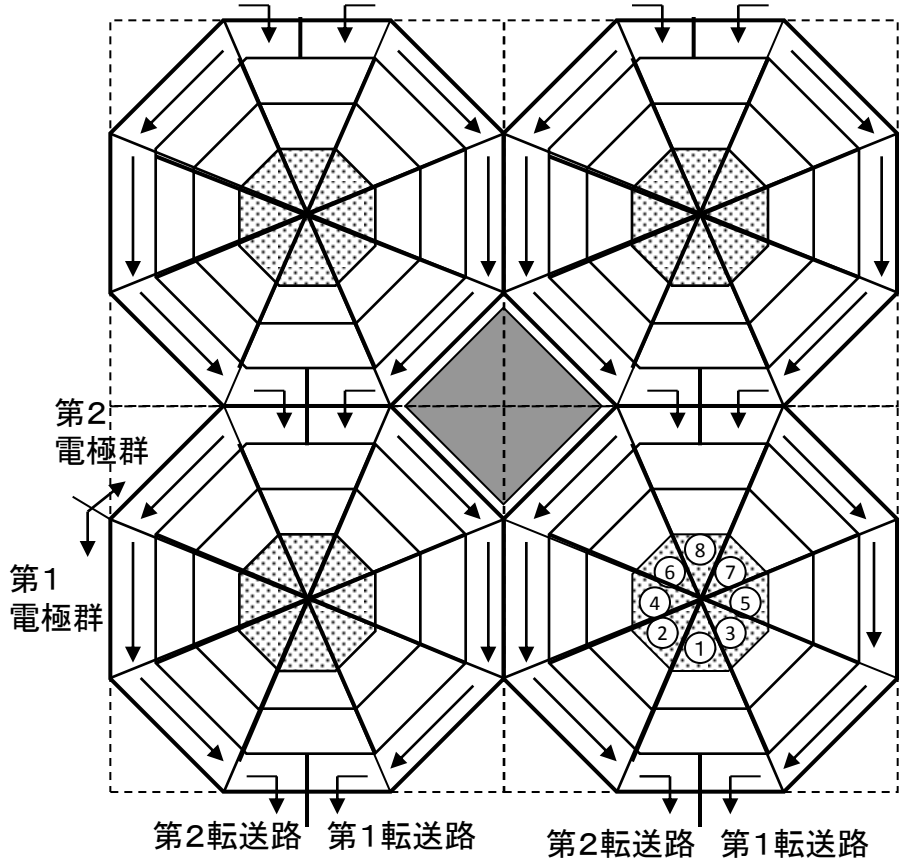
☆ I hope that the new image sensor opens out the new imaging world.☆

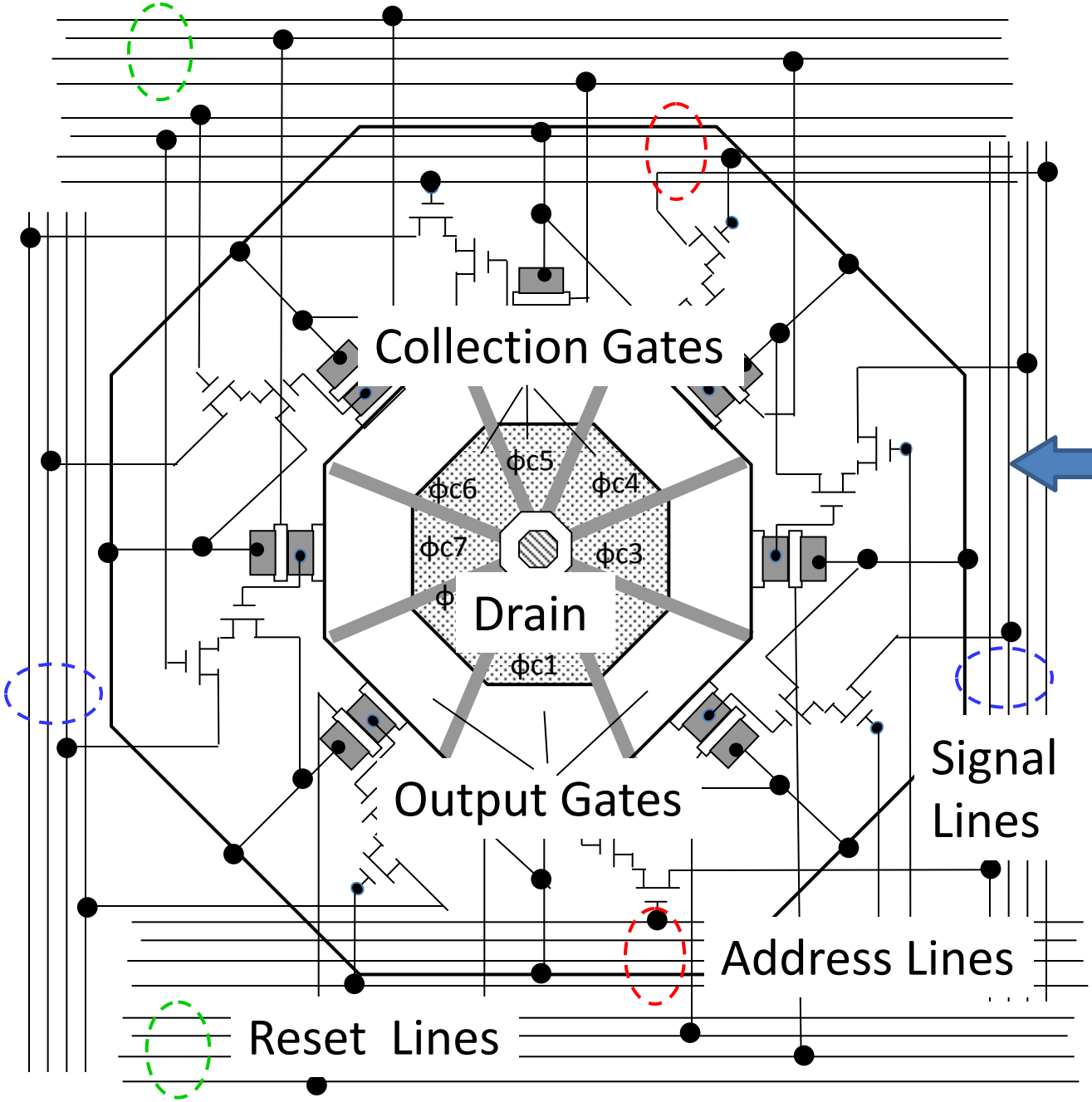
Thank you for your attention.



Principle of Heightening an Imaging Speed by The In-Pixel Multi-Gates

新提案画素の配列2
（正方配列と垂直転送CCD構成）





Next Generation !

Tetra-stratified BSI
+
Stacking

[Chip 1]
Honeycomb Multi-Collection Gates/ Readouts

+

[Chip 2 + more]
- Analogue Memory
- ADC+Dig. Memory
- ADC+Time Record
, etc

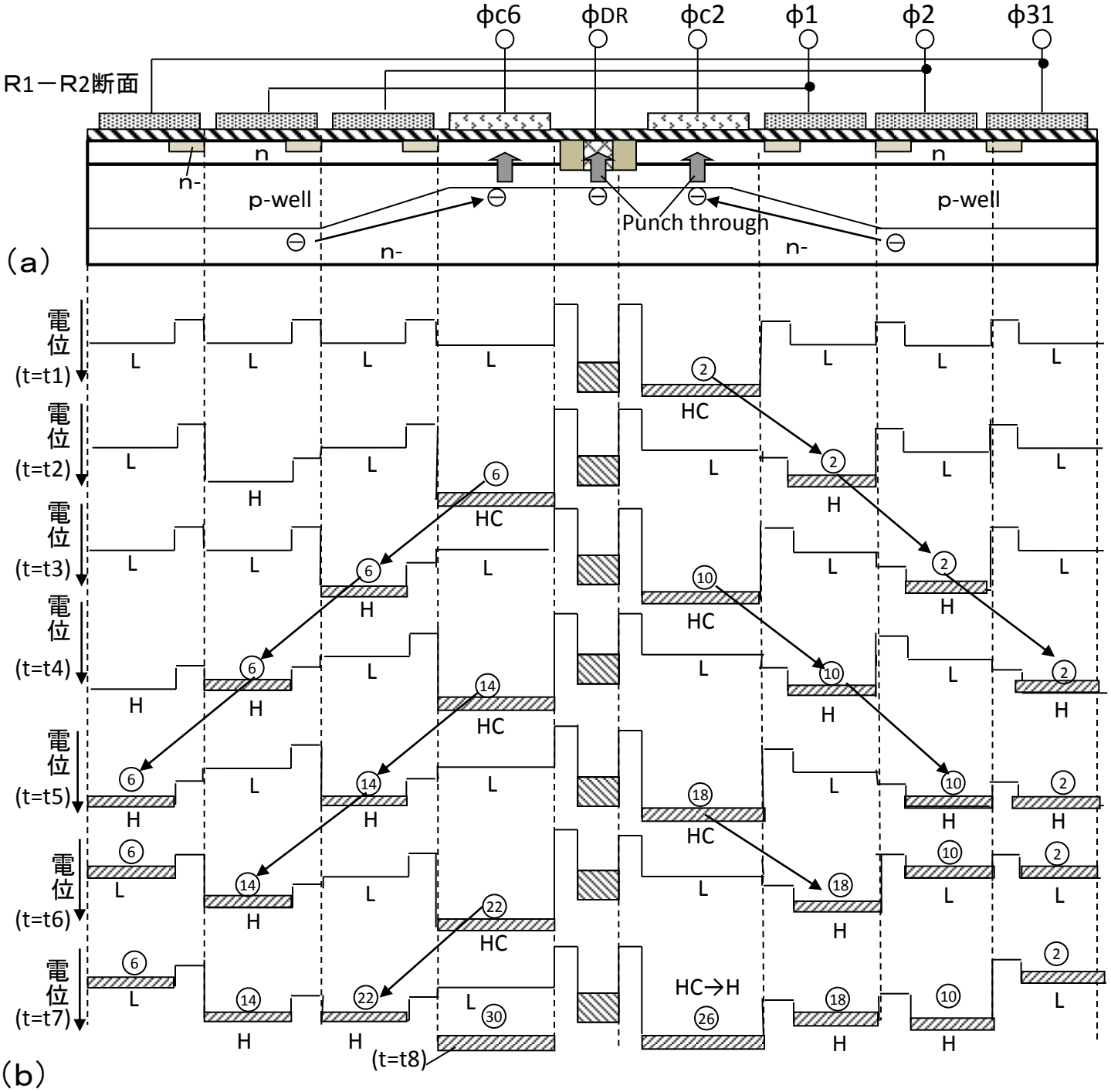
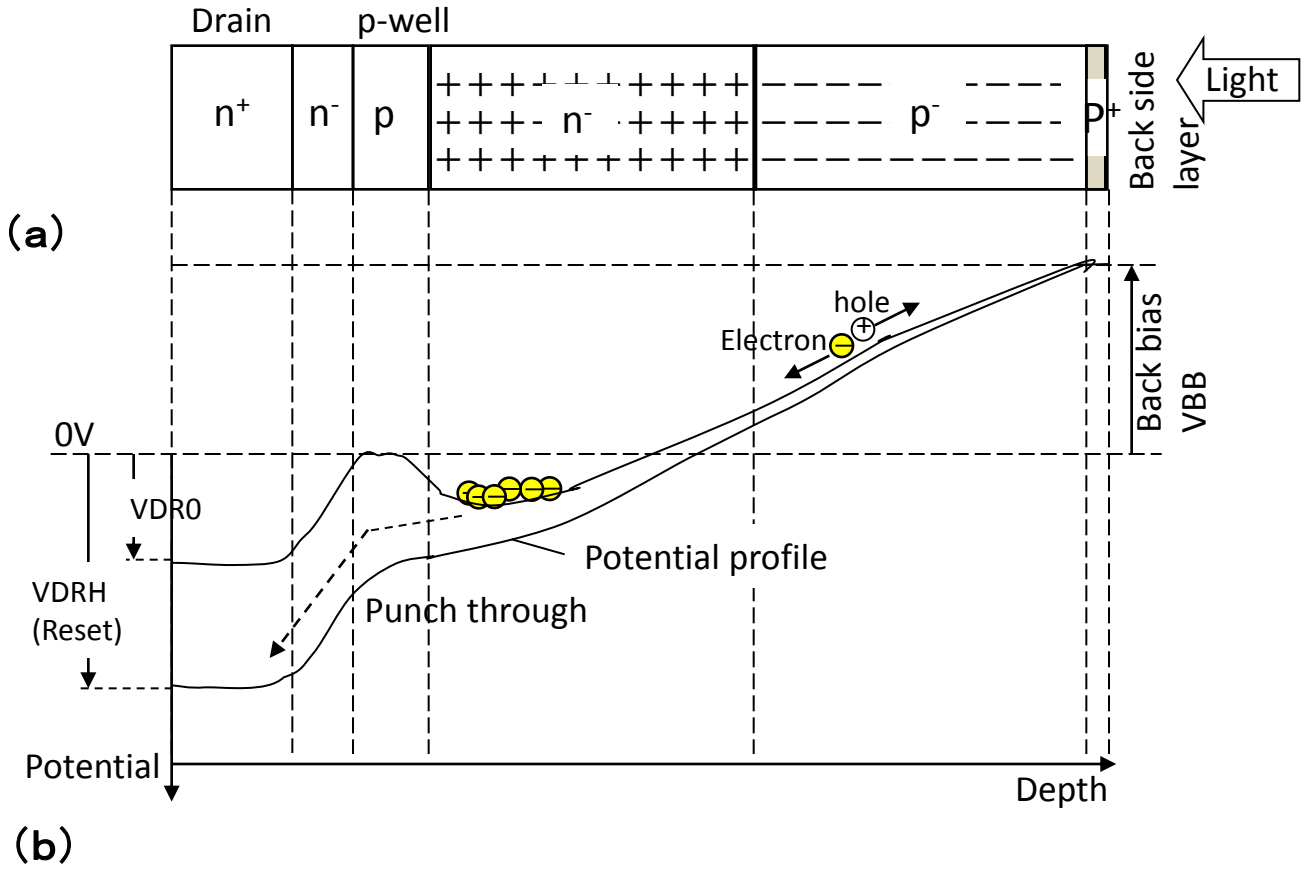


図5（a）断面構造略図と（b）動作原理図



Global Reset Mechanism

(a) One Dimensional Si-Bulk Structure, (b) Potential Profile

感度（入射光量）に関する課題

超高速イメージセンサが直面する本質的問題の一つとして感度（入射光量）がある。
ここでは、波長550nmの光を例に議論する。

・フォトンのエネルギーをEとすれば、$E=h\nu$（h：プランク定数，ν：波数）であるから、波長550nmのフォトンは、$E=3.61\times10^{-19}$ [J]のエネルギーをもつ。

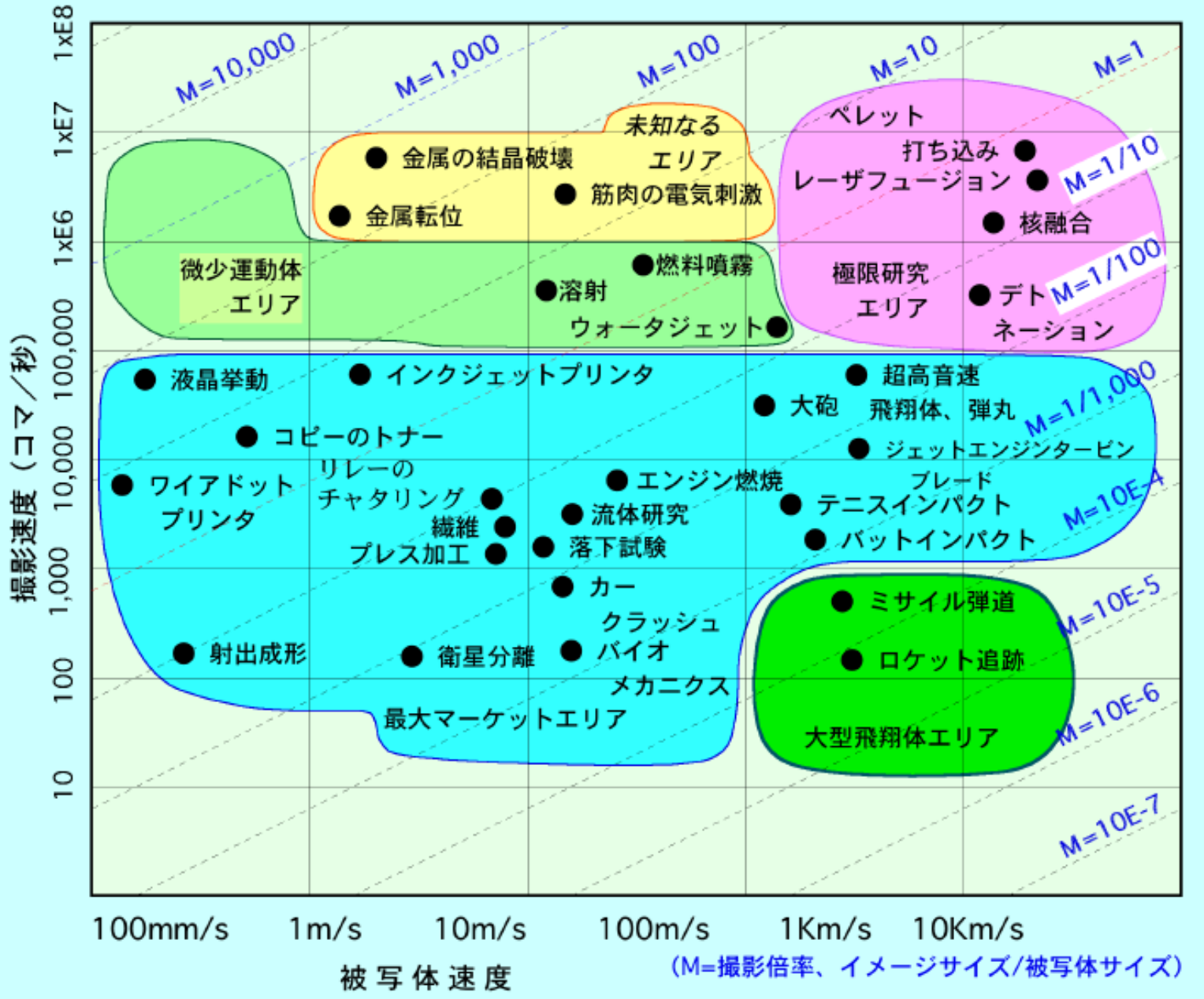
・1ルックスは、標準比視感度（683 lm/W at 555nm）から、1.46×10^{-3}[J/sec･m^2]に換算できる。

・電荷収集時間t_i[sec]，照度P[lux]，面積S[m^2]の場合の入射フォトン数N_pは、

$$N_p=0.404\times10^{16}\cdot t_i\cdot P\cdot S \quad [個] \qquad (1)$$

となる。

【計算例】(1)から1画素に1フォトン入射するに要する照度P_1を求める。
$t_i=10^{-8}$sec (100Mfps) 、画素サイズ:10μm 角の場合の$N_p=1$になる照度P_1は、
$P_1=247$[lux]になる。→ 外部量子効率を1に近づけても、約250luxで
1電子が得られるに留まる。→ Photon Counting の領域
100電子の信号を得るには、約25,000lux が必要。
→ 用途（被写体）によるが、画素サイズは出来るだけ大きくするのが良いか？
【拡大例】 画素サイズを33μm角に拡大すれば、感度(入射フォトン数)は1桁増加。
面積拡大により、メモリ数も増加できるので、連続200 frames程度は容易。
→ 以上の課題を踏まえ、画素サイズを含めた画素設計を最適化する必要がある。



高速度カメラ応用分布図

安藤幸司，**高速度カメラ入門 Q&A**