The Belle II pixel detector

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On behalf of the DEPFET Collaboration

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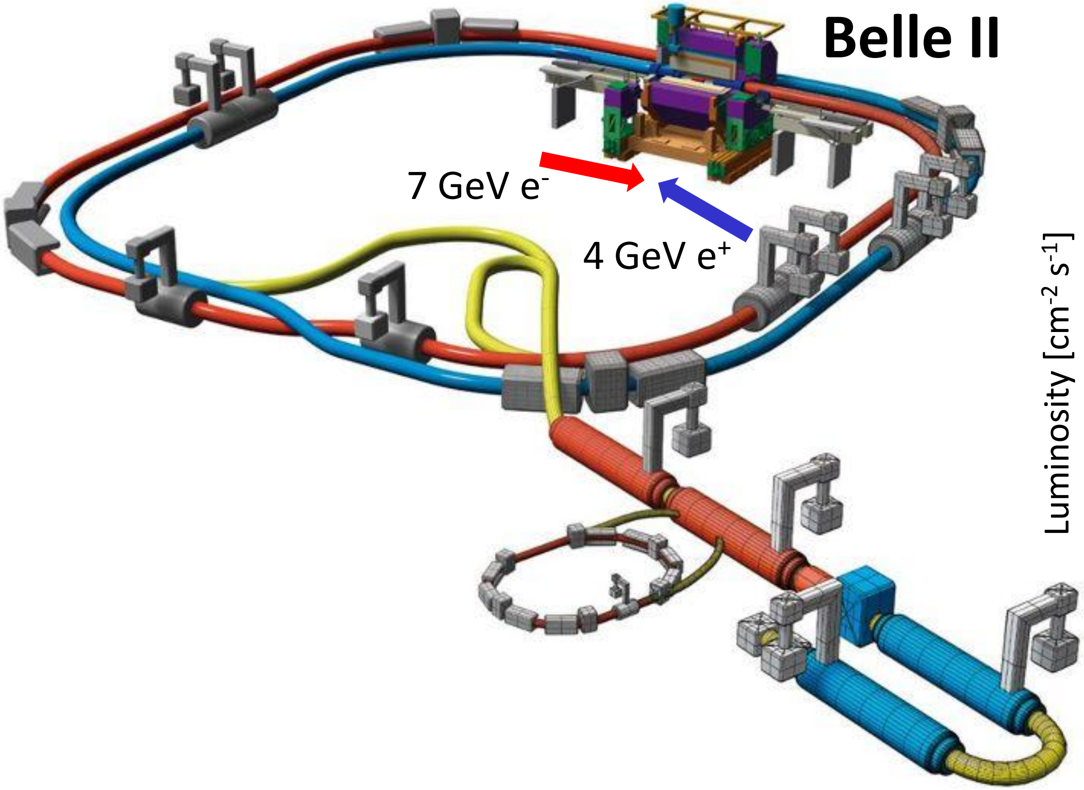
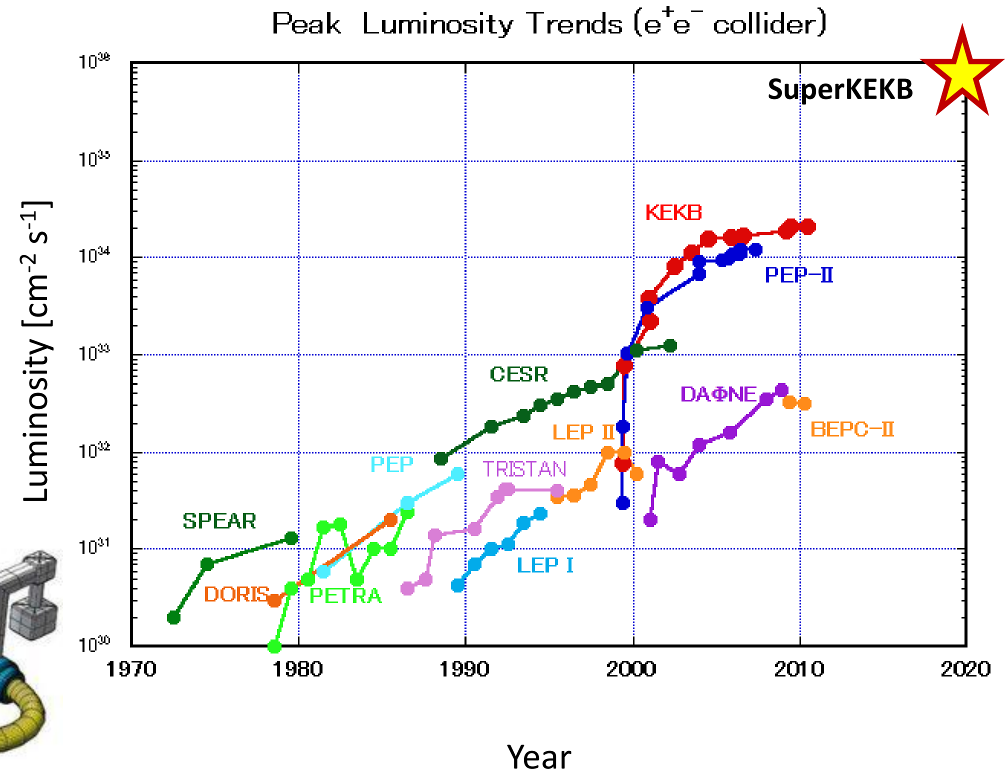
Outline

- SuperKEKB
  - KEKB machine upgrade
  - Belle II DEPFET pixel detector (PXD)
- DEPFET
  - Fundamentals
  - System elements
- Belle II PXD Recent progress
  - PXD6 production
  - Lab and beam tests
  - Radiation hardness

KEKB upgrade plan: SuperKEKB Flavour Factory





- Asymmetric energy (4 GeV, 7 GeV) e^+e^- collider at the E_{cm}=m(Y(4S)) to be realized by upgrading the existing KEKB machine (Tsukuba, Japan)
- Collisions with very small spot-size beams (*nano beam*) and higher currents
- Final luminosity $8\cdot10^{35}$ cm^{-2} s^{-1}, 40 times higher than the existing KEKB Factory
- Start of the machine commissioning in 2014
- Start of the physics run in 2015

KEK High Energy Accelerator Research Organization

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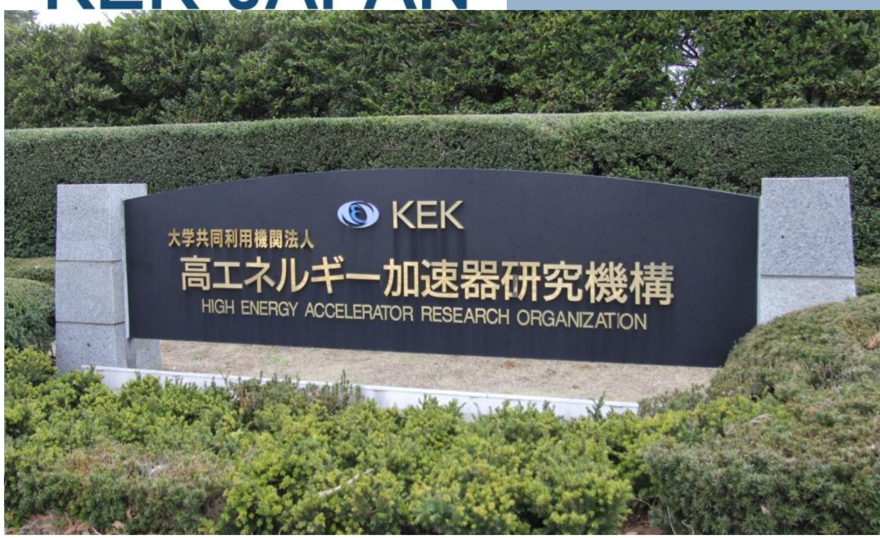
KEK-JAPAN



~ 250 km away from the Conference site

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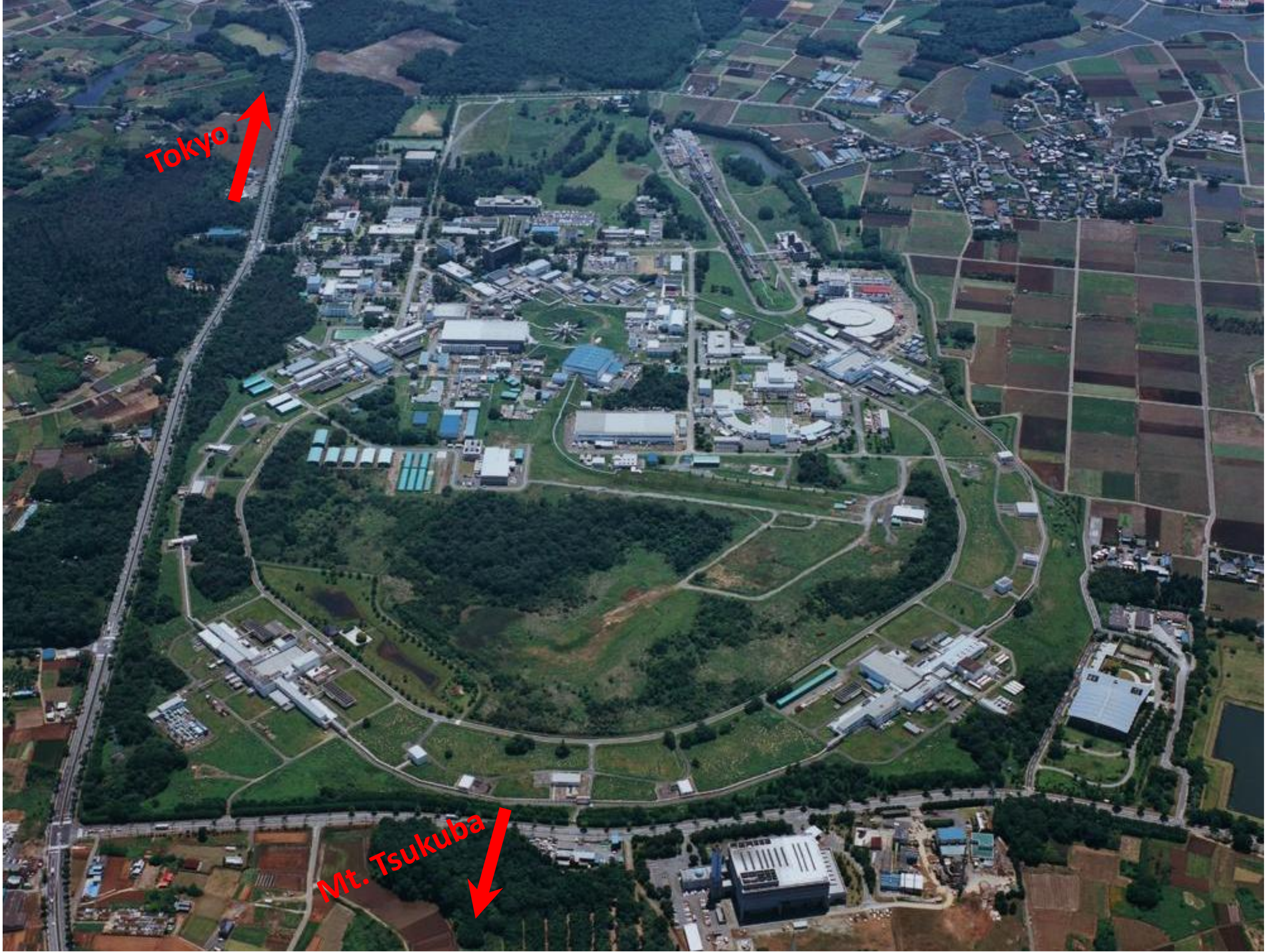
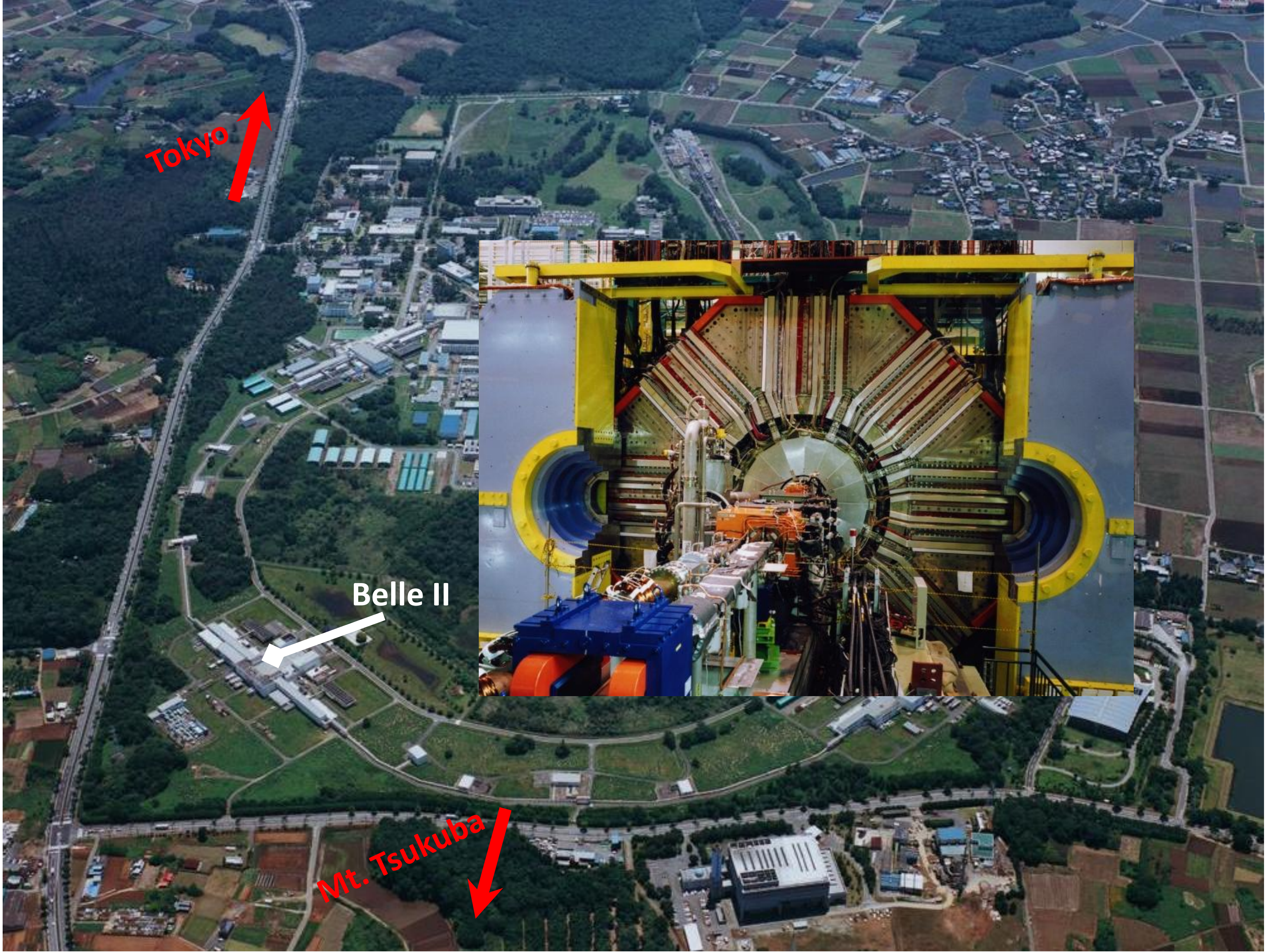
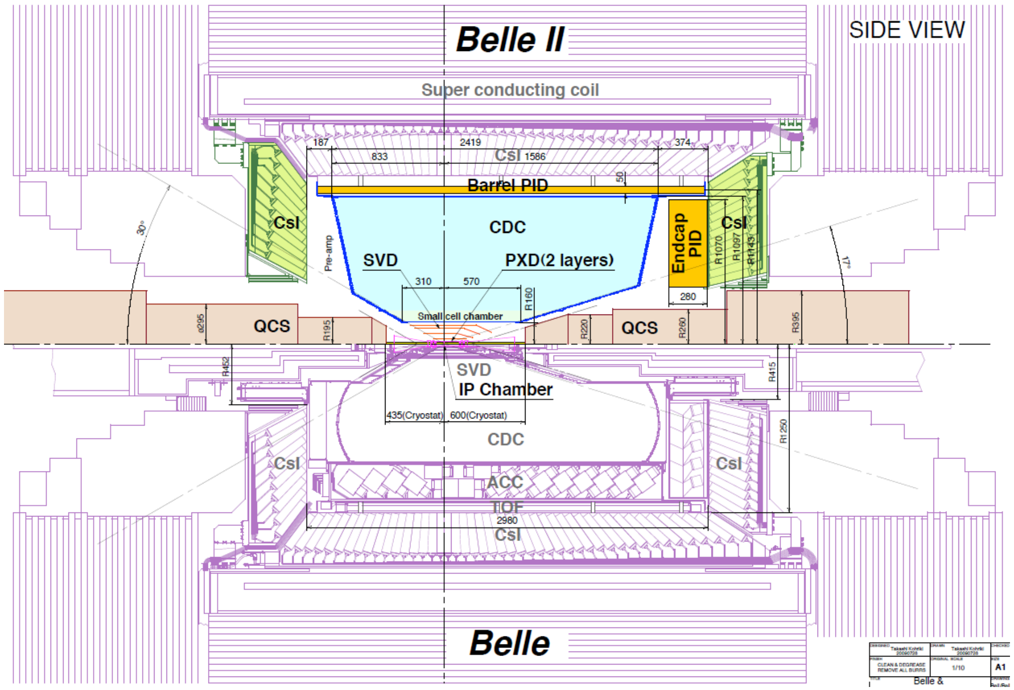
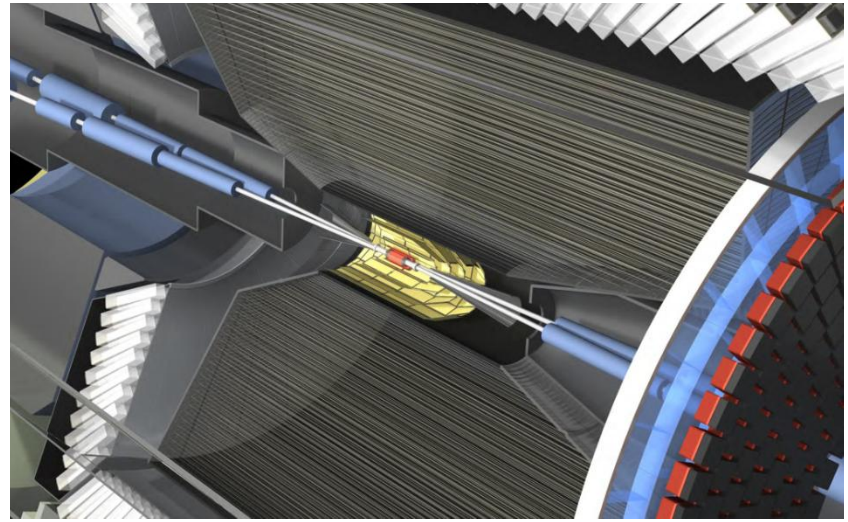

Tokyo
Mt. Tsukuba



Tokyo
Belle II
Mt. Tsukuba

Belle II Silicon Vertex Detector





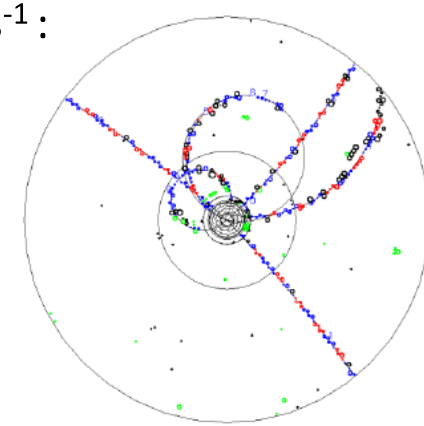
New: The Belle II Collaboration decided on DEPFETs for the two innermost layers

- ✓ More robust tracking (6 layers)
- ✓ Better vertex resolution (closer to IP)

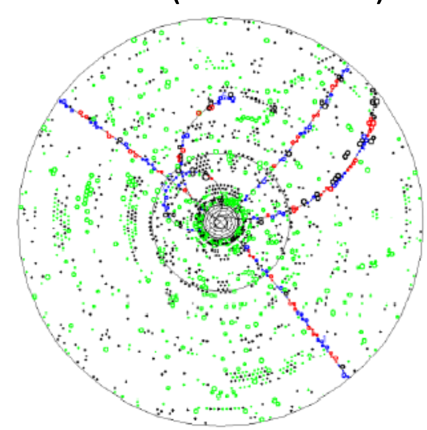
▪ Critical issues at ultra high luminosity $\mathcal{L}= 8{\cdot}10^{35}\ cm^{-2}\ s^{-1}$:

- Higher background
  - → Radiation damage , large occupancy, fake hits
- Higher event rate
  - → Higher rate trigger, DAQ and computing

→ <u>Significant upgrade</u>!



Belle



Belle II

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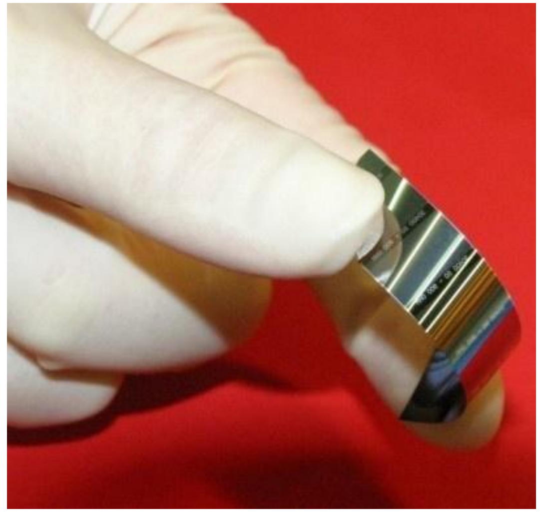
Belle II PXD detector requirements

	Belle II PXD
Occupancy	0.1 hits/µm²/s
Radiation	1.5 Mrad/year
Frame time	20 µs (continuous r.o. mode)
Momentum range	**Low momentum** (< 1GeV)
Acceptance	17º-155º



The combination of resolution, mass and power dissipation is a substantial challenge

- Belle II is dominated by low momentum tracks
  - ➢ Modest intrinsic resolution (10 µm), dominated by m.s. → Moderate pixel size (50 x 75 µm²)
  - ➢ Lowest possible material budget (0.2% X_0/layer**)

→ The DEPFET technology can cope with these challenging requirements

Tight schedule to develop a complete detector system by 2015

** Including support Si, bumps and metal layers

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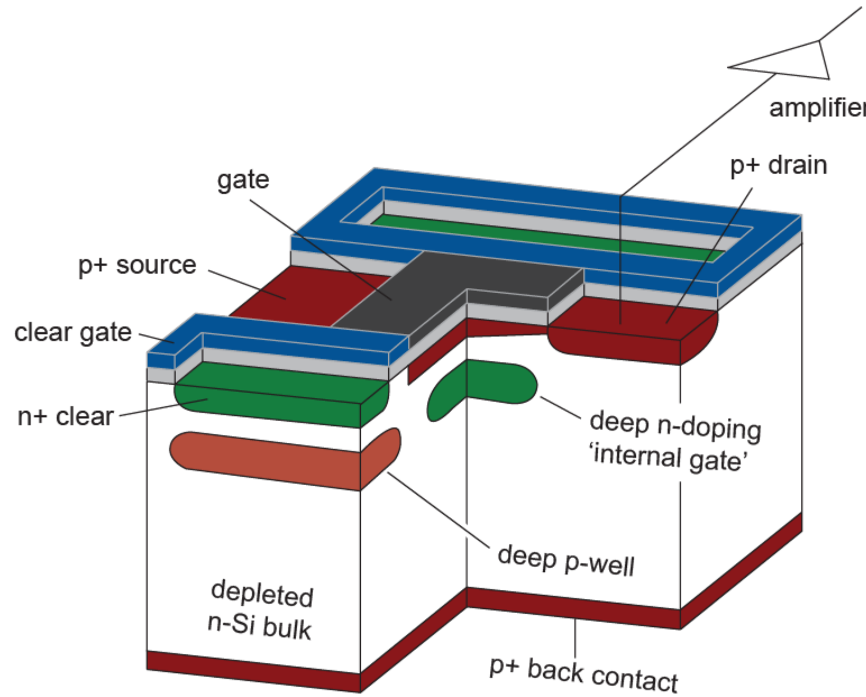
DEPFET – DEpleted P-channel Field Effect Transistor

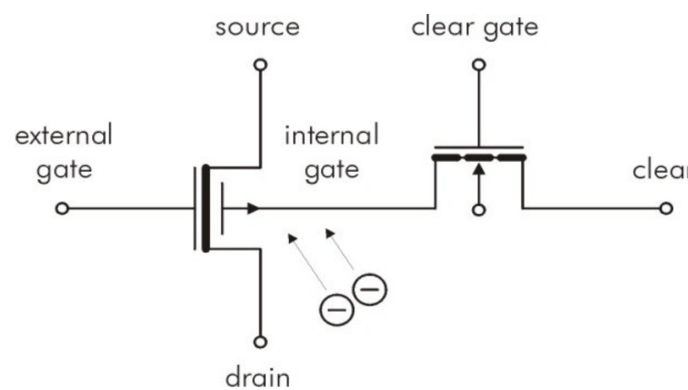
- Each pixel is a p-channel FET on a completely depleted bulk (sideward depletion). Charge is collected by drift
- A deep n-implant creates a potential minimum for electrons under the gate (internal gate)



- Signal electrons accumulate in the internal gate and modulate the transistor current ($g_q \approx 400$ pA/e$^-$)
- Accumulated charge can be removed by a clear contact

- Detection, fast charge collection and internal amplification
- Excellent signal-to-noise ratio
- Low power consumption
- Thin detectors

Features



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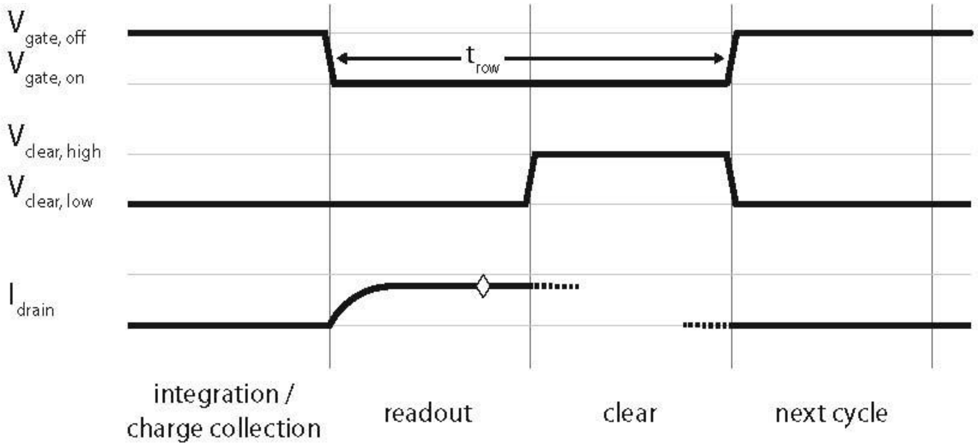
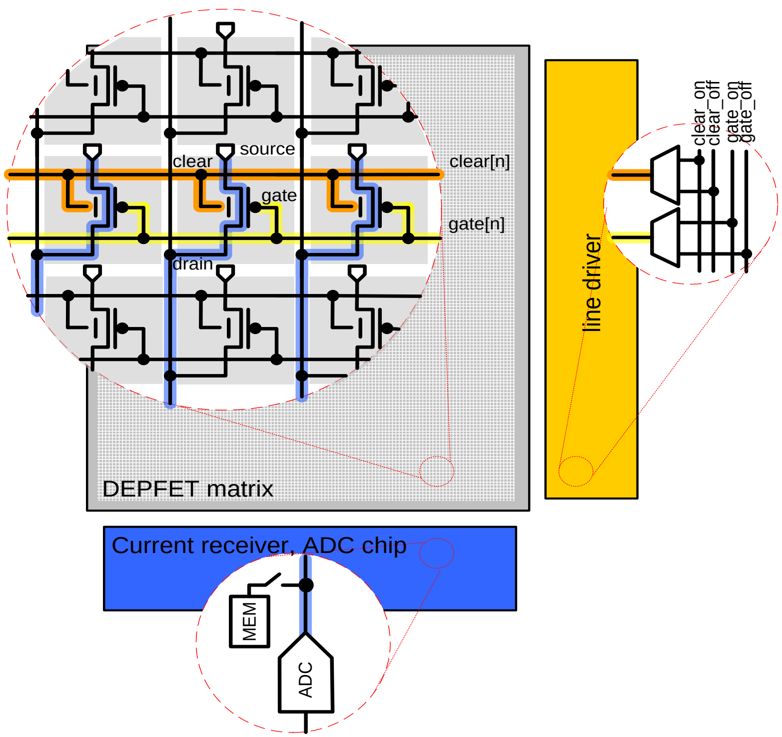
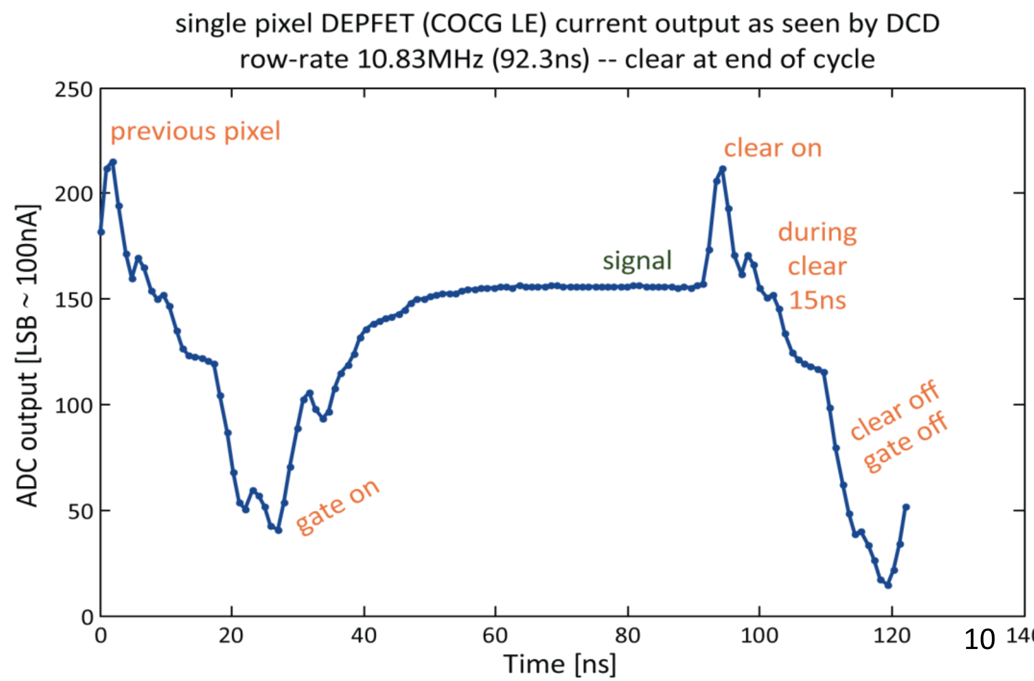
Operation mode: Row-wise readout



Rolling Shutter Mode

- Low power consumption: Only one row is active at a time; readout on demand.
- Single sampling with pedestal subtraction in digital domain
- PXD readout time: 20 µs (50 KHz frame rate)
- Read-clear cycle: 100 ns





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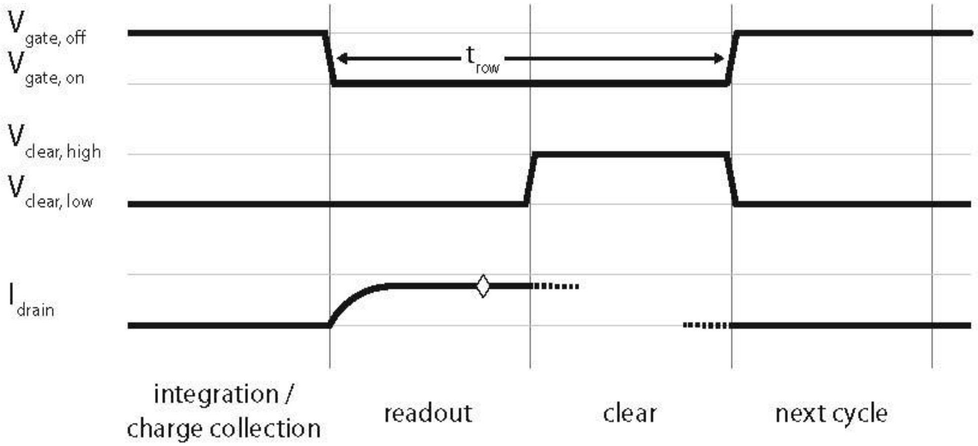

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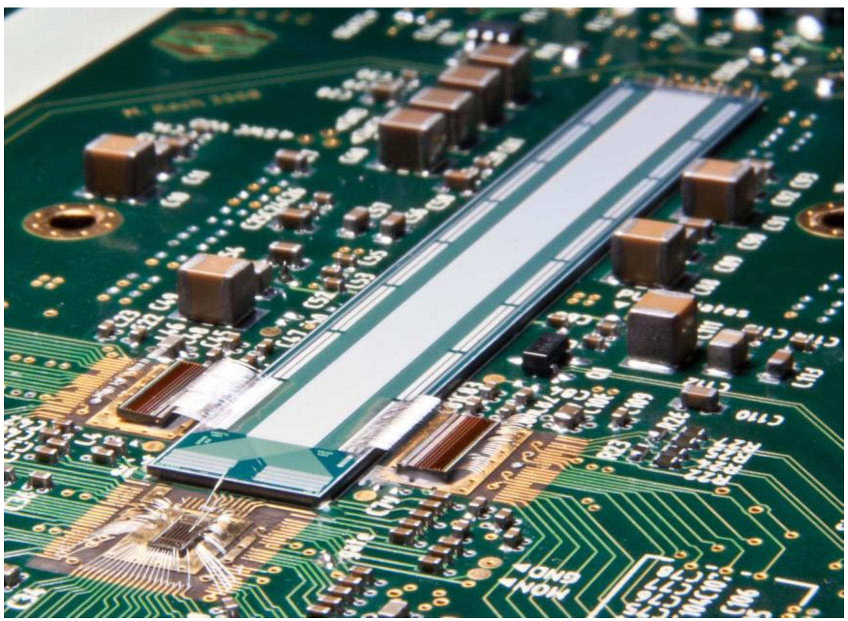

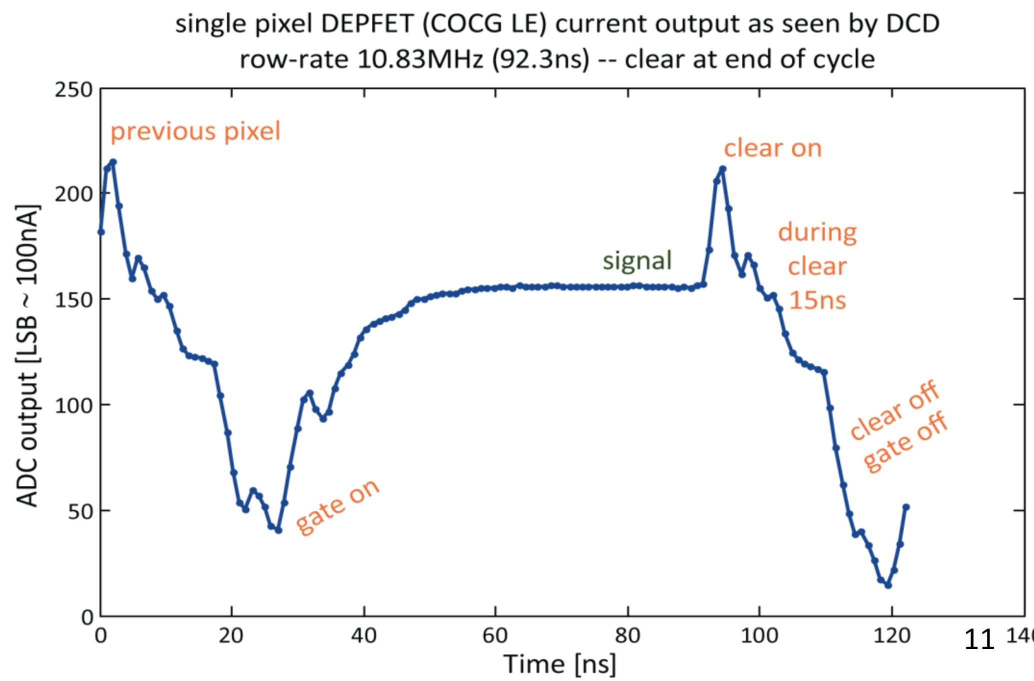

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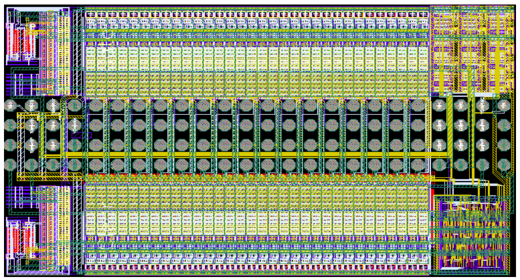
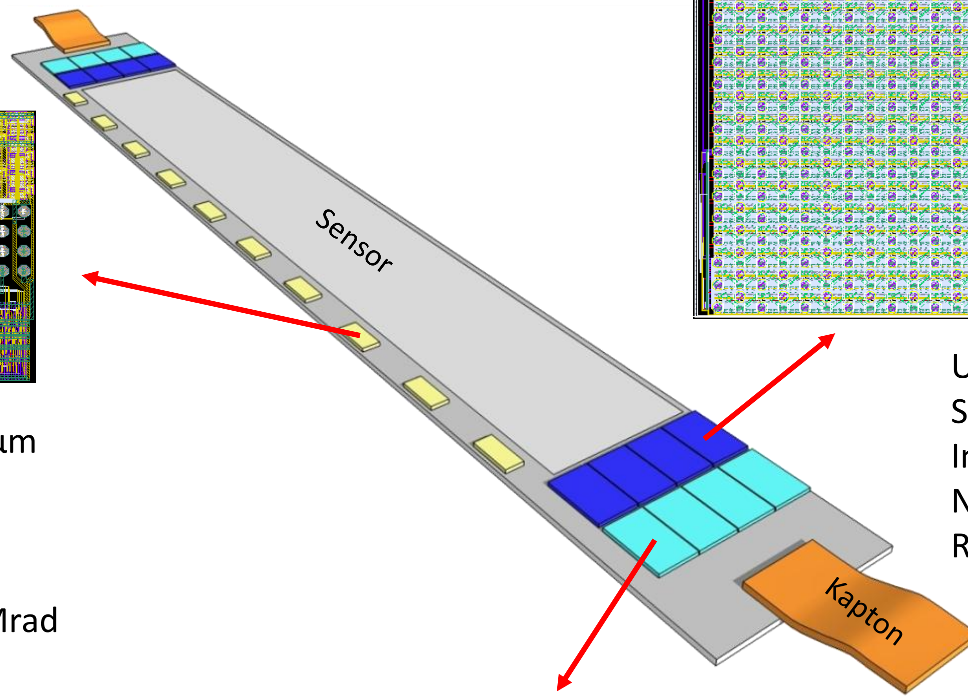
DEPFET auxiliary ASICs

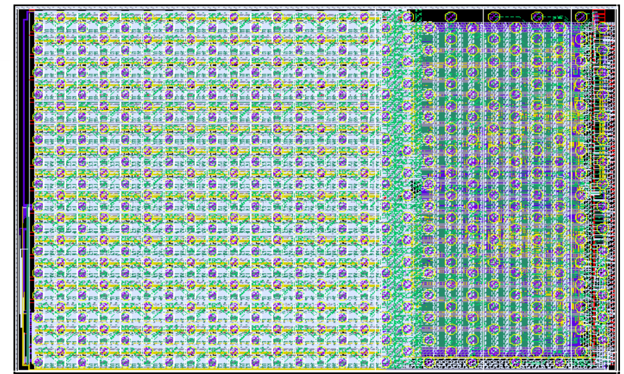
SwitcherB
Row control



AMS high voltage 0.35 µm
Size 3.6 × 2.1 mm²
Gate and Clear signal
Fast HV up to 30V
Rad. Hard proven >36 Mrad

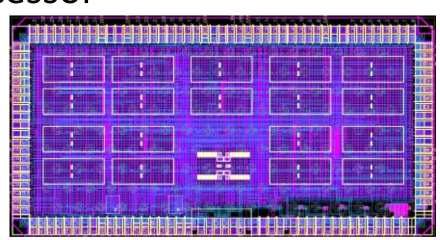


DCDB (Drain Current Digitizer)
Analog frontend



UMC 180 nm
Size 3.3 × 5.0 mm²
Integrated ADC
Noise 40 nA
Rad. Hard proven >7 Mrad

DHP (Data Handling Processor)
Processor



IBM CMOS 90 nm (TSMC 65 nm)
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation
Rad. Hard proven >10 Mrad

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DEPFET auxiliary ASICs

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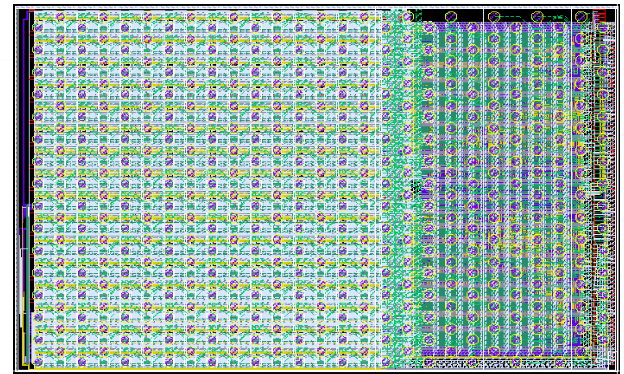
The full-size close to final versions of the ASICs are designed, produced and found to work

DCDB (Drain Current Digitizer)
Analog frontend



UMC 180 nm
Size 3.3 × 5.0 mm^2
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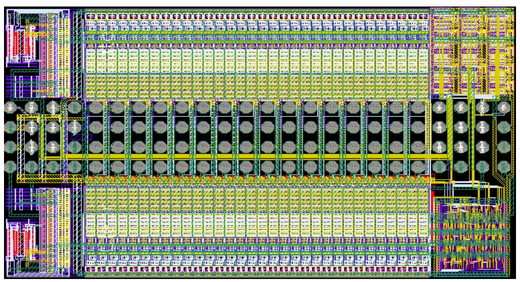
Milestone!

SwitcherB
Row control



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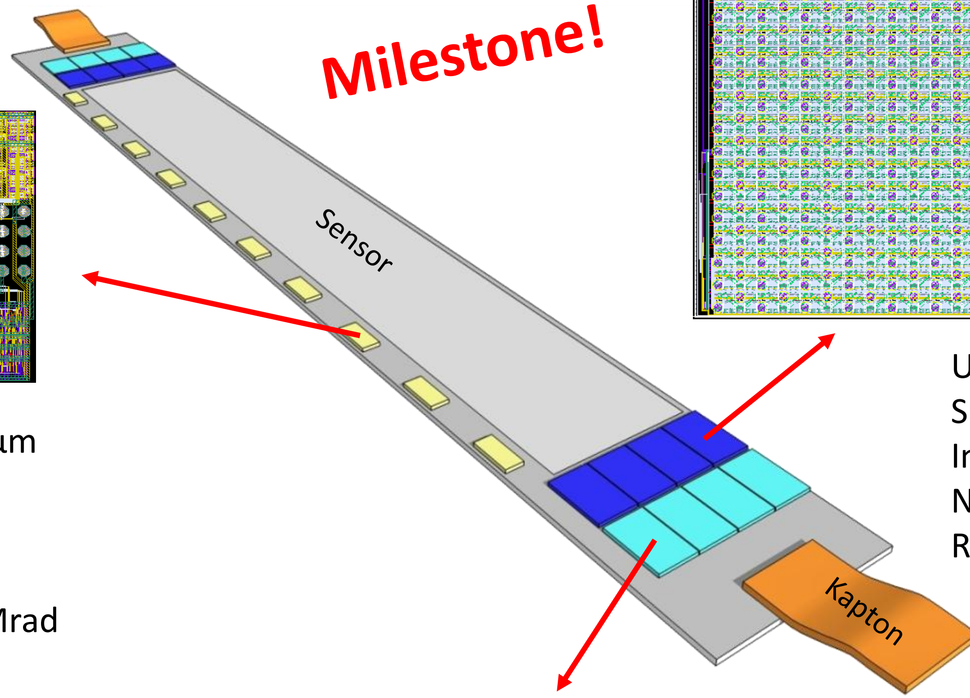

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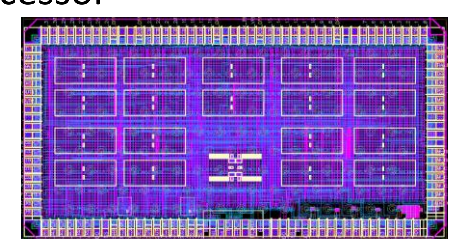


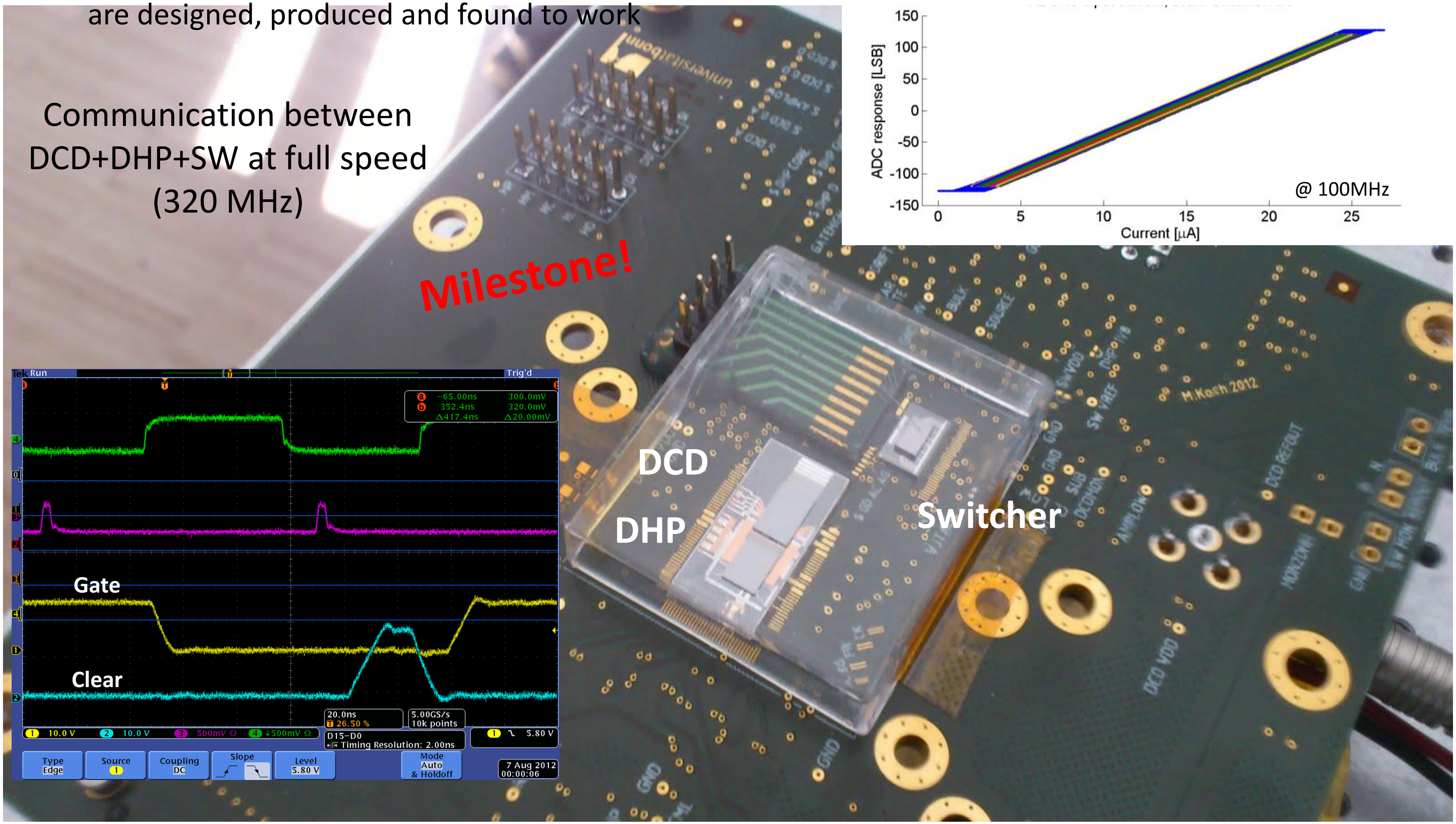
IBM CMOS 90 nm (TSMC 65 nm)
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation
Rad. Hard proven >10 Mrad

The layout of the module periphery is ready as well

DEPFET auxiliary ASICs

The full-size close to final versions of the ASICs are designed, produced and found to work

Communication between DCD+DHP+SW at full speed (320 MHz)



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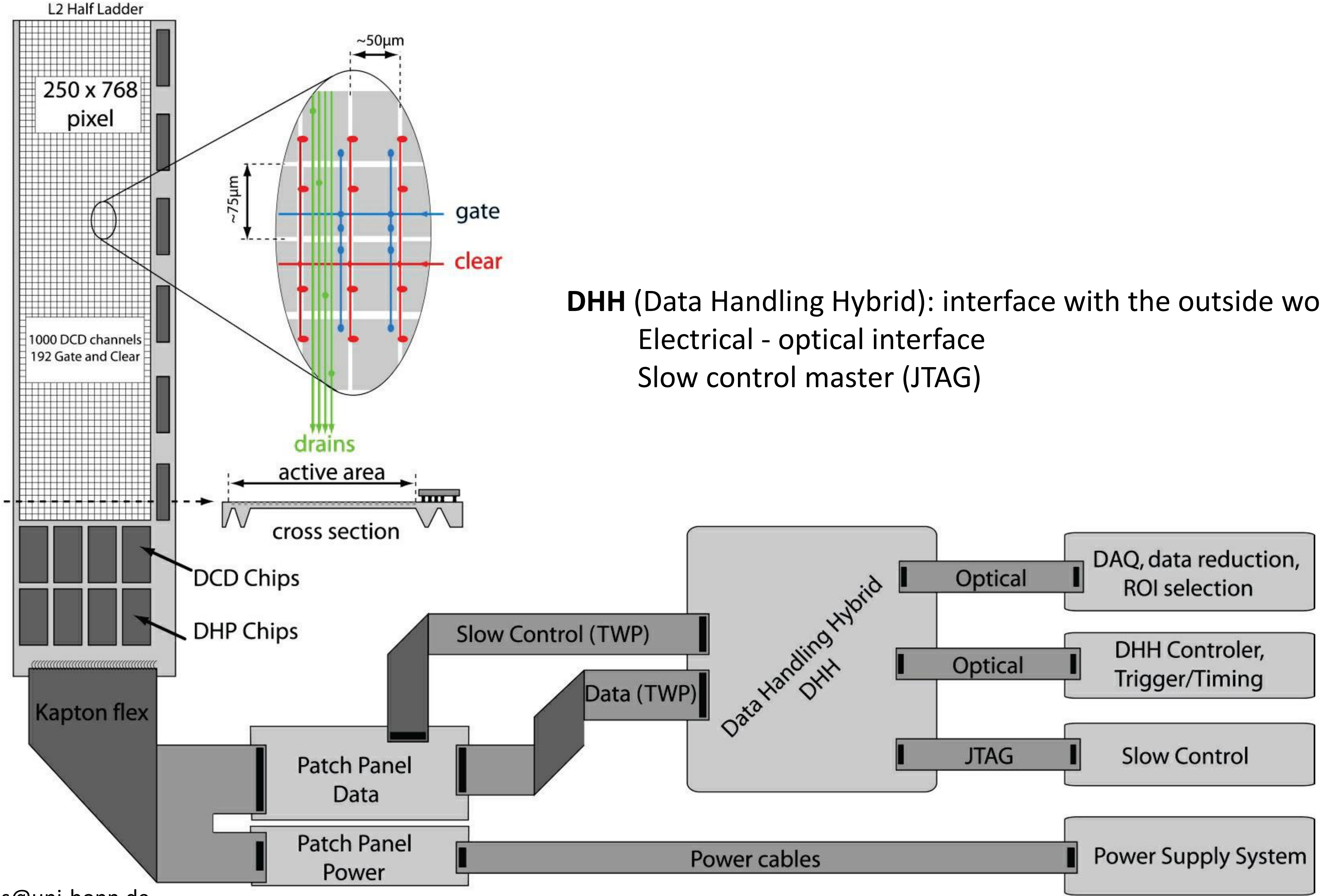
Off-module signal flow



DHH (Data Handling Hybrid): interface with the outside world

Electrical - optical interface

Slow control master (JTAG)

Optimization: Full simulation chain

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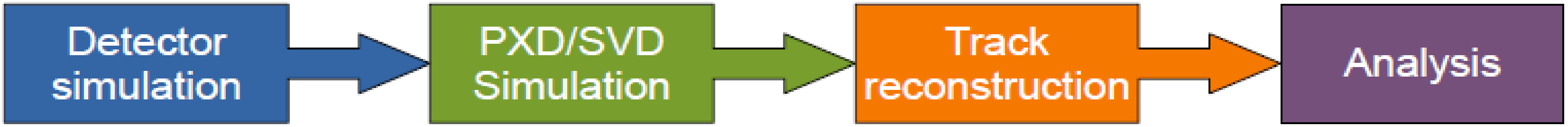
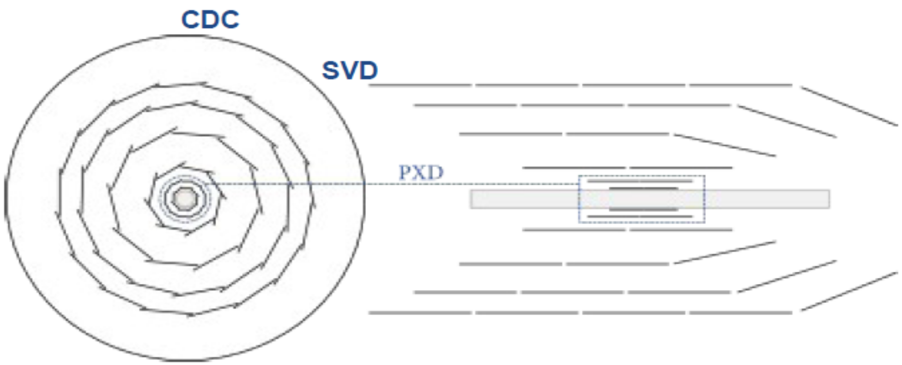


Particle gun (single event)
EvtGen (physics event)
Mokka geometry

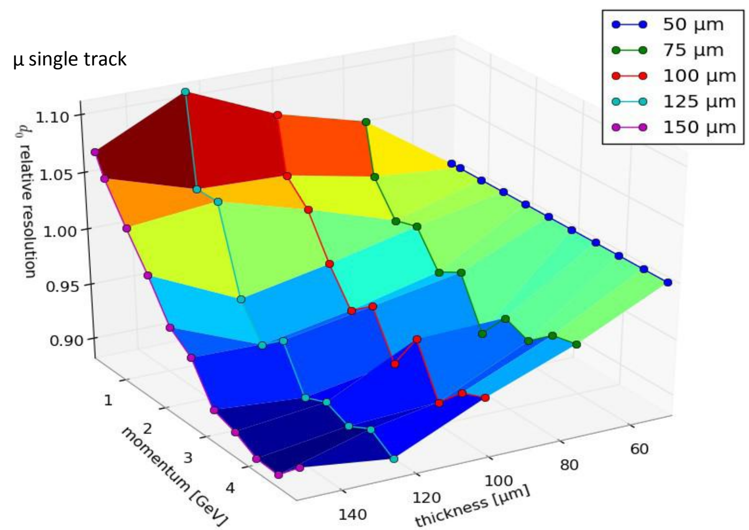
e/h pair creation
Drift/diffusion
Electronic noise
Digitization and clustering

Marlin tracking
PXD+SVD+CDC

Physics channels



- Digitizer (Geant4) tuned with TBeam data:
- Electric noise
- Electric field in Si (charge collection time)
- Lorentz angle in magnetic fields



Optimization studies:
- Sensor thickness
- Pixel size
- Inner layer radius

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Optimization: Full simulation chain

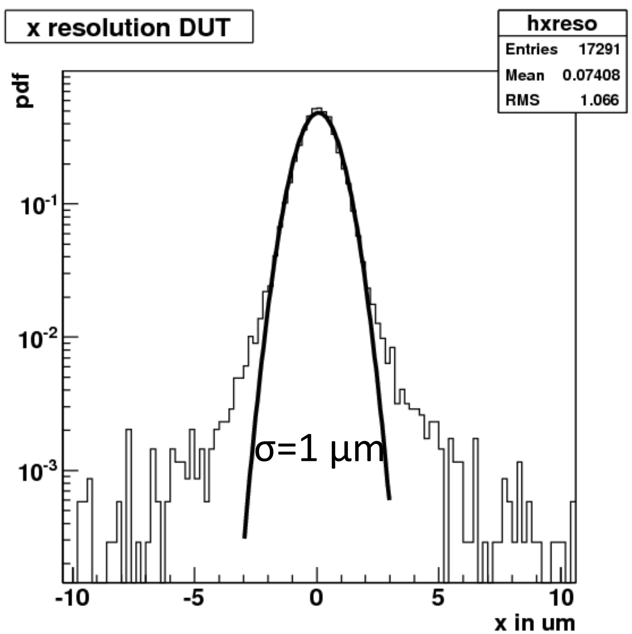
Detector simulation → **PXD/SVD Simulation** → **Track reconstruction** → **Analysis**

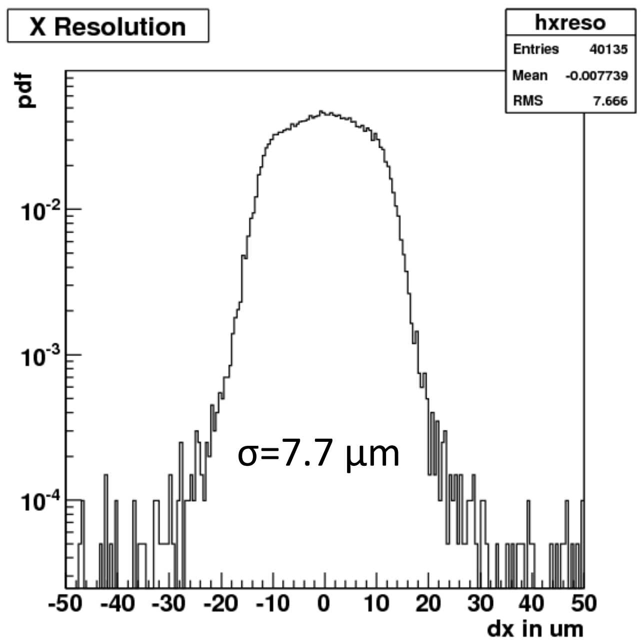
Detector simulation	PXD/SVD Simulation	Track reconstruction	Analysis
Particle gun (single event) EvtGen (physics event) Mokka geometry	e/h pair creation Drift/diffusion Electronic noise Digitization and clustering	Marlin tracking PXD+SVD+CDC	Physics channels

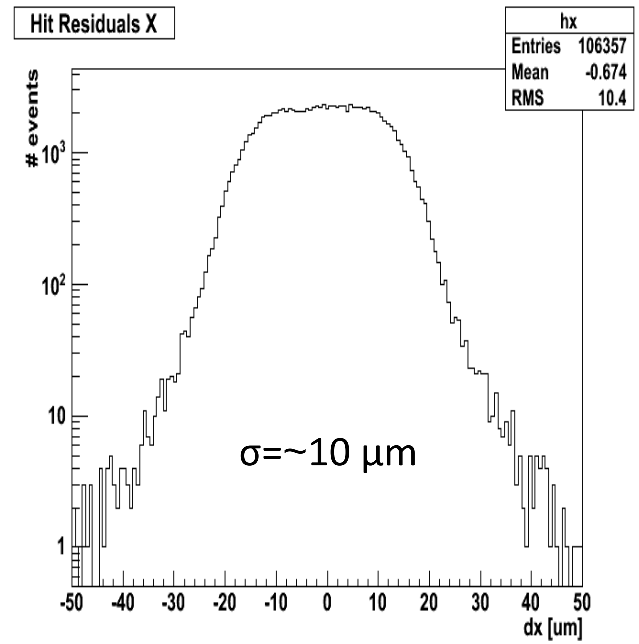
ILC PXD5 Test Beam Data
20x20x450 μm^3
Single point resolution: 1 μm

Belle II (Simulation)
50x50x**75** μm^3
Single point resolution: 7.7 μm

Belle II PXD6 Test Beam Data
50x50x**50** μm^3
Single point resolution: ~10 μm







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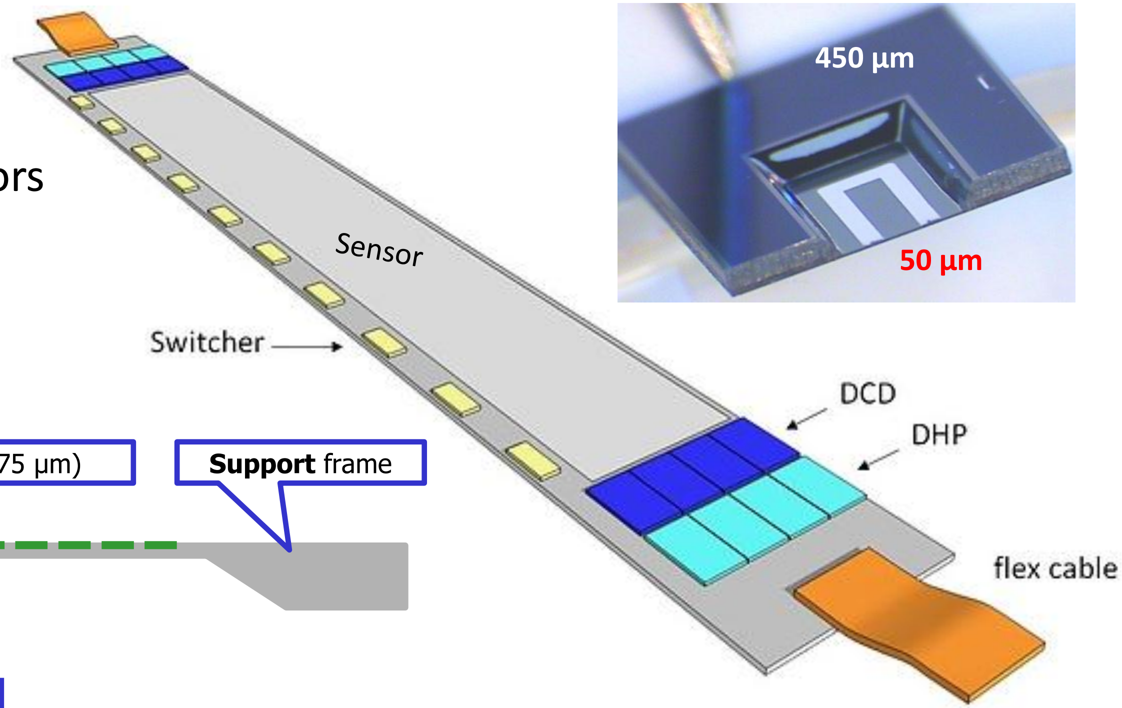
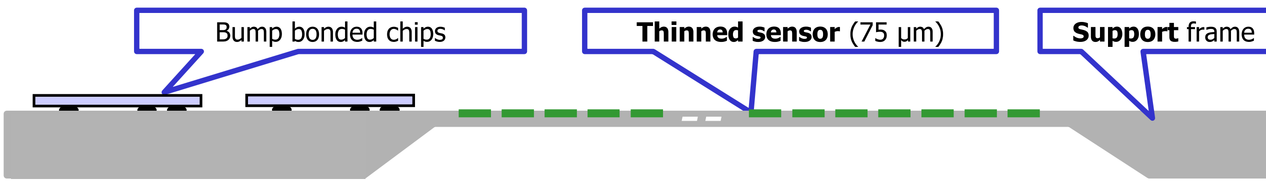
General layout of a DEPFET detector

- The basic unit is the DEPFET ladder
  - Central region covered with thin sensors
  - Switchers on the lateral balcony
  - Front end at both ends





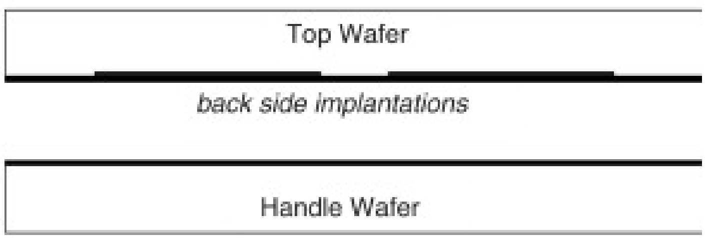
	Belle II	
Radii	14, 22	mm
Ladder length	136 (L0), 169 (L1)	mm
Sensitive width	12.5 (L0-L1)	mm
Number of ladders	8, 12	
Pixel size	50x50 (L0), 50x75 (L1)	µm^2
Row rate	10	MHz
Number of pixels	8	Mpix

- 8 Million pixels
- Close to the IP
- Low material budget
- 0.2% X_0/layer

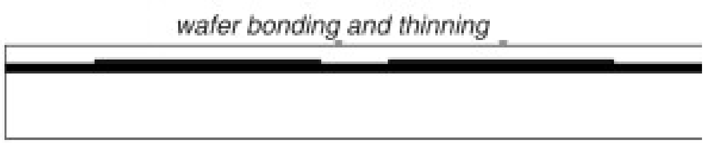
Thinning technology: All silicon sensors

Use anisotropic etching on bonded wafers to create a thin, self-supporting sensor

→ One material uniform and small thermal expansion



• Oxidation and back side implant on sensor wafer

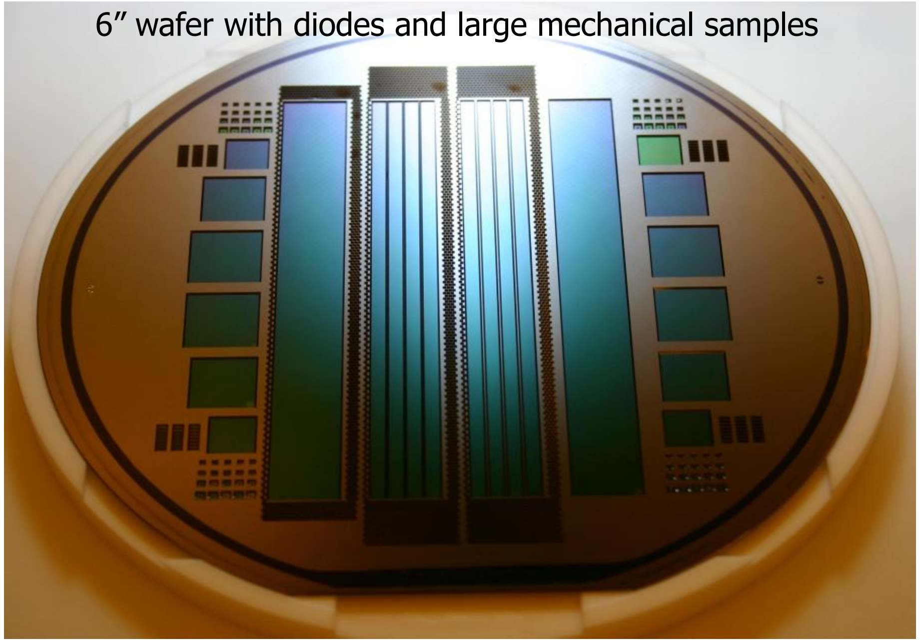


• Wafer bonding (with SiO_2 in between) and grinding/polishing of top wafer. Thin sensor side to the desired thickness

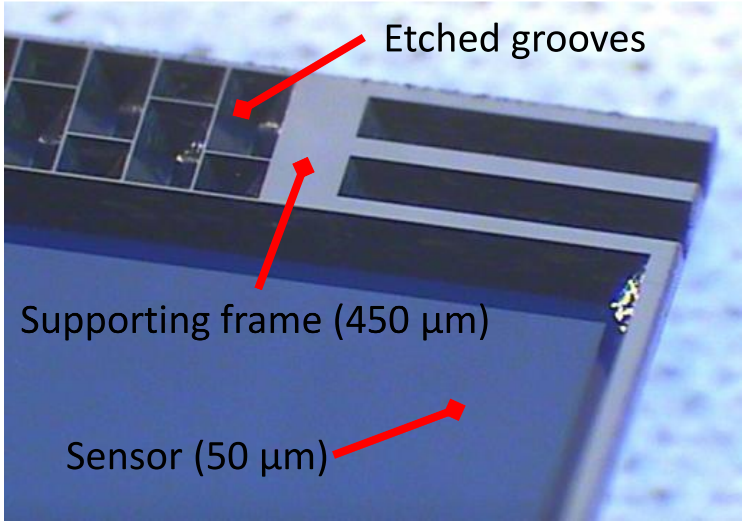
• Process DEPFET on top side → passivation

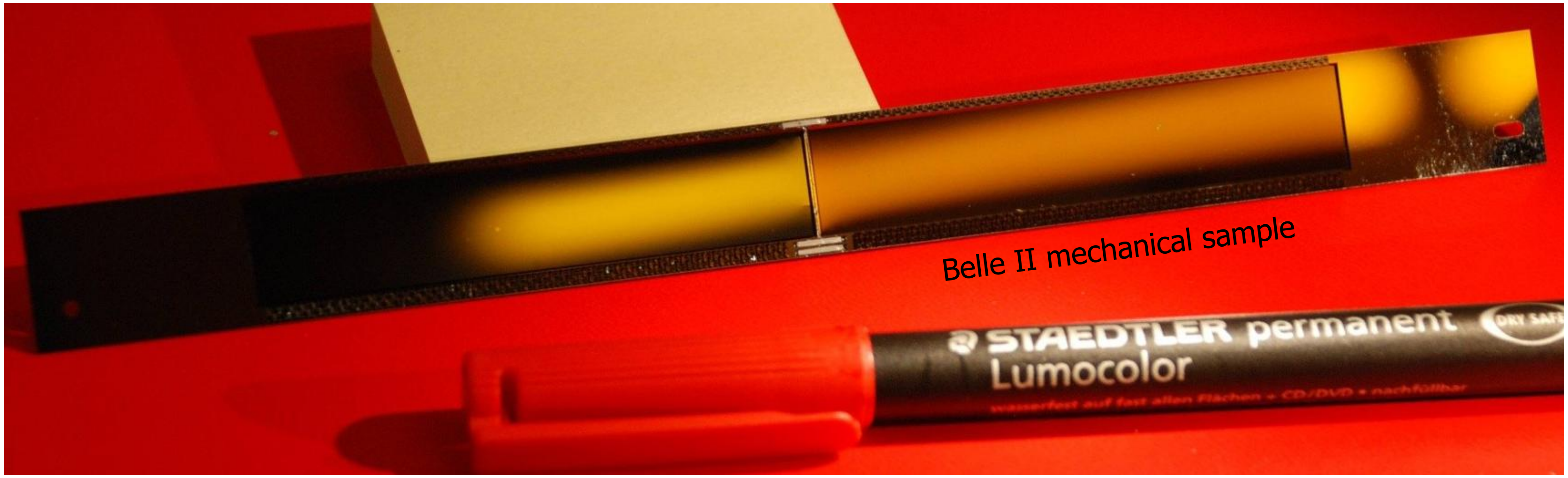
• Anisotropic deep etching opens “windows” in the handle wafer. Etch backside up to oxide/implant (etch stops SiO_2)

Thinning technology



All-silicon sensors





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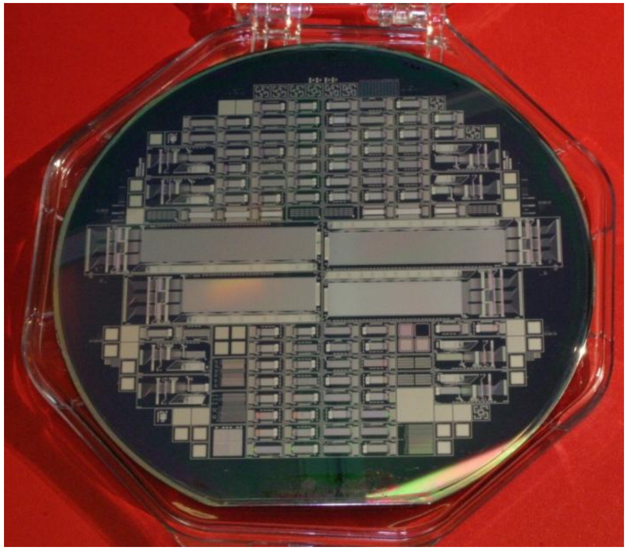
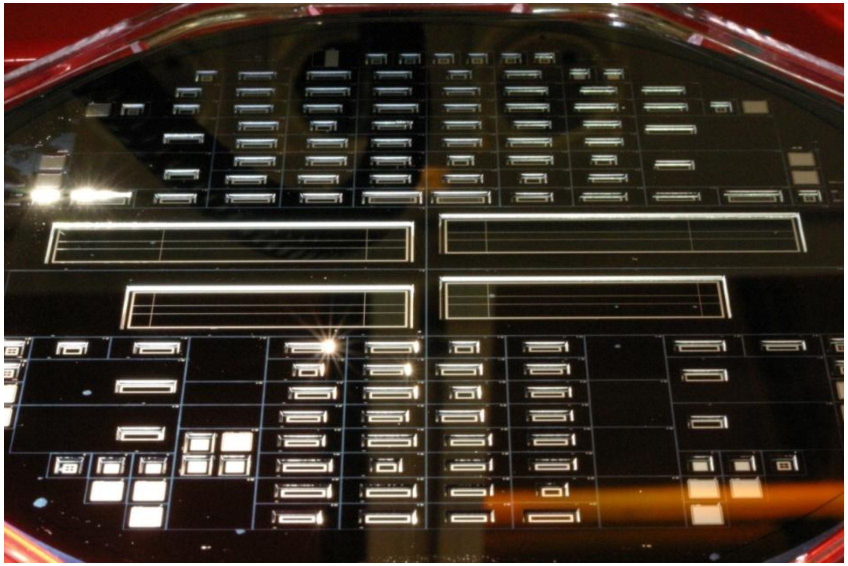
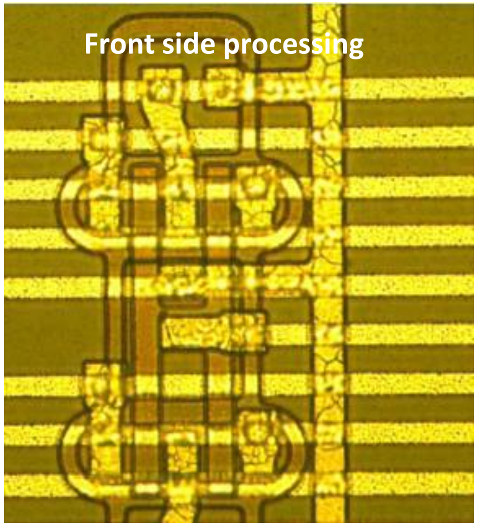
PXD6 prototype production



8 wafers with 50 µm thin sensors

- Small test matrices to test different pixel sizes (50-200 µm)
- Design variations: short gate lengths, clear structures, drift
- Full size sensors –half ladders for prototyping
- Technology variations on the wafer level





90 steps fabrication process:

25 mask steps
9 Implantations
19 Lithographies
Double Poly layers
3 Metal layers
Back side processing

First thin DEPFET sensors produced!

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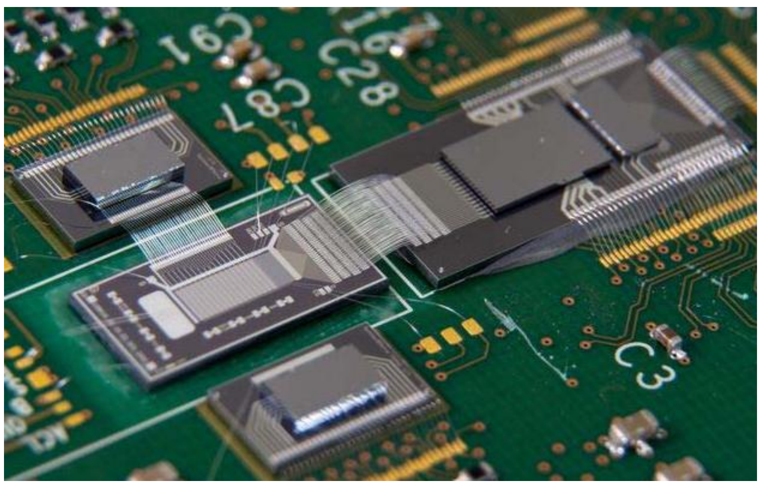
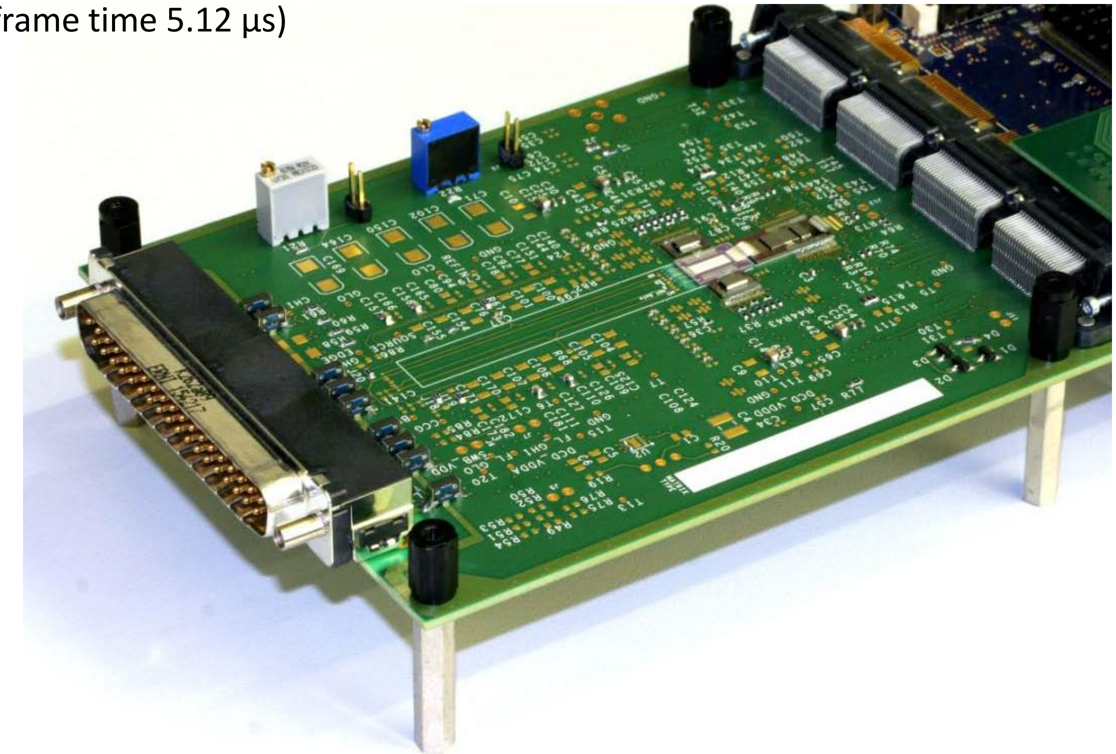
PXD6 - Beam Tests

Measurement in 120 GeV Pion beam at CERN SPS

- PXD6 Standard Design ***Belle II Type***
- SwitcherB and DCDBv2 (100 MHz*, frame time 5.12 µs)
- Pixel size 50x75x50 µm^3
- Gate Length 5 µm
- Thick oxide*

Close to final specs!





Based on the valuable information obtained with the PXD6, the final Belle II production (PXD9) is already launched

Electrically precharacterized in the lab

* 320 MHz and thin oxide in the final production

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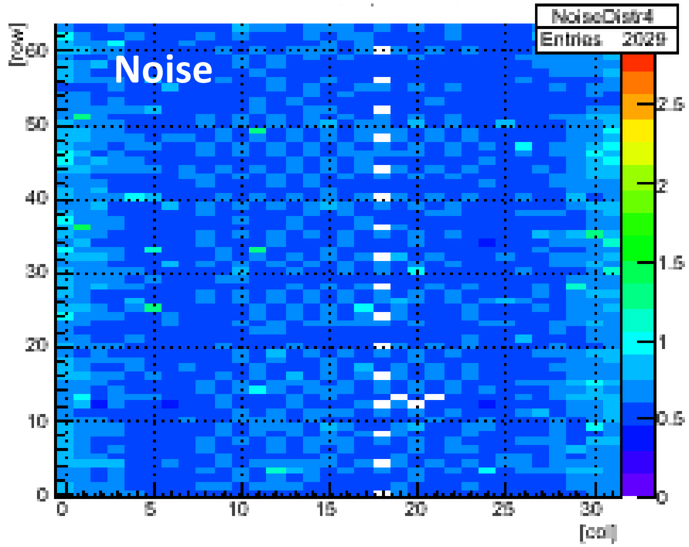
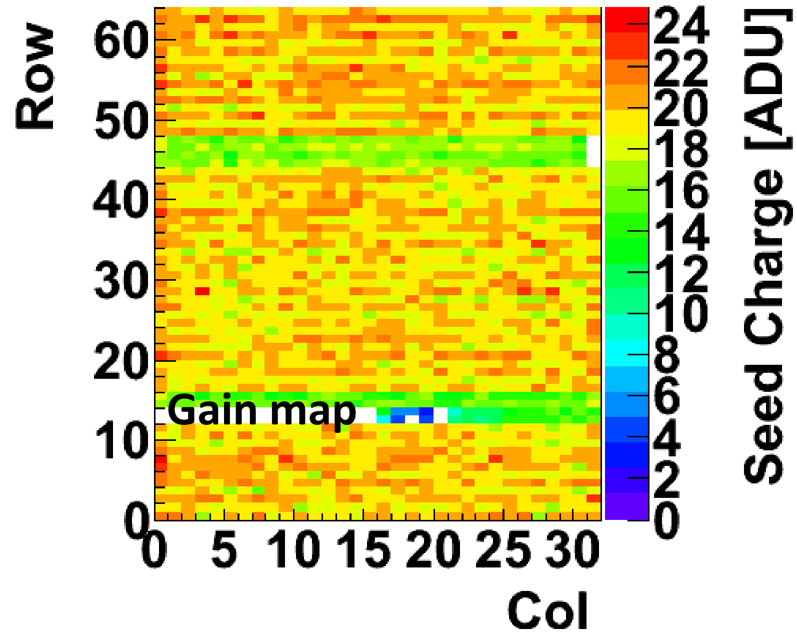
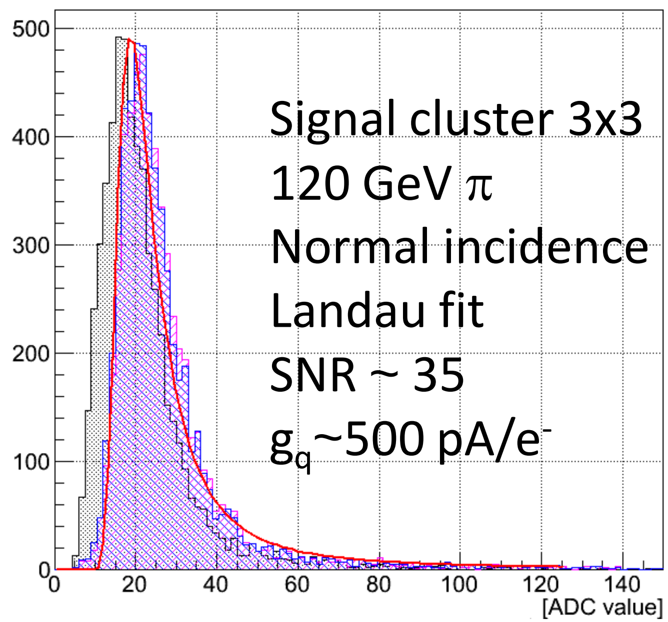
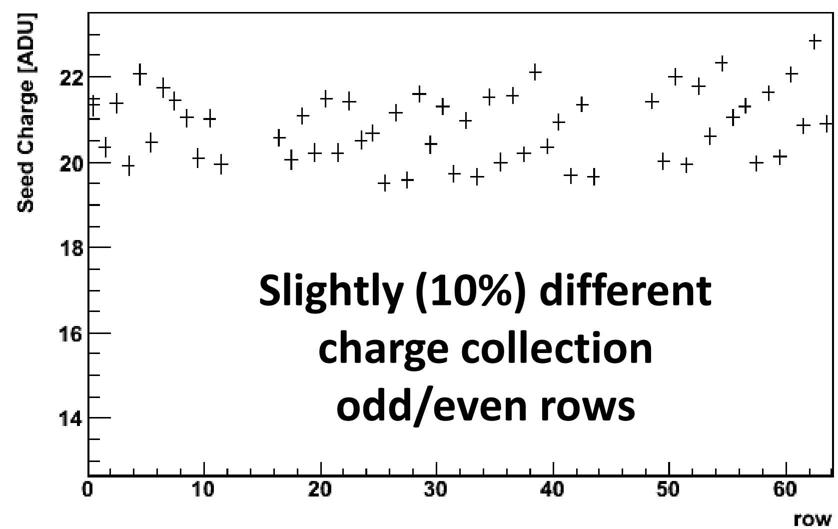
Signal, noise and pixel gain



- Flat noise distribution 0.5 LSB (slightly higher at the edges)

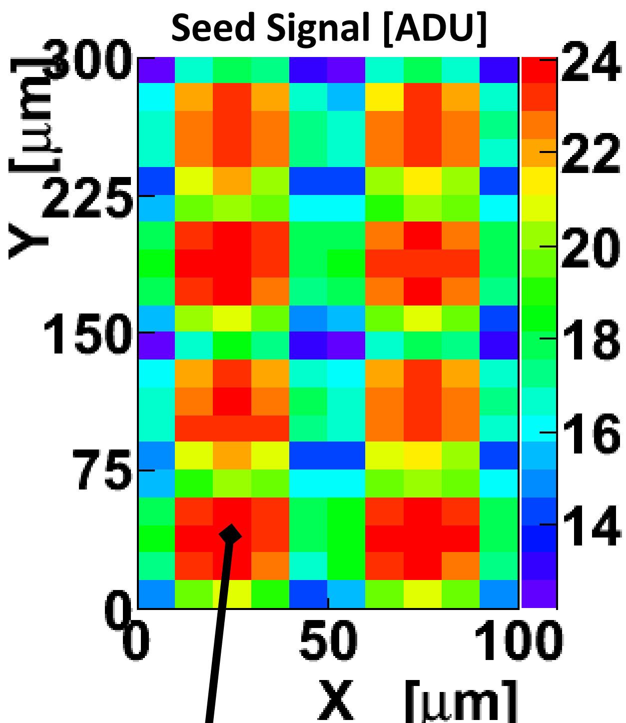


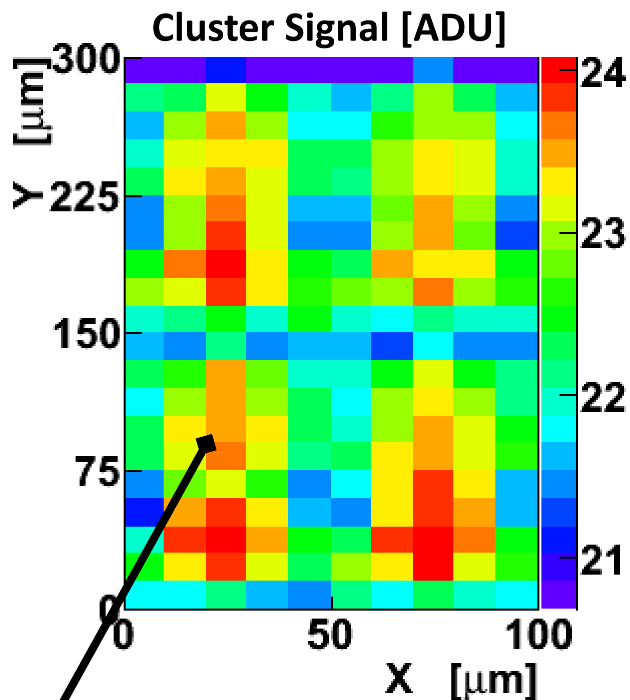


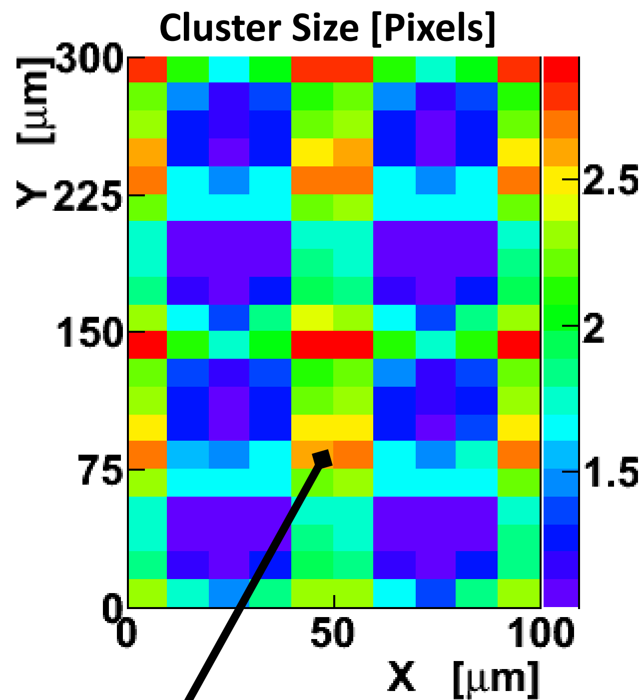


In pixel studies

In pixel studies on a 2x4 pixels area of the matrix







Slightly less charge collection

Charge sharing at pixel edges

Maximum seed signal at the pixel center

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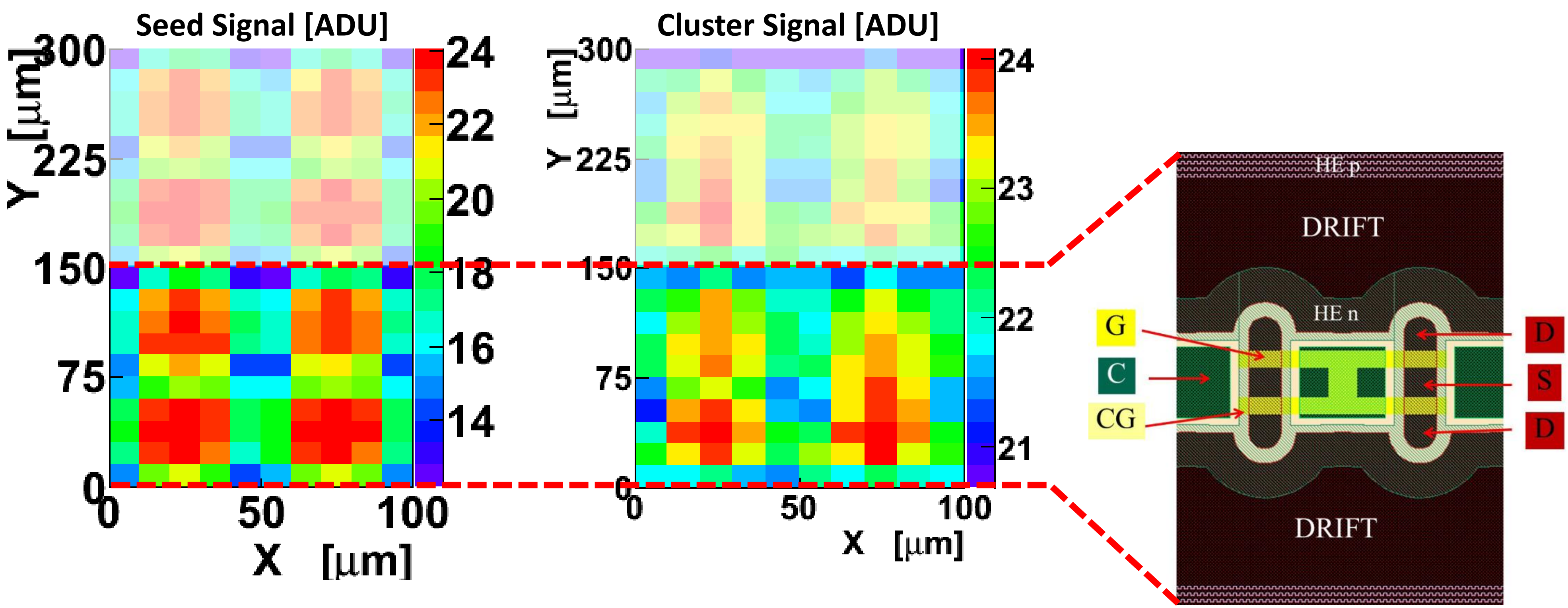
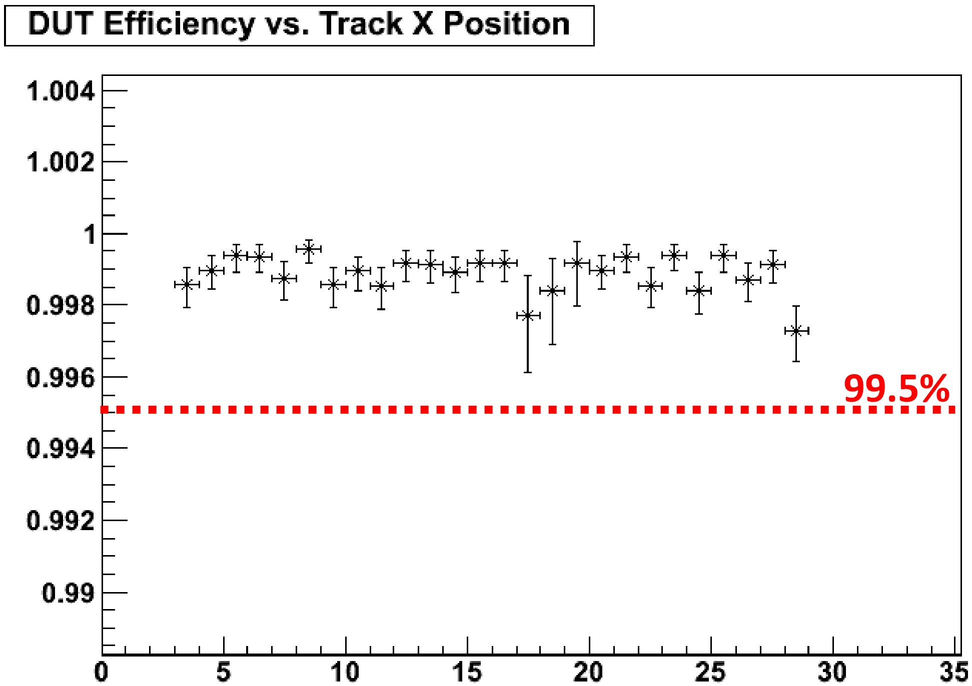
In pixel studies

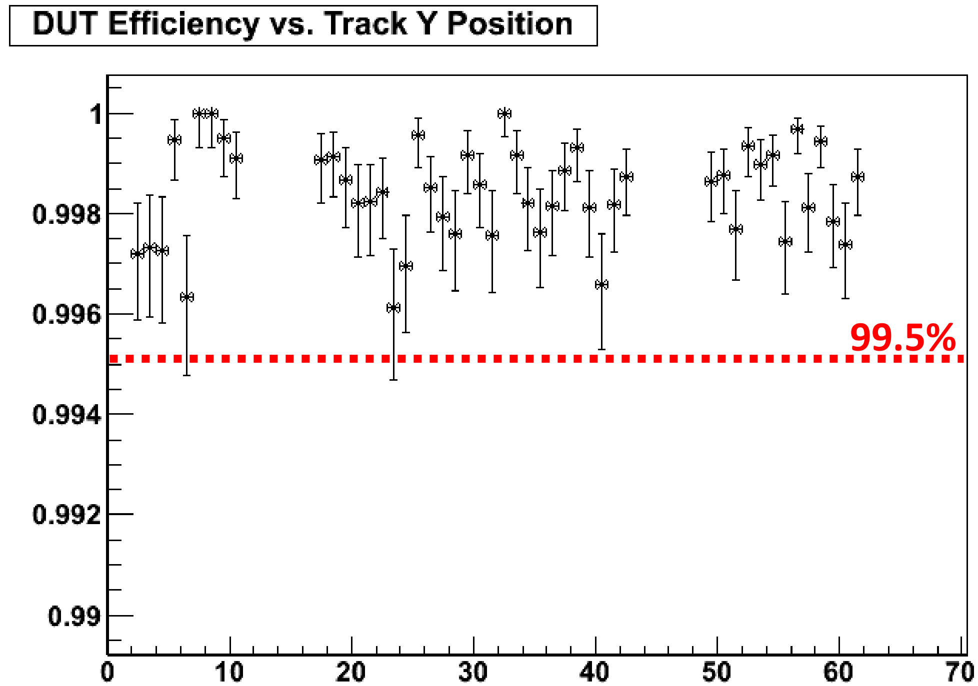
In pixel studies on a 2x4 pixels area of the matrix



Slightly different charge collection odd/even rows
↘ Under investigation

Efficiency





→ The efficiency is higher, both column and row wise, than 99.5%

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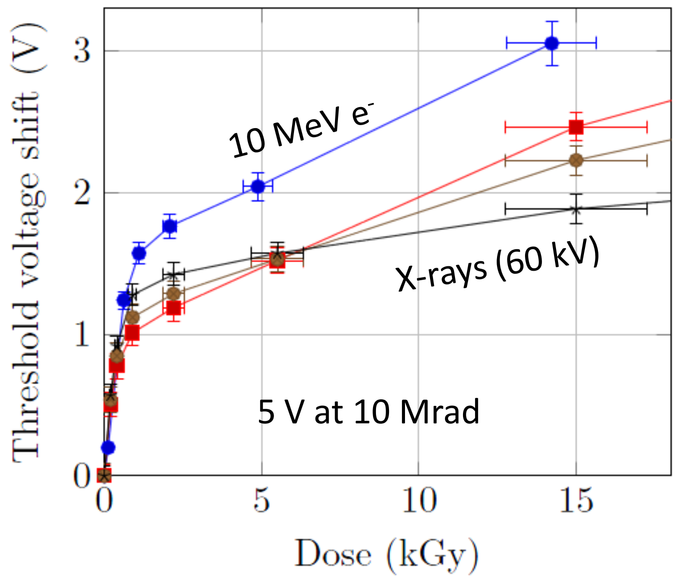
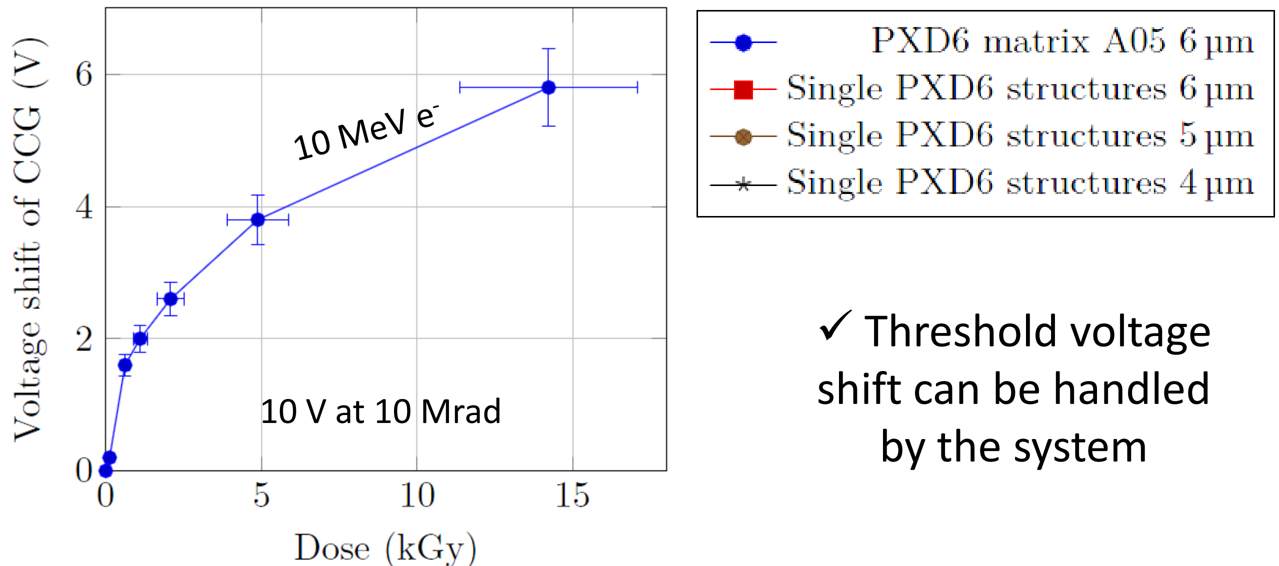
Radiation hardness

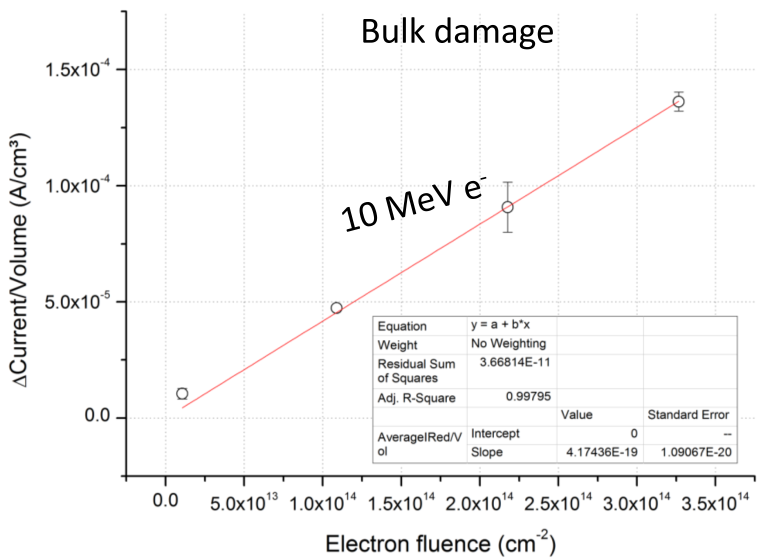
Oxide damage at Gates



Oxide damage at Clear Gates



✓ Threshold voltage shift can be handled by the system



Damage constant: $\alpha_{el}=4.2\cdot10^{-19}$ A/cm

Damage constant: $\alpha_{n}=4.0\cdot10^{-17}$ A/cm

→ Hardness factor is lower than expected

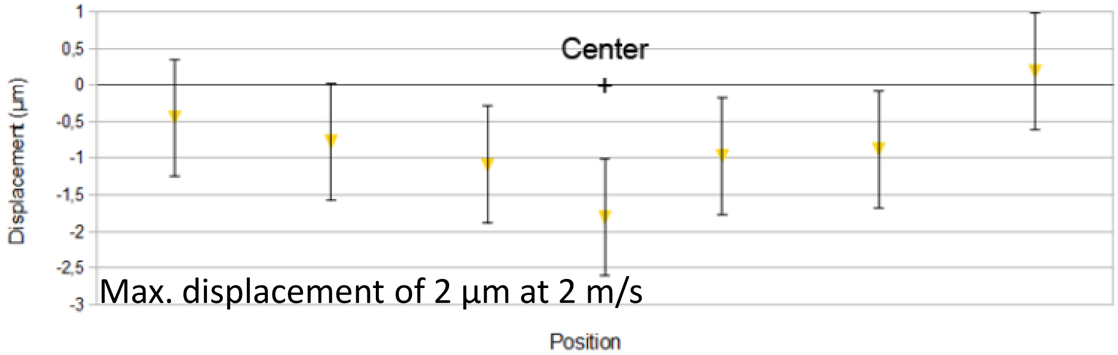
$$\kappa_{meas}=\frac{\alpha(10MeVe^-)}{\alpha(1MeVn)}=0.014$$

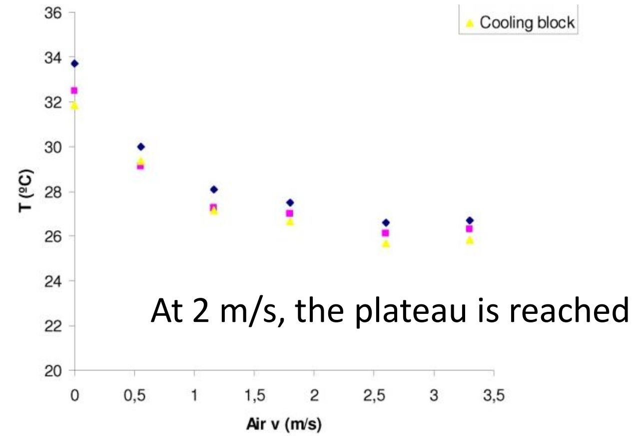
$$\kappa_{theo}=\frac{NIEL(10MeVe^-)}{NIEL(1MeVn)}=0.06$$

Negligible contribution (<400 e^-) at T^{room} after 10 Mrad (Internal Gate: 40000 e^-)

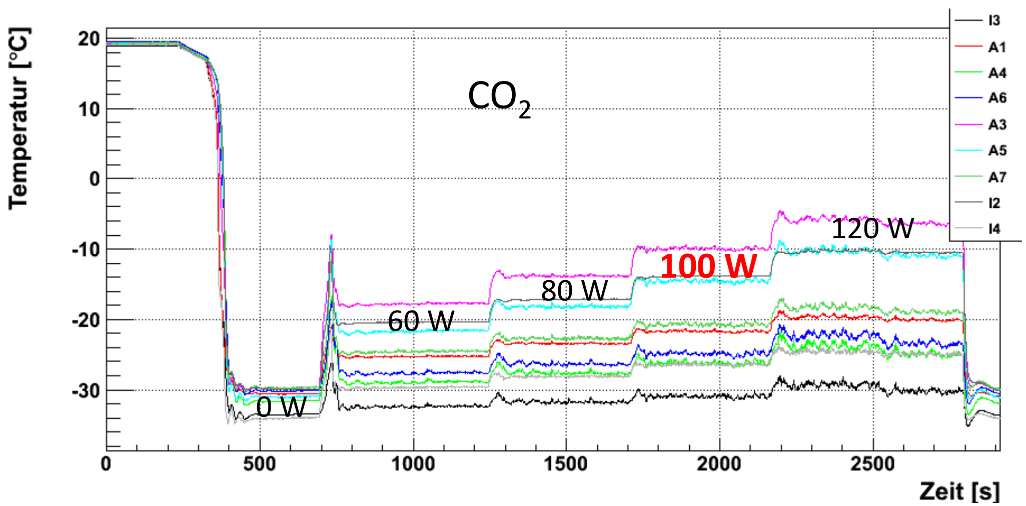
✓ Relaxed bulk damage

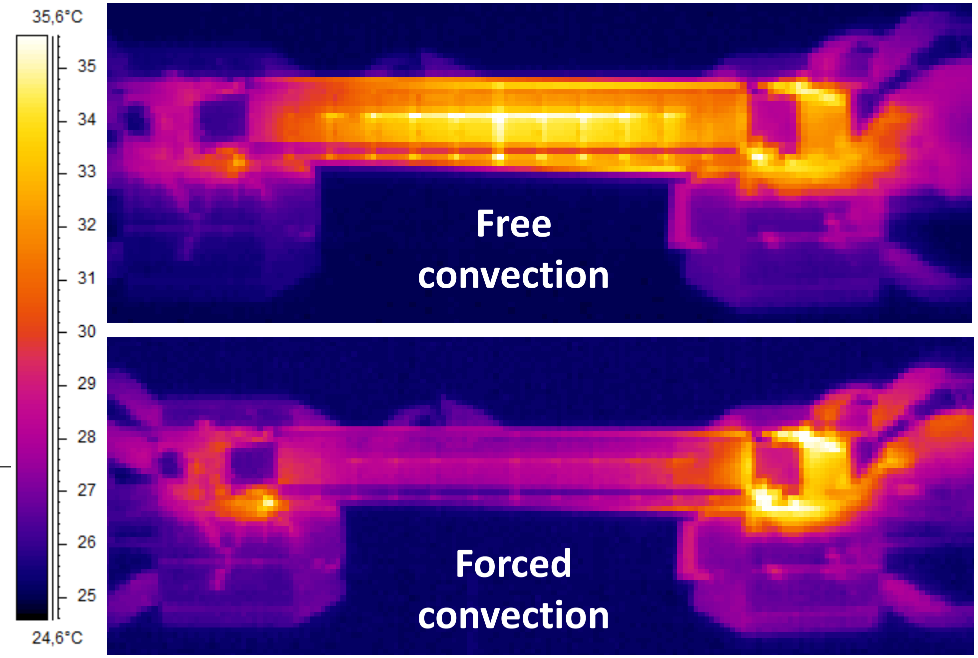
Thermo-mechanical measurements





The ultra low mass cooling system of the Belle II DEPFET detector. P. Ruiz and C. Marinas for the DEPFET Collaboration. Poster session.





Cooling proof of principle

Summary

- A new super flavour factory, SuperKEKB, is currently being built at KEK (Japan)
- To fully exploit the high luminosity, the detector will be upgraded (Belle II)
- The pixel detector will be made of DEPFET sensors
  → Excellent single point resolution (10 μm), high SNR (>35), low power consumption (<0.1 W/cm^2), low material budget (<0.2X_0/layer), radiation hardness (10 Mrad)
- The DEPFET PXD entered the construction phase
  - All readout ASICs and radiation hard sensors are produced and being operated in a close to final version
- Many aspects not covered in this talk, though in development by the Collaboration

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Thank you

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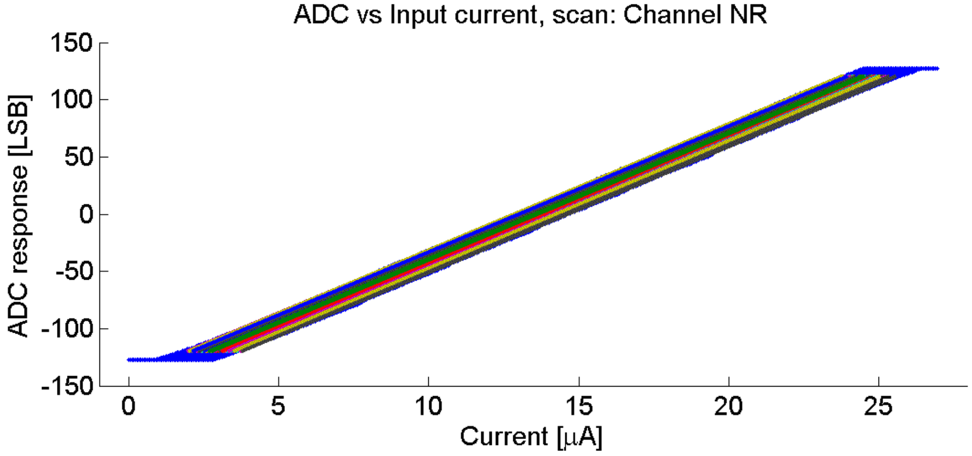
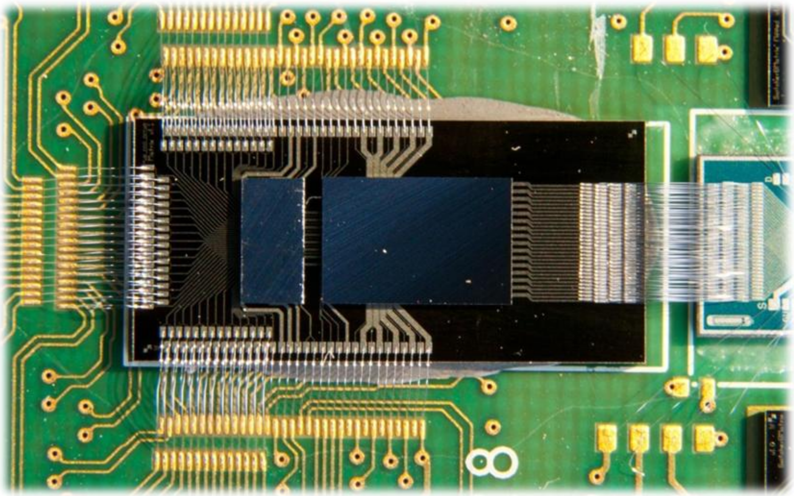
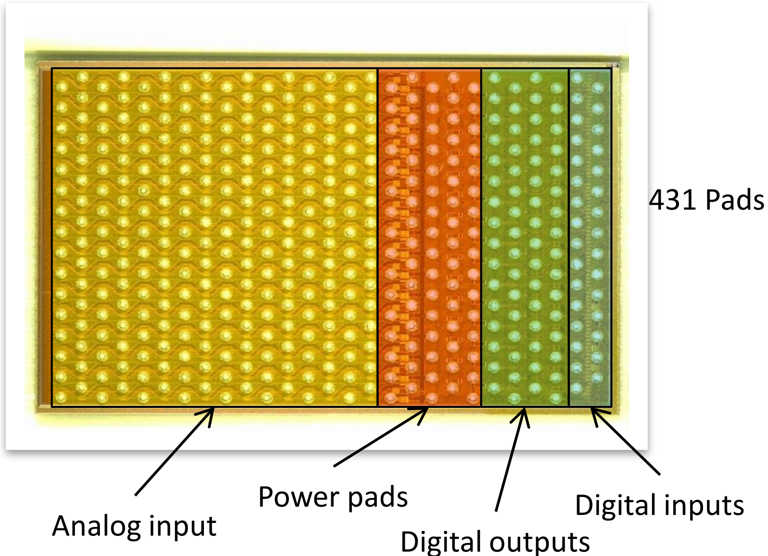
DCDB

Drain Current Digitizer for Belle II

- 512 ADCs
- Cyclic conversion
- 320 MHz clocked
- 100 ns conversion time
- Mean INL < 1.5LSB (Max <2.2 LSB)
- Gain variation < 5% (peak to peak)







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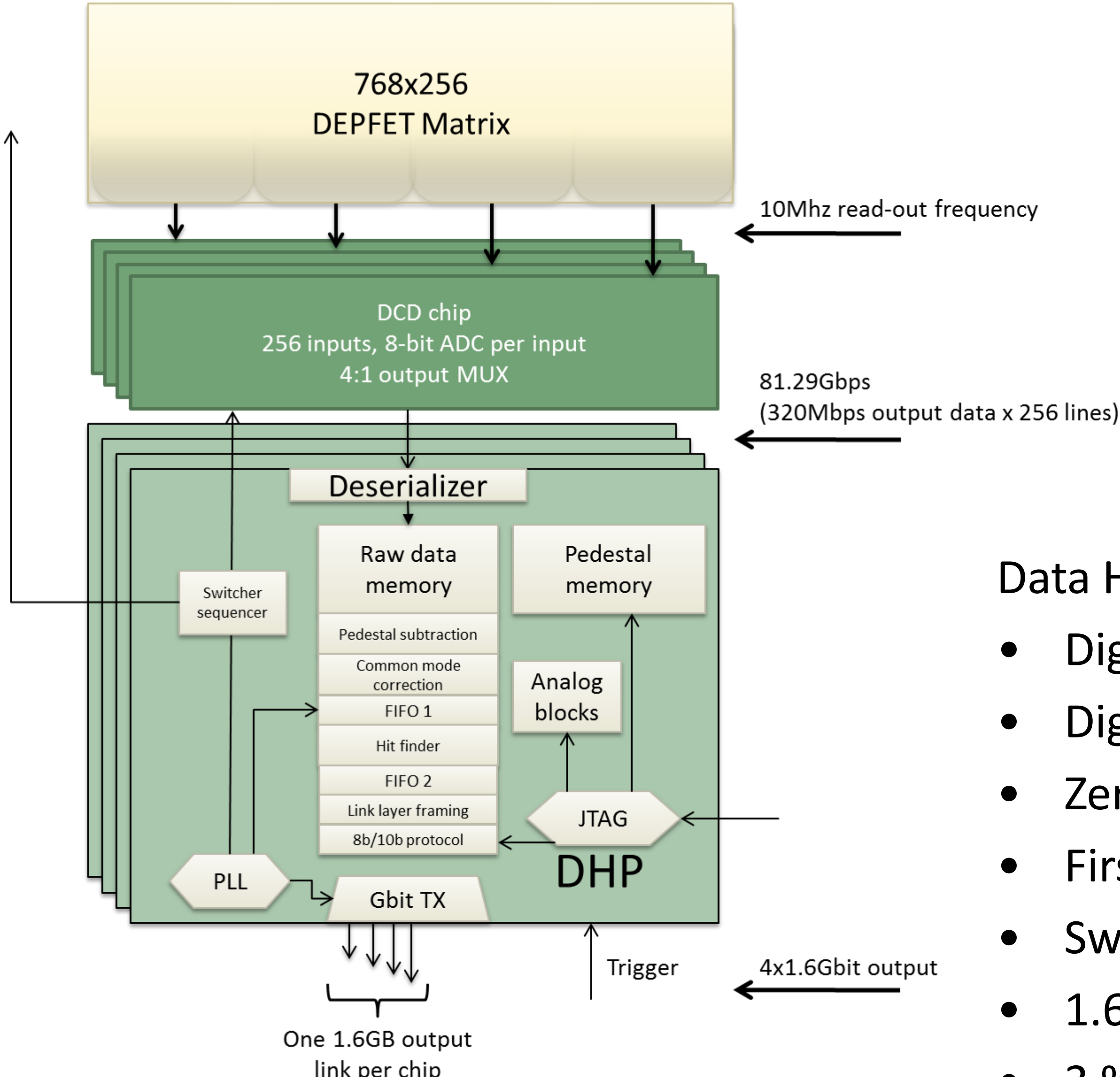
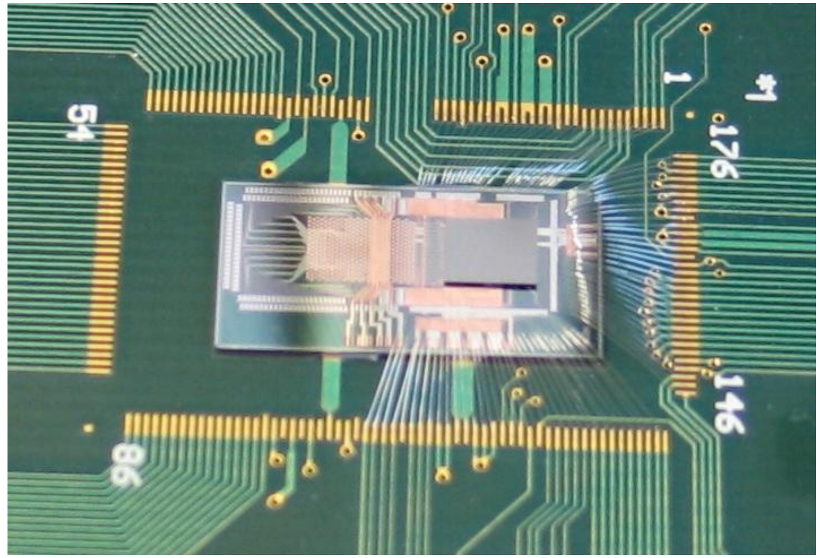
DHP 0.2





Data Handling Processor

- Digital common mode subtraction
- Digital pedestal compensation
- Zero suppression
- First full size chip
- Switcher control
- 1.6 Gb serial link
- 3 % occupancy with <1% data loss

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