University of Glasgow
Experimental Particle Physics

Planar pixel detector module development for the HL-LHC ATLAS pixel system

Richard Bates

On behalf of the UK ATLAS upgrade collaboration

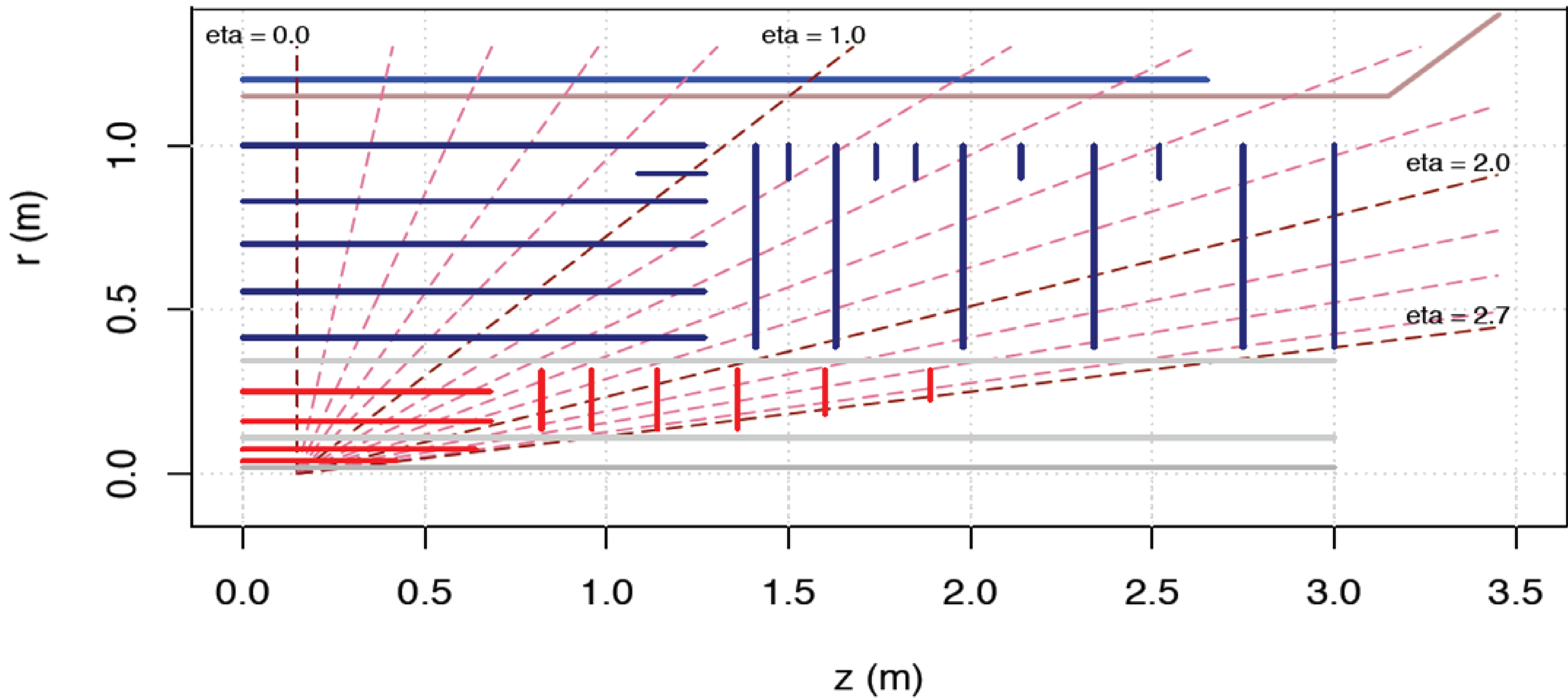
Contents

- Introduction/Motivation
- Sensor wafer design and device selection
- Single chip modules
- Quad module
- Future work
  - TSVs
  - Multiplexing and redundancy
- Summary

Introduction

- Luminosity upgrade to LHC driven by
  - Desire to reduce statistical uncertainties
  - Desire to increase search for new physics at higher energy via lower probability events
- Luminosity increase by an order of magnitude
  - Corresponding increase in occupancy (depends on luminosity leveling)
  - Radiation damage to a maximum of 10^{16} 1MeV n_{eq}/cm^2

- 4 pixel barrel layers
  - Radius from 39 mm to 250 mm
  - Z: ±449 mm to ±694 mm (outer 2 layers)
- 6 Pixel disks
  - R_{inner} = 150 mm
  - R_{outer} = 315 mm
  - Z: 820 mm to 1890 mm



Pixel system for HL-LHC

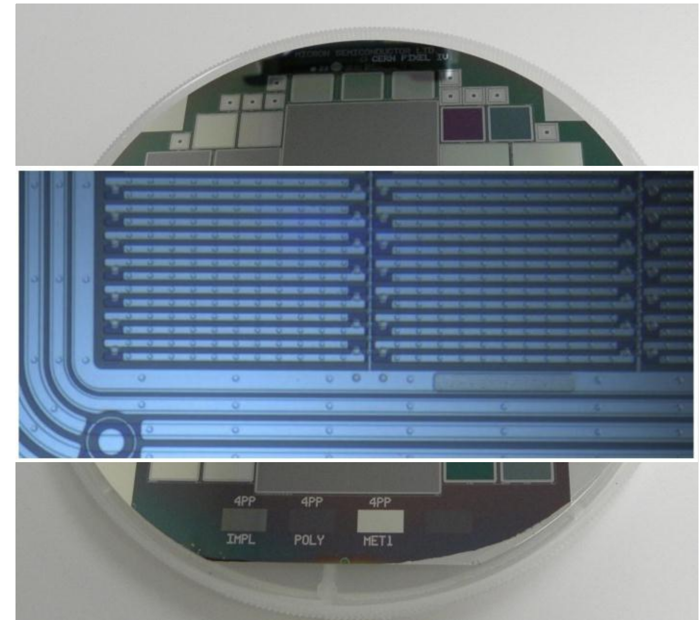
- Pixel modules should be
  - Large with high active fraction
    - Reduced material
    - Reduced cost of assembly
  - Thin
    - Reduced material
    - Reduced power from sensor
  - Low power ROIC
    - Reduce cooling material
  - Small pixel size
    - Cope with increased occupancy
  - High rate multiplexed data
    - Reduce pile-up
    - Reduced data links
  - Serial power
    - Reduced service material

- 2 Inner Barrel layers
  - Sensors
    - All sensor materials possible
    - 150 µm silicon or thinner
  - Pixel size 25 µm x 150 µm
  - ROIC thickness 150 µm
  - ToT = 0-8 bits
  - 2x1 and 2x2 chip modules
  - 2x2 sensor = 33.9 mm x 40.6 mm
  - Data rate as high as 2 Gbit/s per module
- 2 outer Barrel layers / **Disks**
  - Sensor
    - planar n-in-p
    - 150 µm
  - Pixel size 50 µm x 250 µm
  - ROIC thickness 150 µm
  - ToT = 4 bits
  - 2x2 (Quad) and 2x3 (Hex) chip modules
  - Data rates of 640 Mbit/s per module

Sensor wafer design

- 2 wafer designs fabricated at Micron Semiconductor Ltd.
  - All 6 inch 10k Ohm-cm FZ material
  - n-in-p sensors with p-spray isolation
  - 300 µm and 150 µm thick wafers made

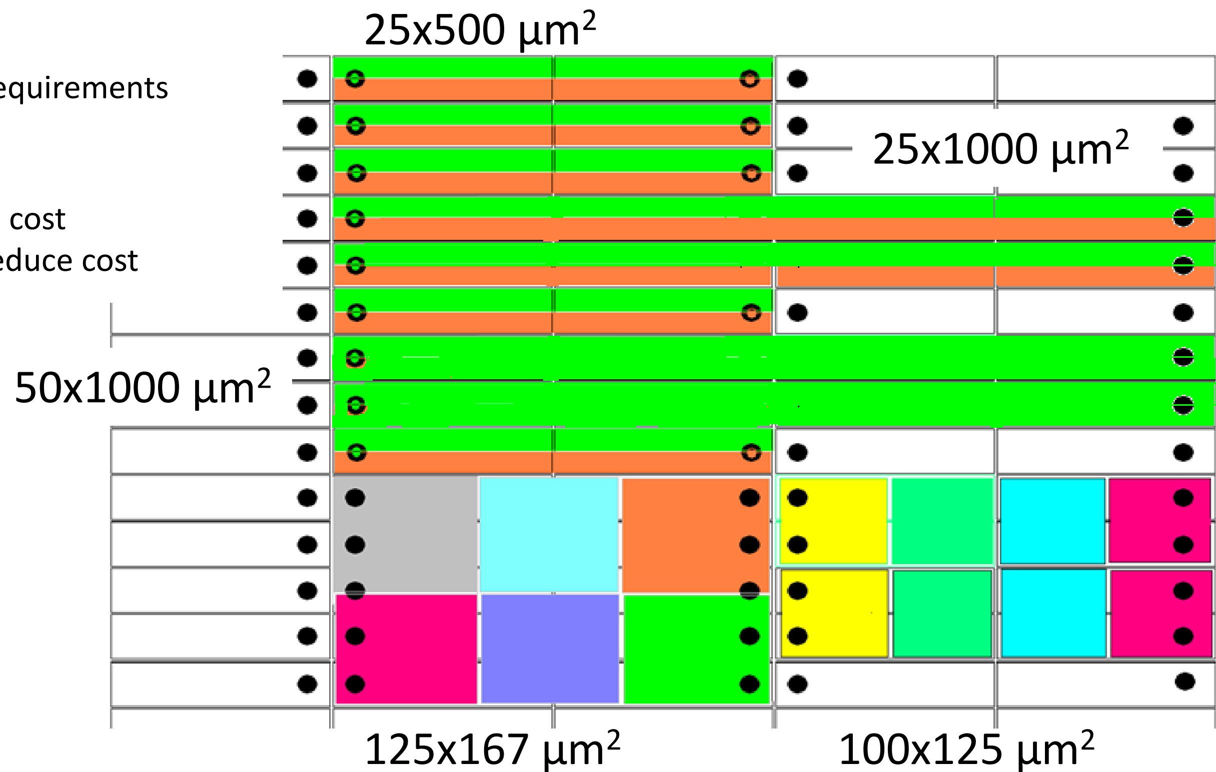
  (Only assembled 300 µm devices at VTT to date)
  - V_{fd} = 70 V
- CERN Pixel II wafer
  - Singles with differing guard ring designs
  - Including slim edge – 200 µm wide guard rings
- CERN Pixel IV wafer
  - 5 quad and 8 singles FE-I4 sensors
  - Quads include slim edges design
  - Singles includes a 25 x 500 µm implant device



The next wafer design

- Test vehicle for different layouts and structures
- All compatible with FE-I4
- Disks
  - Square pixels may be an advantage for tracking
- Large radius use strips
  - Lower position resolution requirements
  - Lower power and cost
- Long large area implants
  - Turn off some pixels to save cost
  - Lower density flip-chip to reduce cost

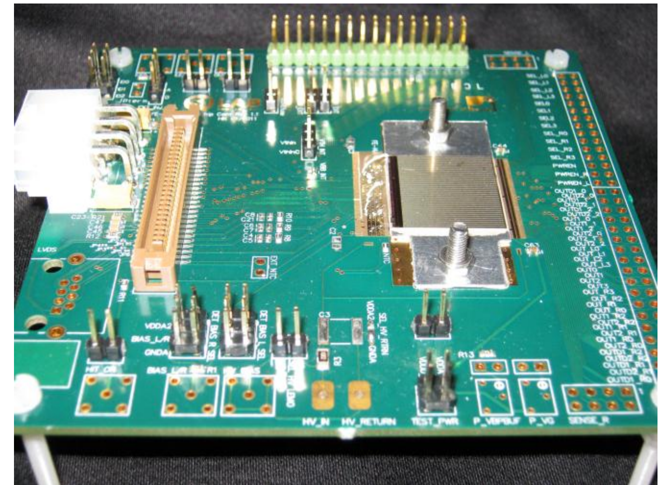
- Bias dot optimization to increase detection efficiency after high radiation dose
- Poly-silicon bias structures
  - Remove bias dot completely
  - AC couple detectors possible



Single chip assemblies

- UBM and PbSn bumps deposited on FE-I4 wafers
  - Visually inspected after bumping
  - One wafer thinned to 200um post bumping
- 300um thick sensors
  - UBM deposited at VTT
  - IV measured post dicing at VTT before assembly
- 15 single assemblies fabricated at VTT
  - 5 single assemblies mounted on SCC and tested
  - 10 to be irradiated in PS and Ljubljana neutron reactor

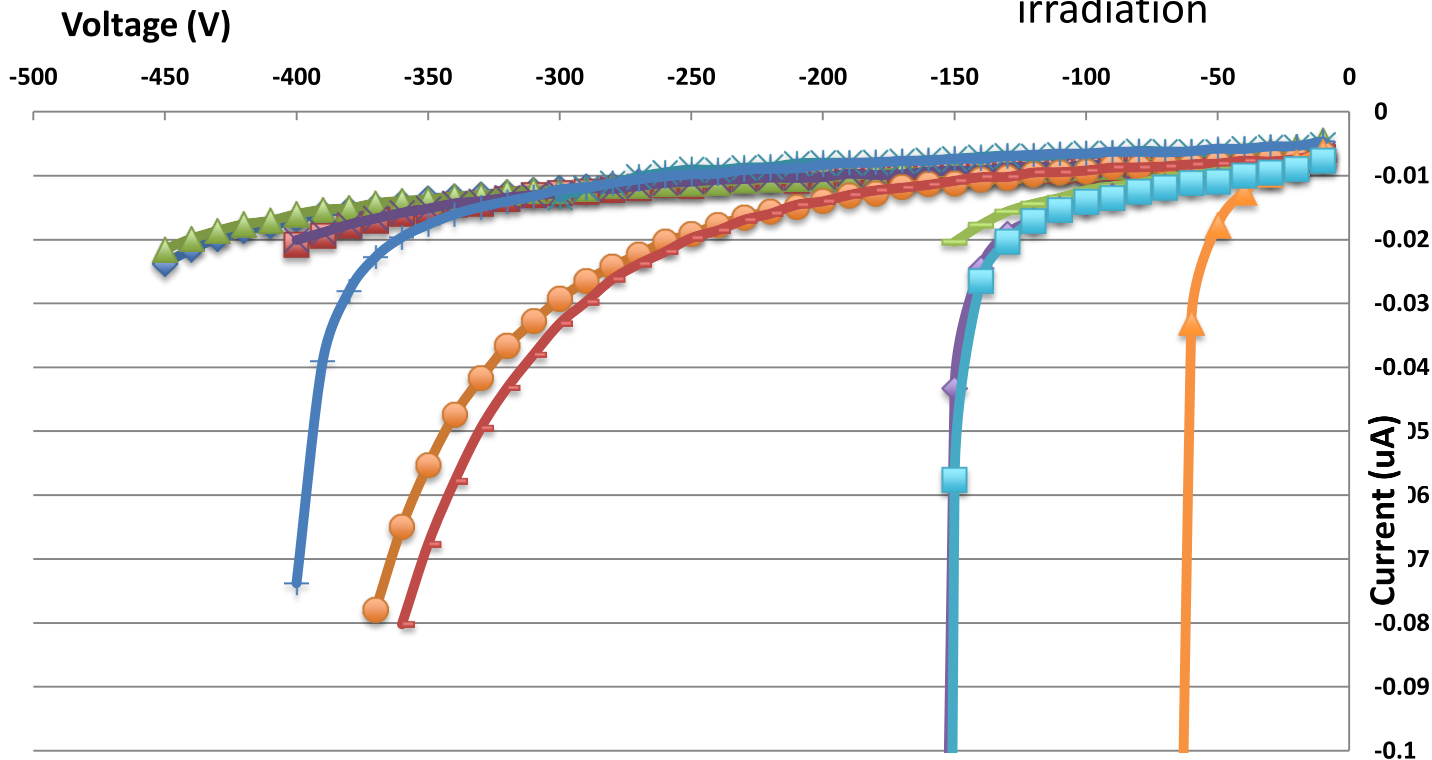
- DAQ is USBPix single chip system from Bonn
- Devices tuned for in-time thresholds 3200e and 1600e
- Devices characterized to find
  - Noisy pixels
  - Merged bumps
  - Disconnected pixels



Assemblies IV characteristics

- IV measured
  - On wafer after fabrication
  - After UBM & dicing
  - As assembies
- IV same post assembly to pre-flip chip

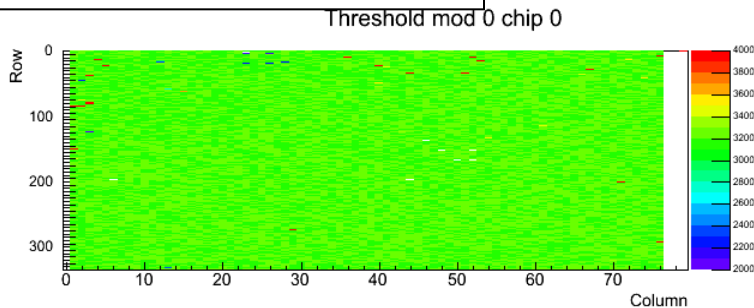
- Current < 2nA/cm^2 @ 20C and 90 V
- Some devices current < 1 µA for 1000V
- Lower breakdown for slim edge devices
  - Still above V_{fd} = 70V
  - HV performance improves after irradiation

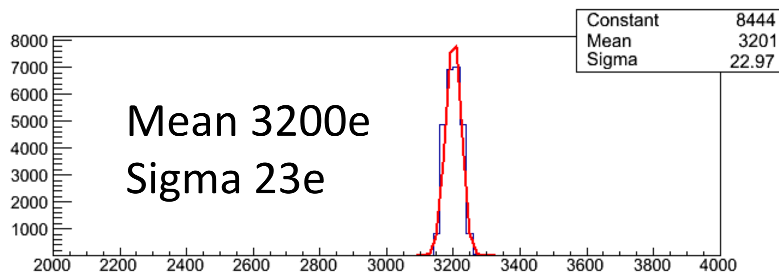


Tuning of assemblies

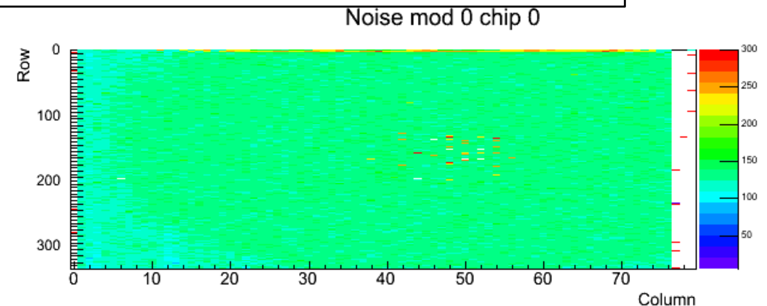
- Each device tuned for
  - in-time threshold = 3200 e
  - ToT = 8 for 20,000e
- Then down to Vth = 1600e
- Operated in forced air flow at 20C for all tests
- Devices appear to work well

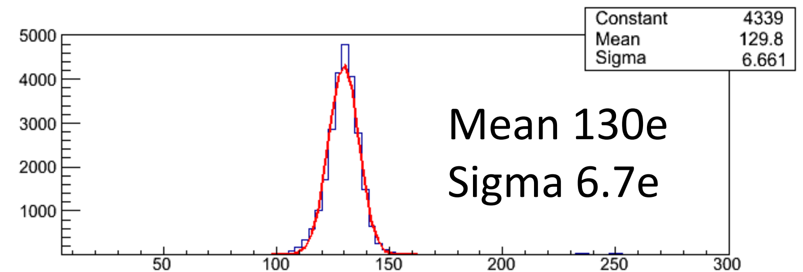
Threshold s-curve mean





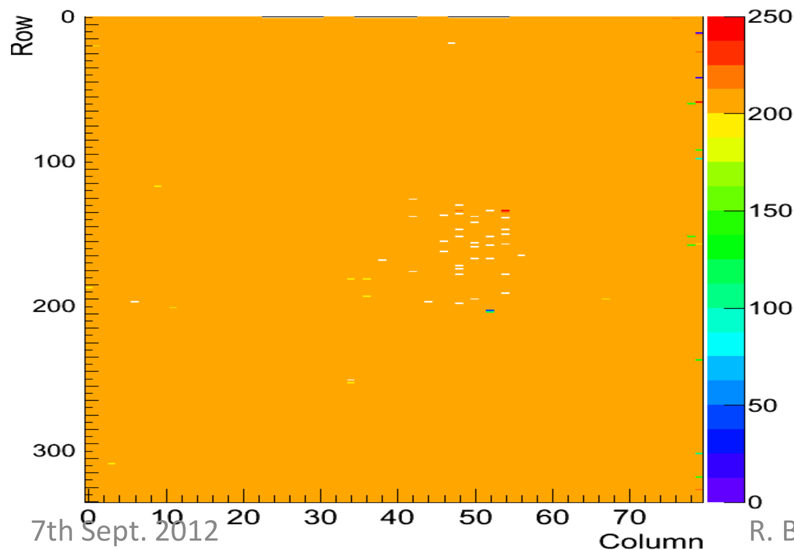
Assembly noise, s-curve sigma



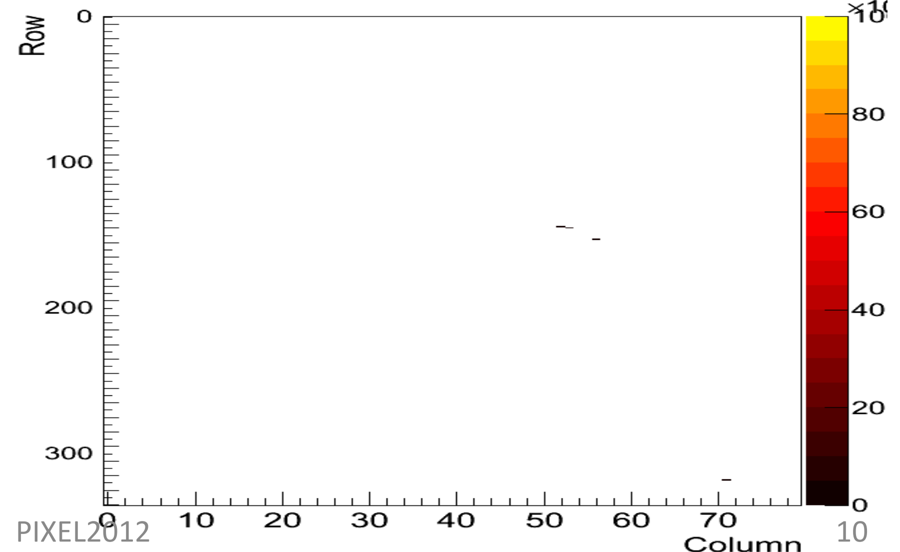


Characterization

- Analogue scan to find dead pixels
  - No dead pixels
  - Expect for 1 assembly
    - Dead pixels = 35

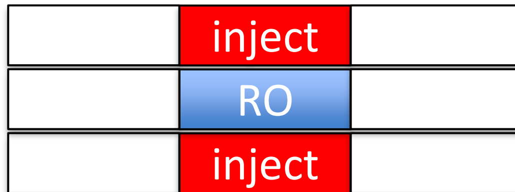


- Stuck pixel scan
  - No stuck pixels except for 24 in row 0, as expected
- Noise occupancy scans
  - Average of 3 pixels per device



Merged bumps

- Cross-talk measured by
  - Applying injection and readout mask

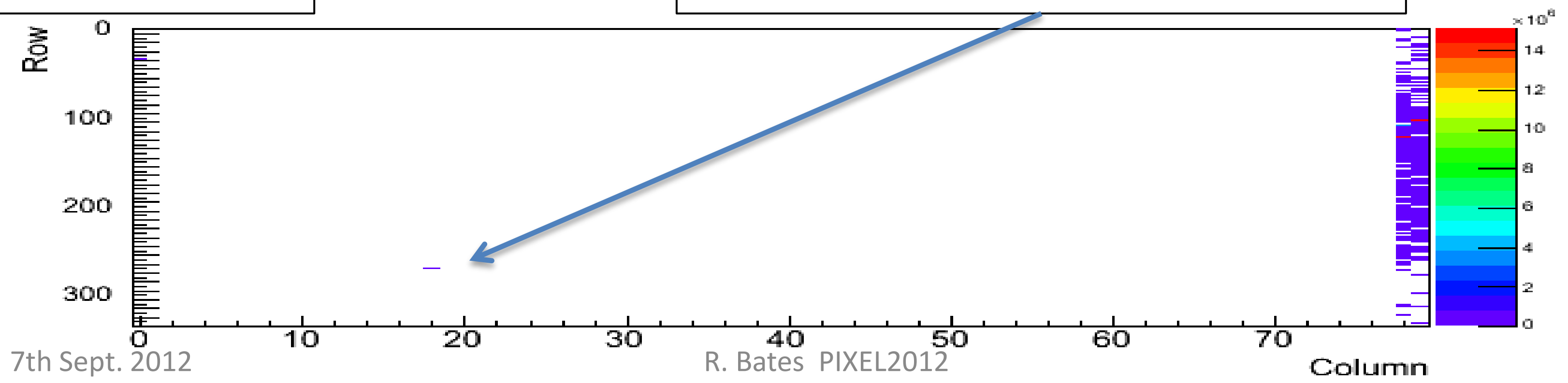


  - Inject large charge w.r.t. in-time threshold

- There is no cross-talk between pixels for an un-bonded FE-I4
  - Cannot inject enough charge
- For fully depleted detector
  - No cross-talk at Vth = 3200e
- If cross talk then due to merged bumps
- Average number of merged bumps = 2

S-curve mean 100V

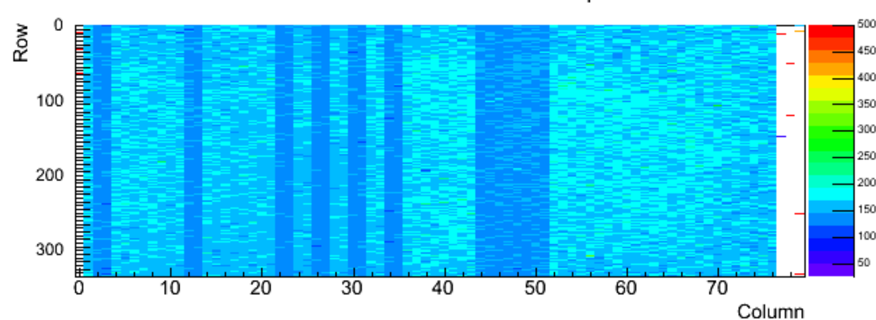
Cross talk here due to merged bump

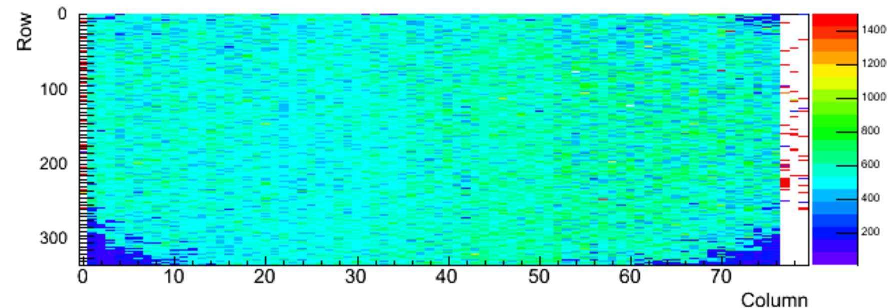


Un-bonded Channels
A: Pixel noise

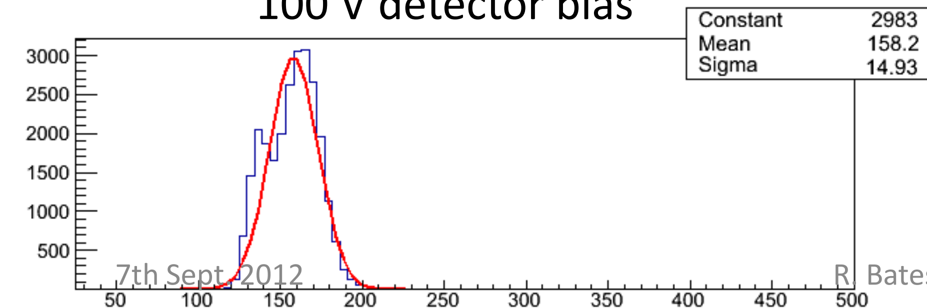
Threshold scan for high and 0 V detector bias

- At high detector bias noise over matrix approximately constant
  - 150e for this device
- Observe low noise pixels
  - No detector capacitance load
  - Ignore dead/masked pixels

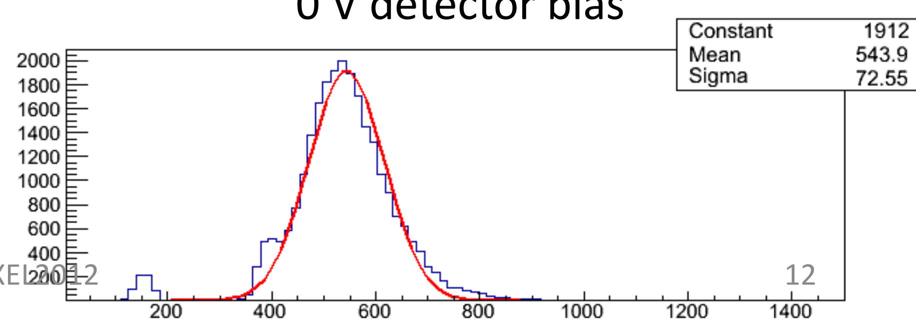




100 V detector bias

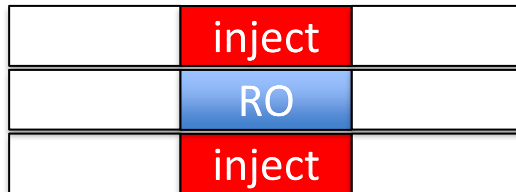


0 V detector bias



Un-bonded channels
B: Pixel Cross-talk

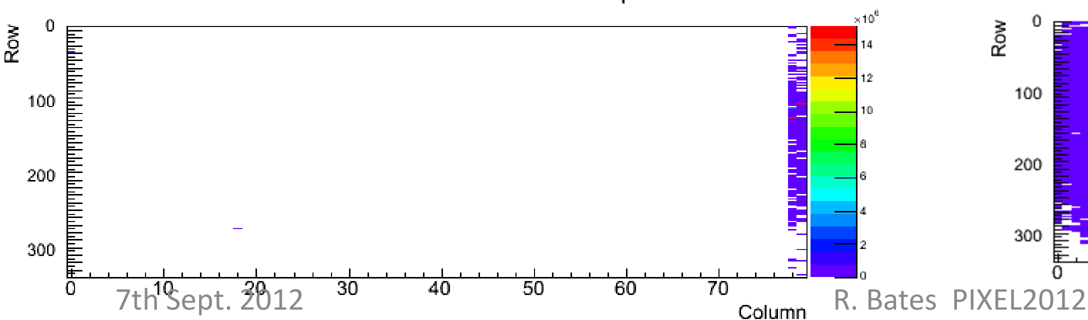
- Cross-talk measured by
  - Applying injection and readout mask



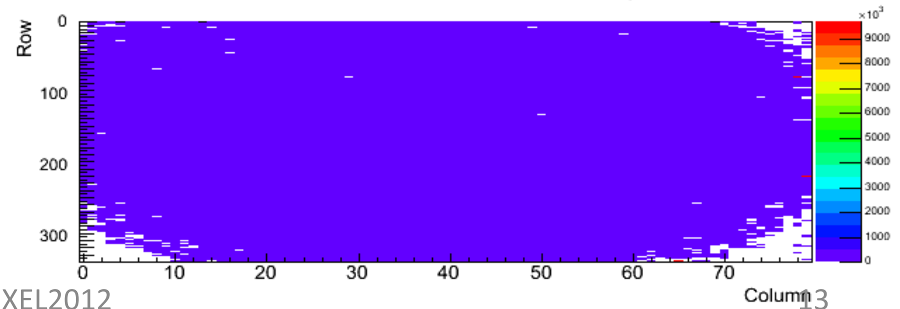
  - Inject large charge w.r.t. in-time threshold

- There is no cross-talk between un-bonded pixel channels
  - Cannot inject enough charge
- For 0 V bias
  - Pixels coupled via detector capacitance
  - ➢ cross-talk high
  - Un-bonded channels those with no cross talk

S-curve mean 100V



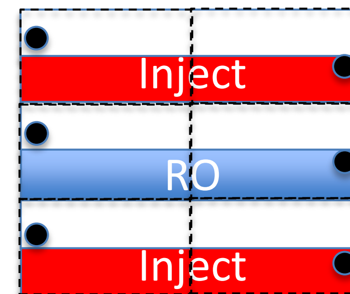
S-curve mean 0V



Cross-talk with 25 x 500 um pixel device

- Never register cross-talk with HV off
- Due to implant design don't inject signal in neighbouring pixels
- Inter-pixel capacitance about the same as standard pixel due to implant design
  - Measured noise is the same for both 25x500 and 50 x 250 sensor designs

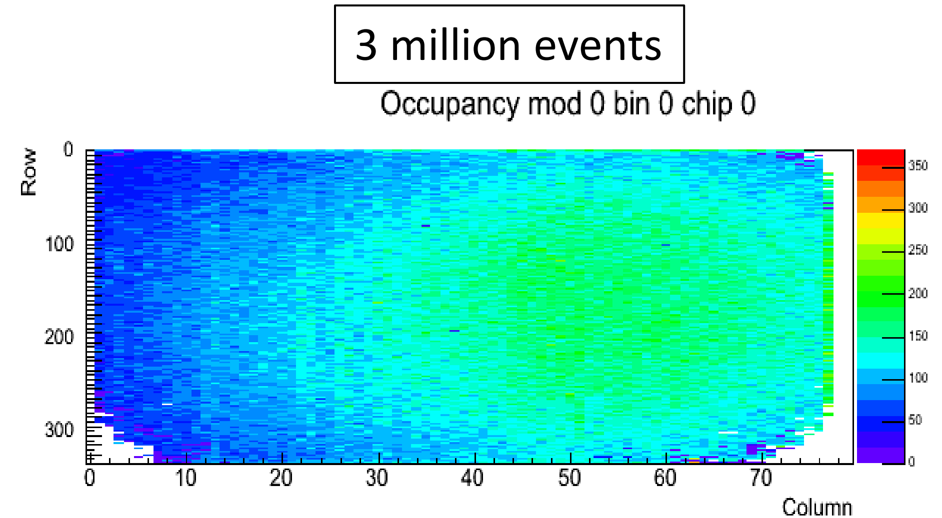
- Implants and ROIC pixels

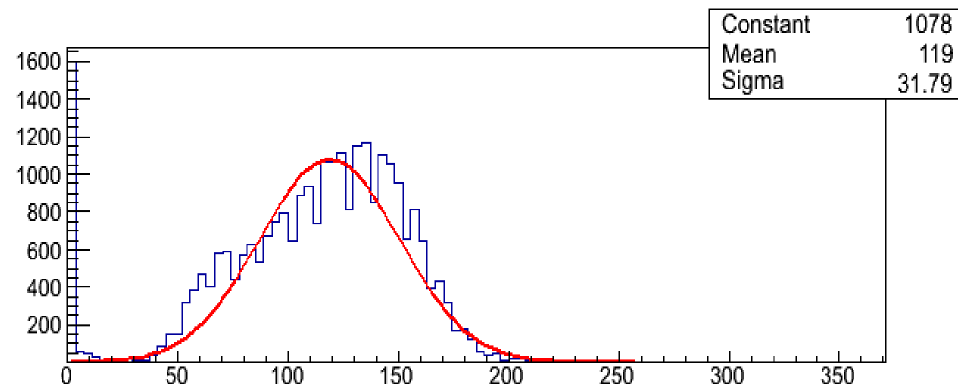


Un-bonded channels
C: Am-241 Gammas

- Flood illuminate sensor with 60keV gammas from Am-241
- Use HitOr (hit in a pixel) output from FE-I4 for self trigger
  - Required to remove stuck/noise pixels
- Non-responding pixels are not bonded

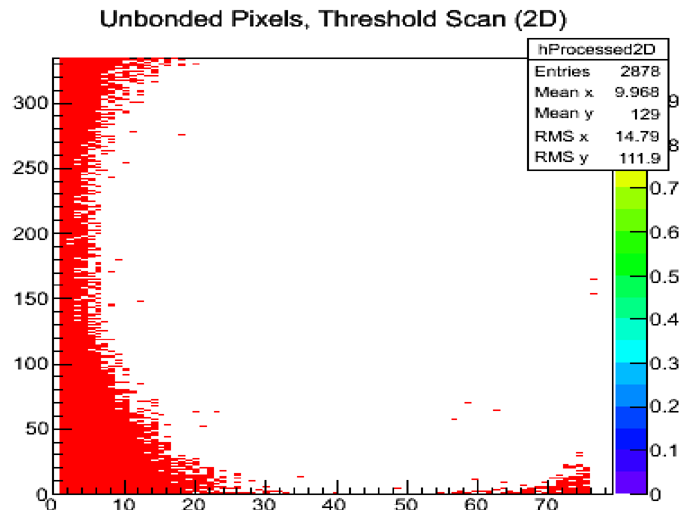
3 million events





Disconnected bumps

- The 3 methods gave similar results
  - Agreement within 4%
- All assemblies are non-perfect
- Large areas of non-boned pixels at the corners & edges
  - Have 3% to 66% open bumps



Bump Process Flow

1. Deposit UBM and bumps on ROIC
2. Thin ROIC to 200 µm / Diced
3. On vacuum jigs perform flip-chip for tack bond
4. Re-flow in reducing atmosphere in oven (260C) unsupported assembly
   - Self-align bumps
   - Obtain good electrical properties

ROIC bows due to non-symmetric layup

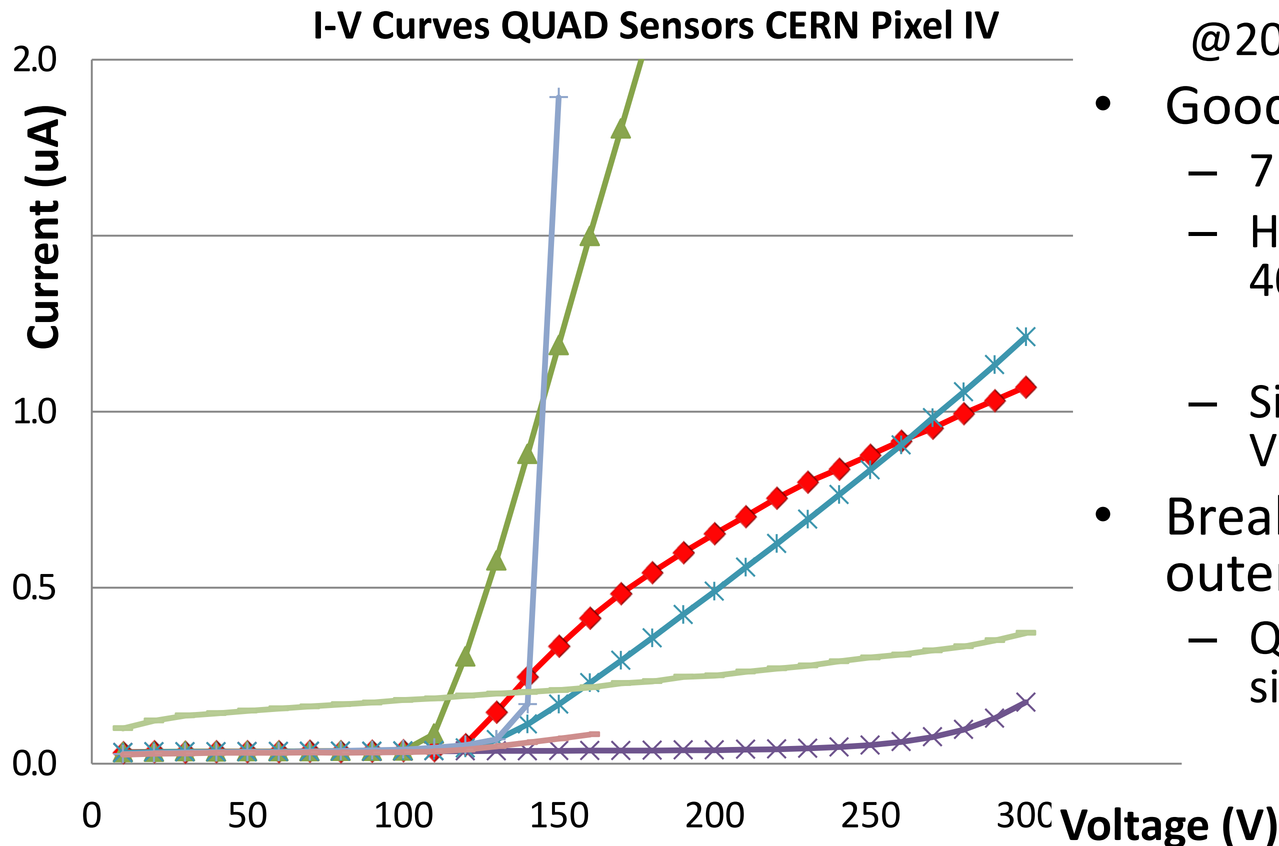
- Thick dielectric layers on top side
- Just silicon on back side

Solution under investigation

- Support wafer technology
- Deposition of balancing dielectric on ROIC

Quad-Sensor selection

- Wafers processed at VTT
  - UBM
  - Dicing
- Characterized at VTT for selection



- Characterized electrically
  - Full depletion by 70 V
  - Current in plateau:

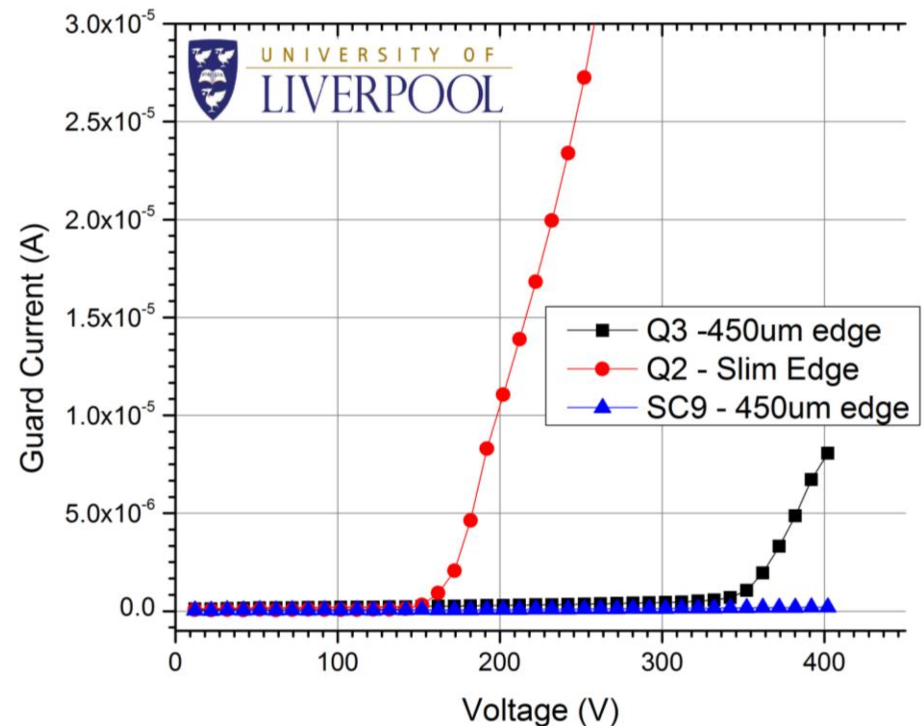
  30 - 40 nA < 3 nA/cm^2 @20C & 90V
- Good yield
  - 7 from 10 hold V_{fd} + 30V
  - HV operation: 5 fine to 400 V

    (I < 2 μA)
  - Singles much better 1000 V operation possible
- Breakdown all at the outer guard-ring
  - Quads more edge than singles

Quad modules

- Test vehicle for module building and testing
- 4 quad modules started
  - 1 with 200 µm ROIC
  - 3 with full thickness ROIC

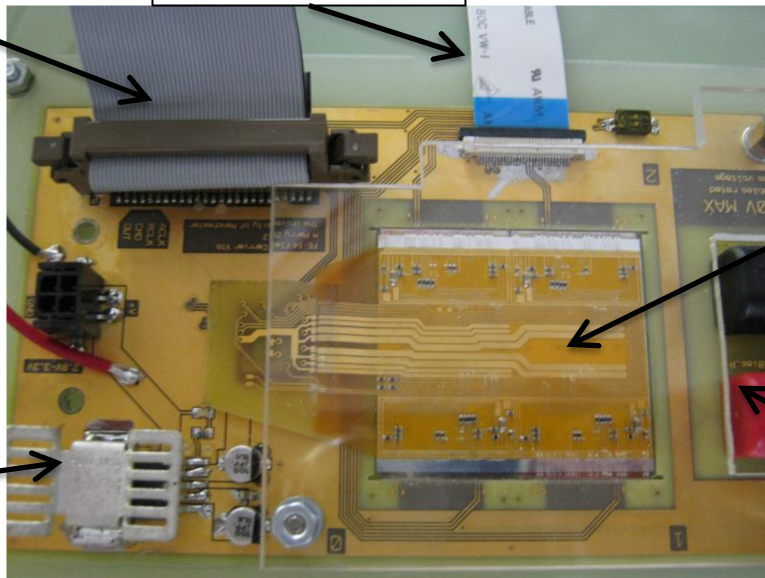
- IV of quad sensor unchanged by flip-chip assembly process



Module assembly

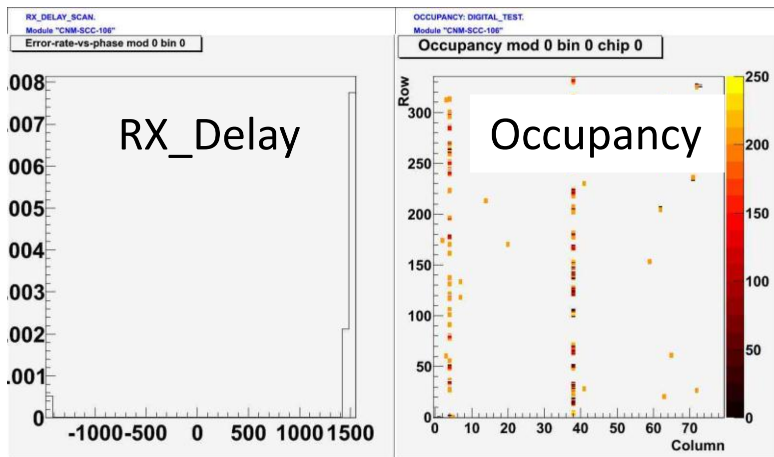
- Kapton based hybrid (from Bonn)
- Glued to sensor
  - Re-use of SCT construction equipment
  - Uses optical alignment to place hybrid relative to ROIC
- Wire bond down to the FE-I4
- Module mounted in carrier PCB and bonded to PCB

- DAQ is single chip USBPix system
- Present flex routes only data lines from one chip
- Decided to route data via carrier PCB
- PCB has switches to select data lines
- Configuration selection done via DAQ and chip address
- ROIC LV generated on support PCB

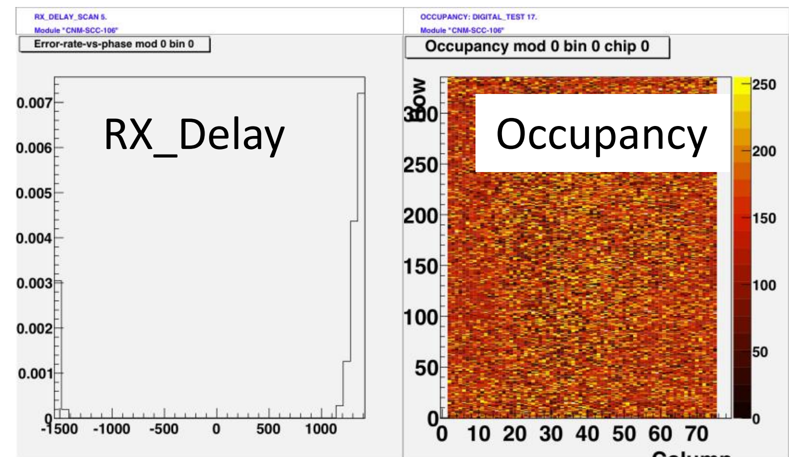


Quad data so far

Chip 3



Chip 4

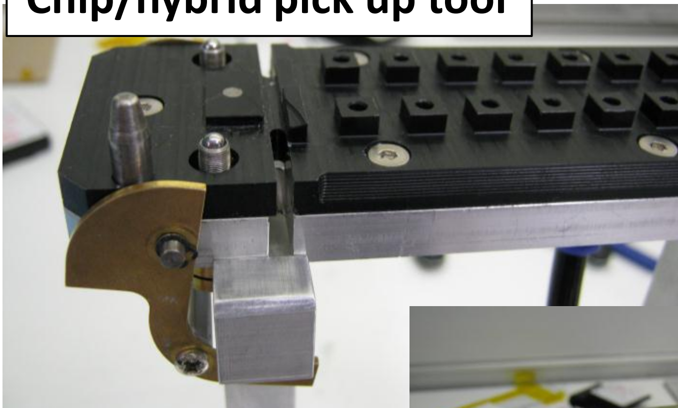


- Data comes off chip/PCB fine
- Configuration of all 4 ROIC done
- Verification of module and support card
- Full device characterization just starting

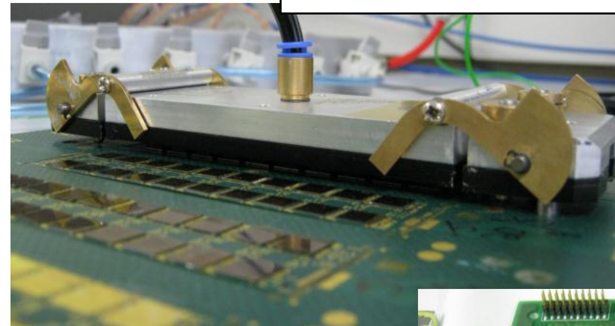
Next steps for quad assembly

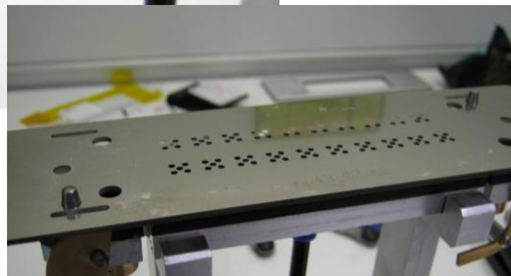
- Quad rigid PCB design taking place in collaboration
  - Simpler module mounting procedure
  - PCB will have 4 RJ45 connectors to allow true 4 chip RO with SLAC developed RCE/HSIO DAQ system
- Design of a flex system based on flex/rigid hybrids
  - Successfully being used for ATLAS strip tracker upgrade
  - Very fast and accurate
  - PCB has precision holes for alignment
  - Stencil application of glue
  - Test connectors cut off at end of build

Chip/hybrid pick up tool

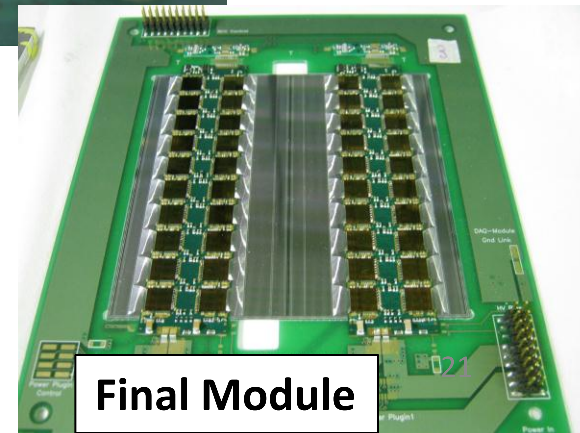


Chip attachment to hybrid





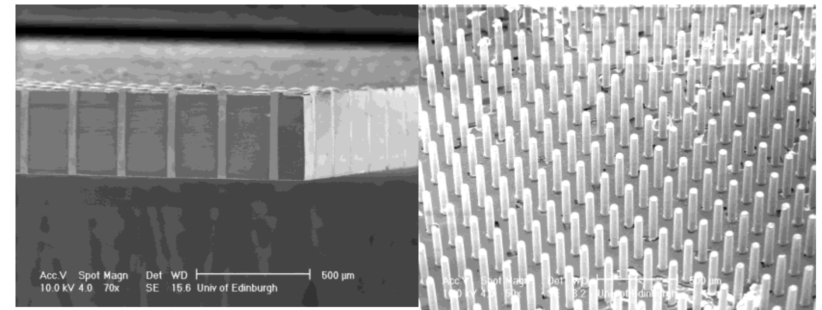
Stencil for glue application to ROIC/Hybrid



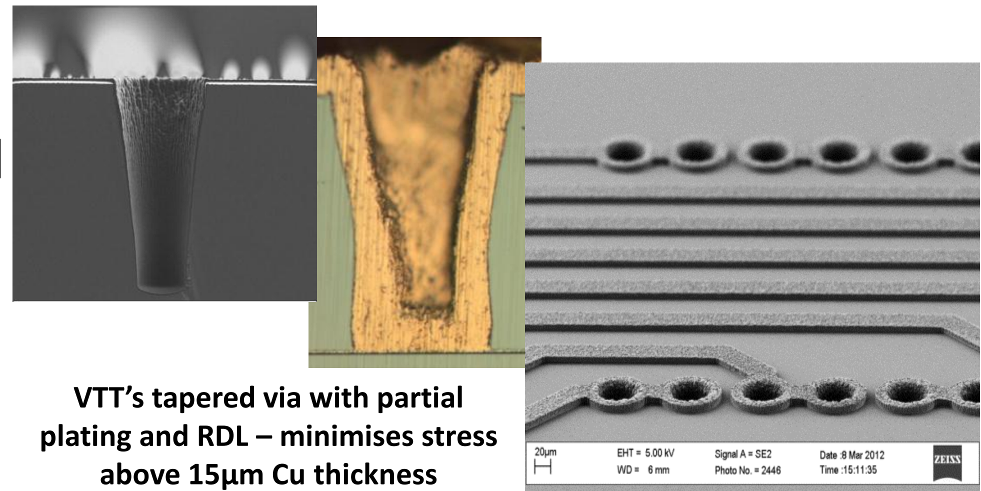
Final Module

Other module/future work
Through Silicon Vias (TSV)

- Reduction of dead area via removal of wire bond pads
- 4 side buttable assemblies
- Sensor must be active over EOCL region
  - Sensor design taking place
- TSV last process being investigated
- High aspect ratio (5:1) vertical side wall TSV from front side
  - Allows TSV monitoring before wafer thinning
  - Non-critical end point (width increase due to over etch)



Scottish Microelectronics Centre's high yielding Cu ECD TSV's



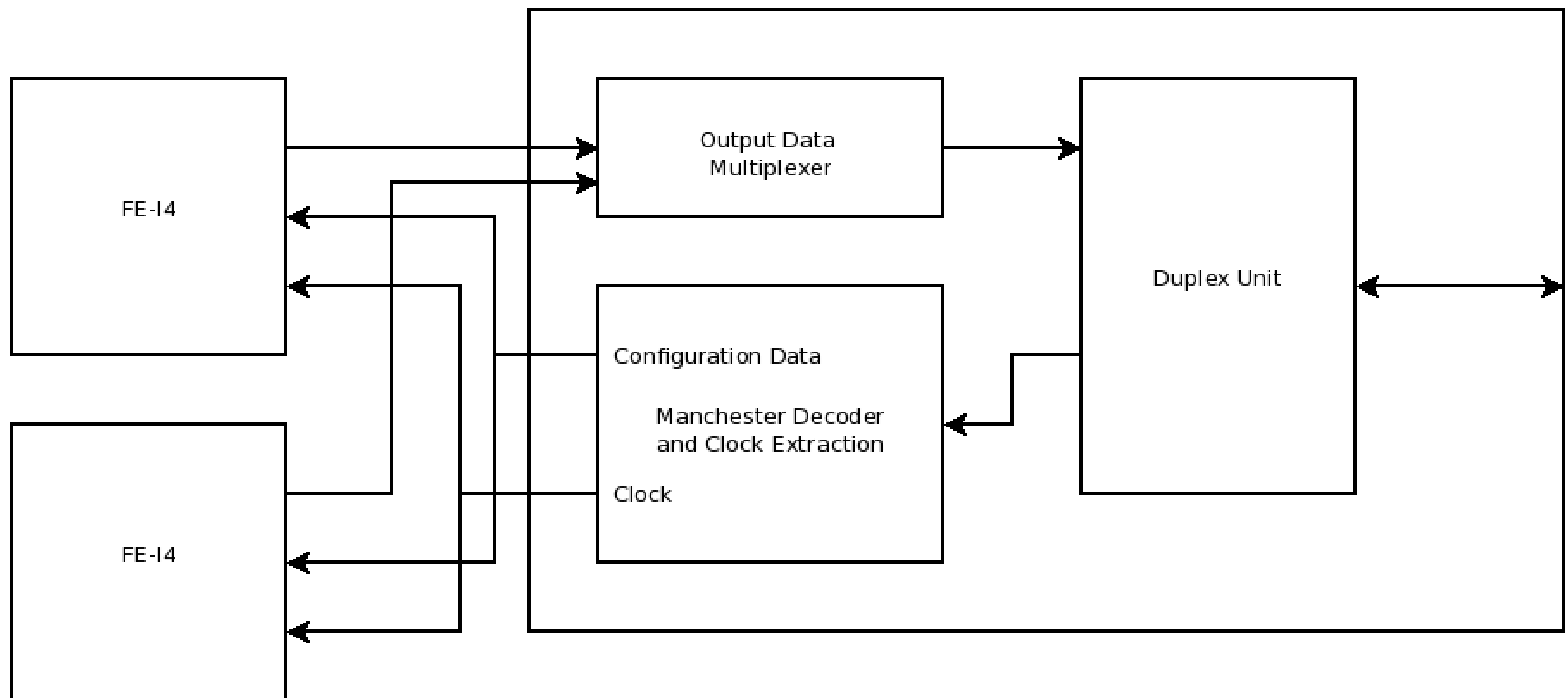
VTT's tapered via with partial plating and RDL – minimises stress above 15µm Cu thickness

Other work/Future work
Data Multiplexing & redundancy

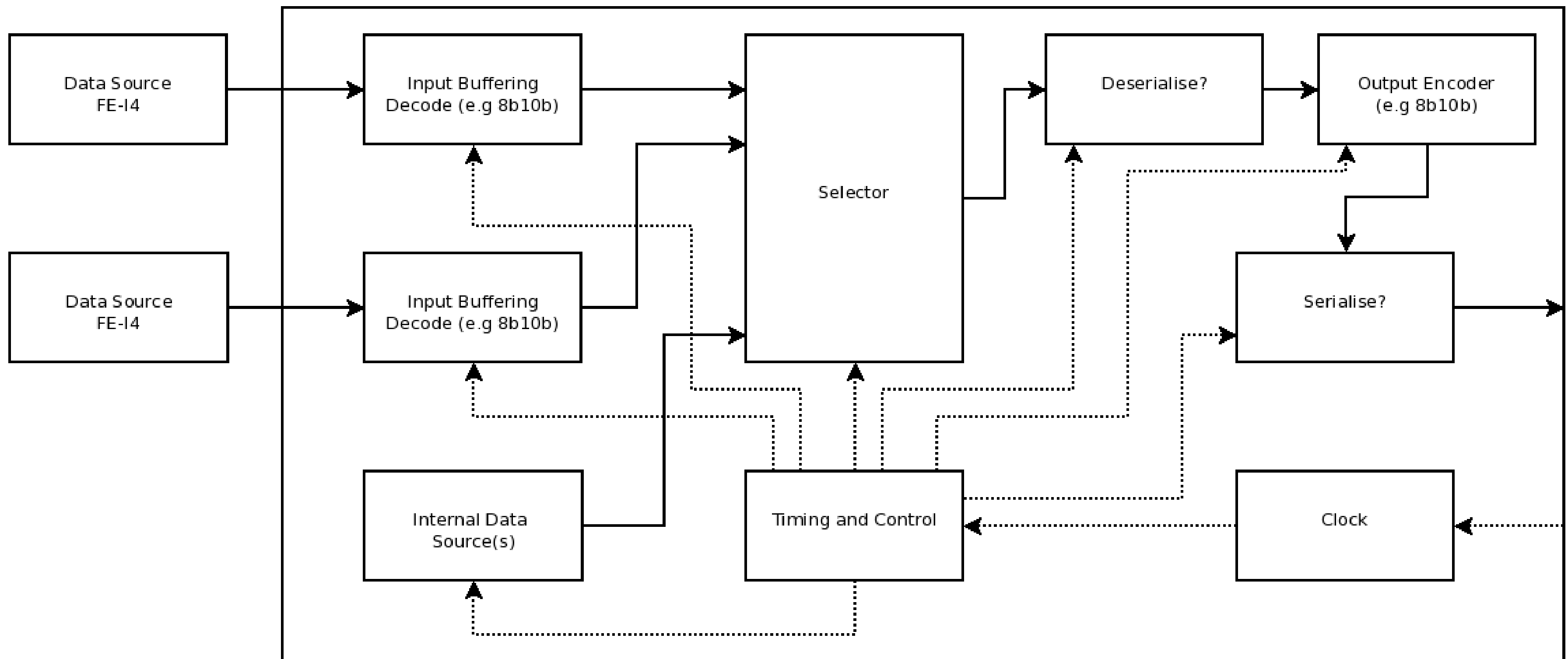
Primary Objectives – Reduce Mass

- Multiplex four FE-I4s to one Tx pair of wires
- Multiplex clock and configuration data into one Rx pair
- Combine the Tx and Rx pairs into one using Full-duplex or Half-duplex
- Reduce number and size of passives on the modules
- Facilitate reliable AC-coupled data for serial power – reduction of cable size
- Allow other FE-I4s to function if one fails
- Other possible I-O functions via same data pair, such as current reference trim for FE-I4s

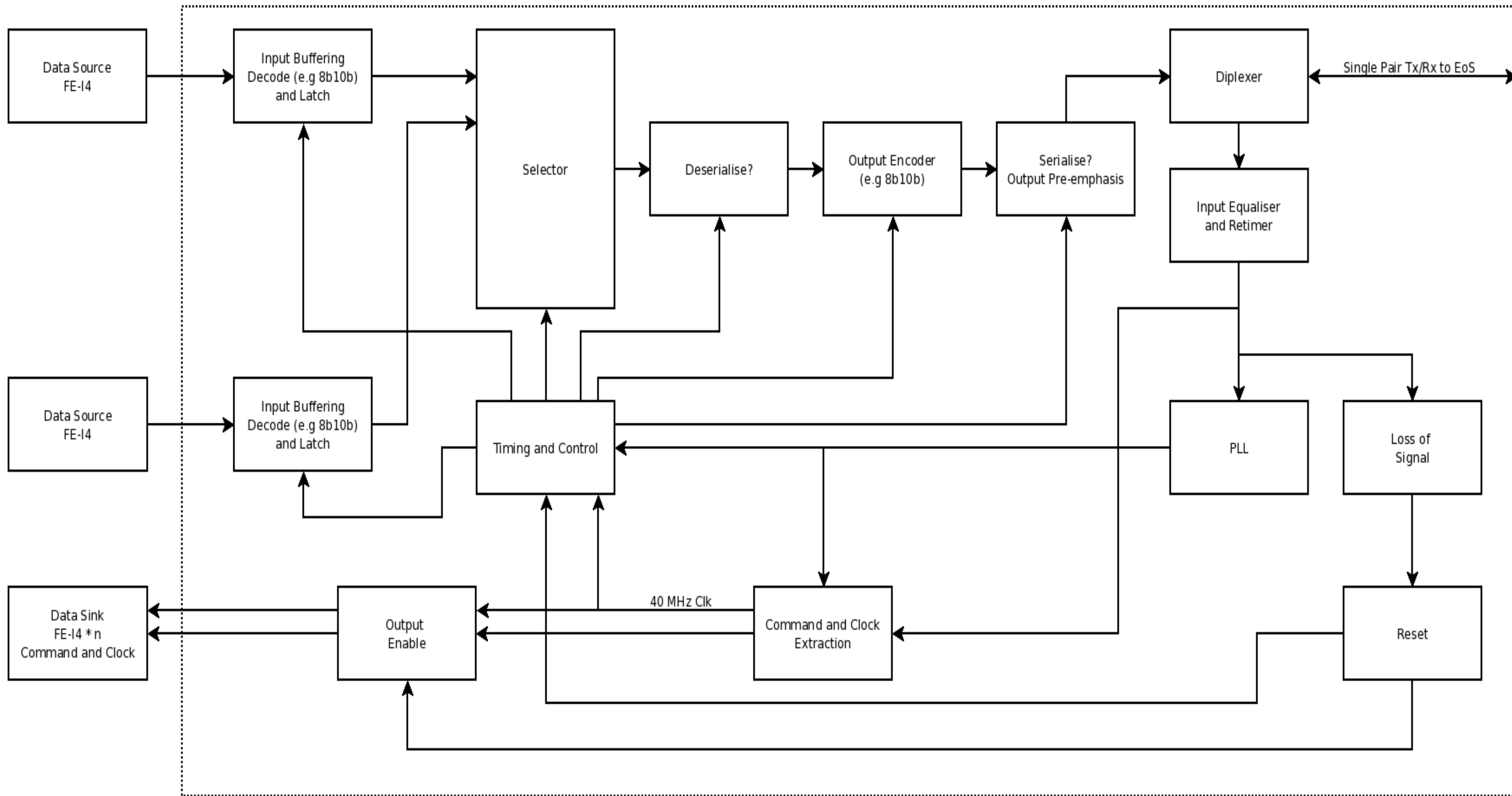
Combined Input and Output Mux



A Possible output Mux Configuration



Multiplexing concept

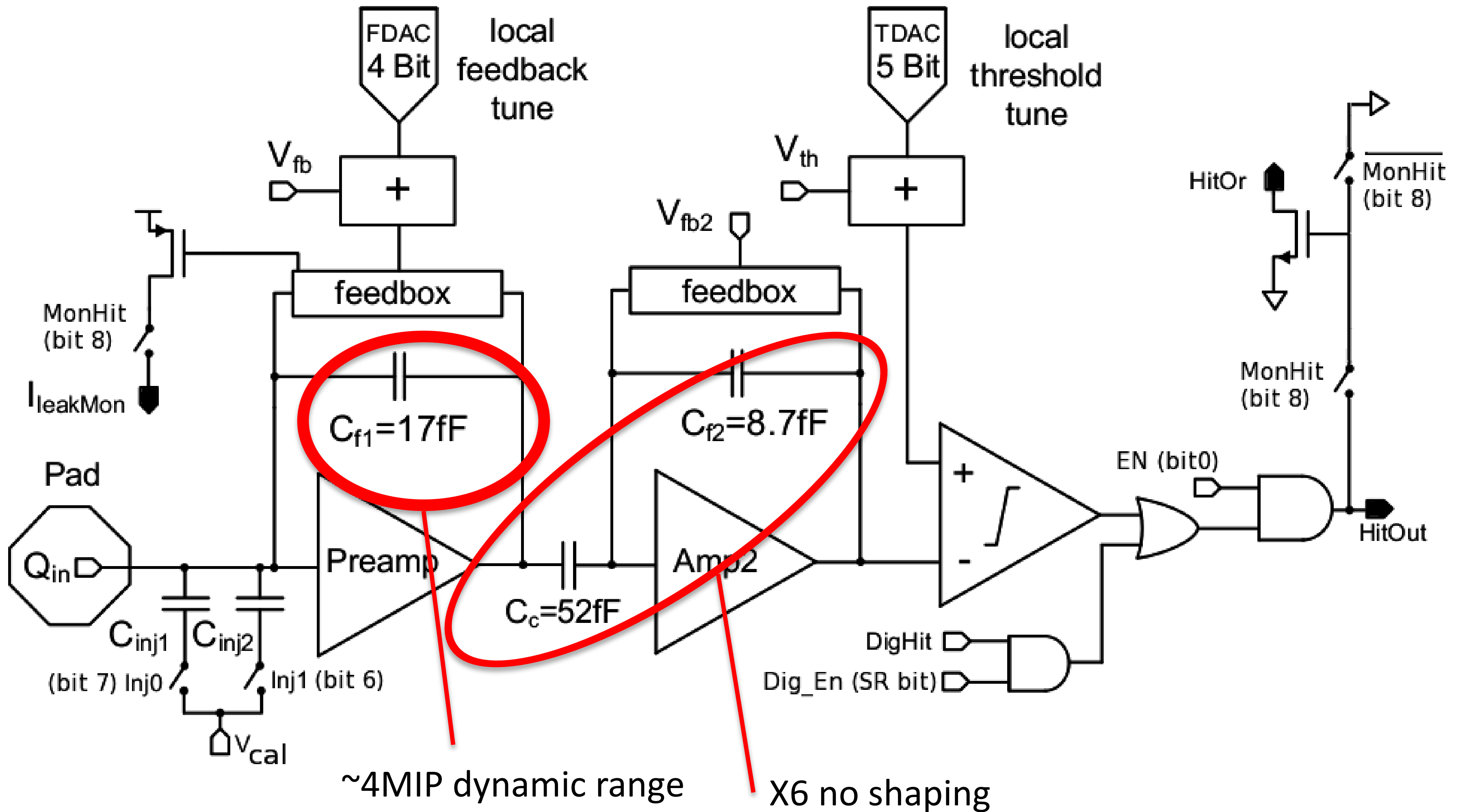


Summary

- Micron 6inch FE-I4 single and quad sensors
  - 300 µm and 150 µm
- Assemblies with flip-chip VTT
  - Excellent assembly IV characteristics
  - Problems at the edge due to bow with low bump yield
- Quad module
  - Hybrid option
- Plans for further development

Back Up slides

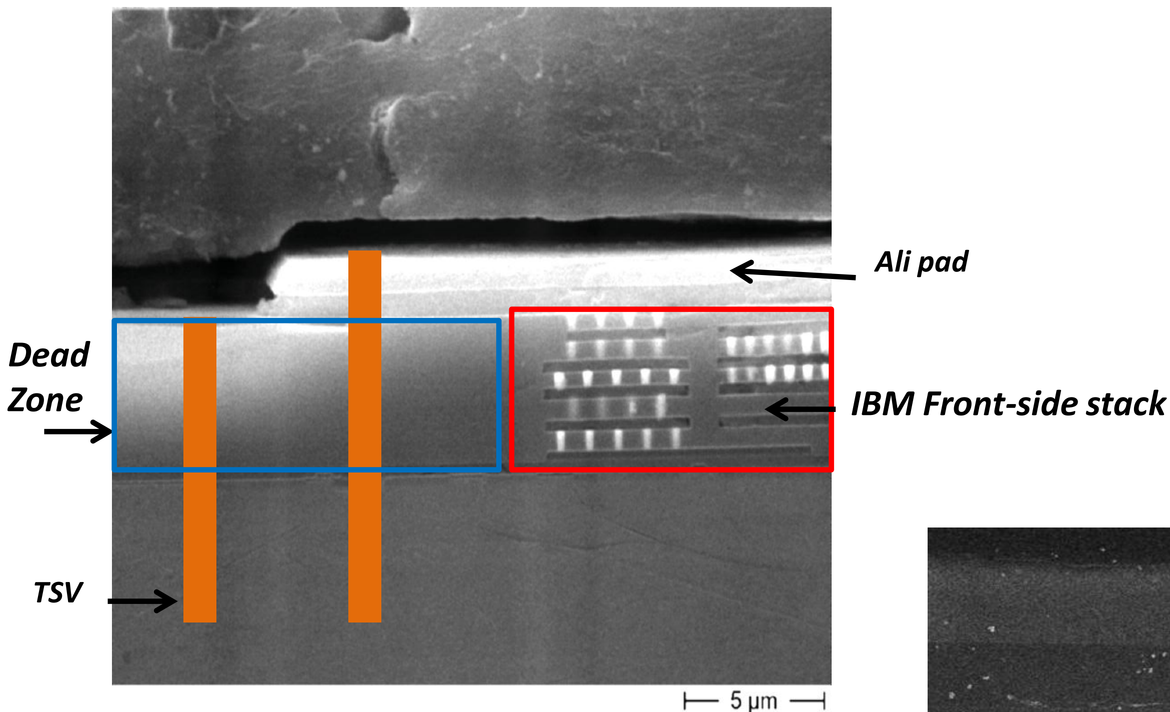
Analogue FE



Through Silicon Vias

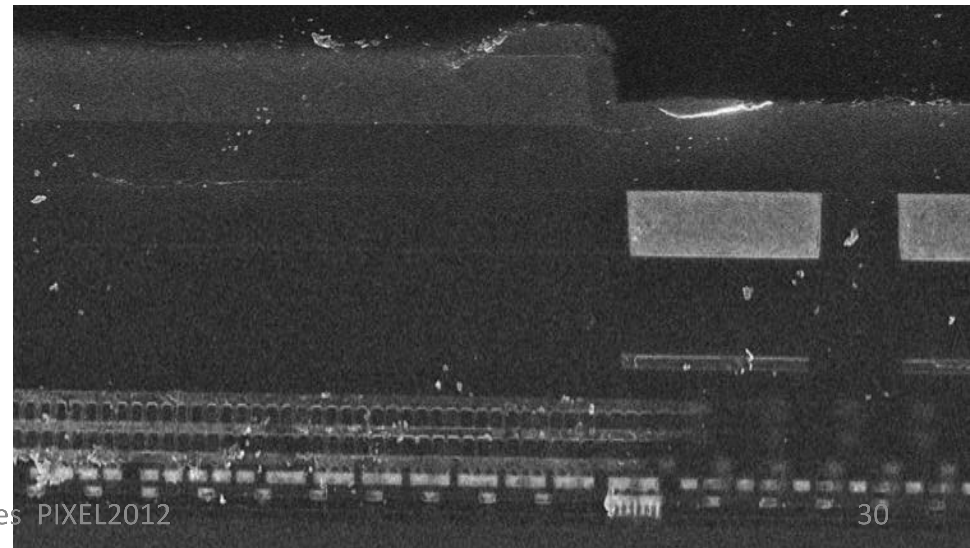
Comparison of FE-I3 and FE-I4

Motivation for decision

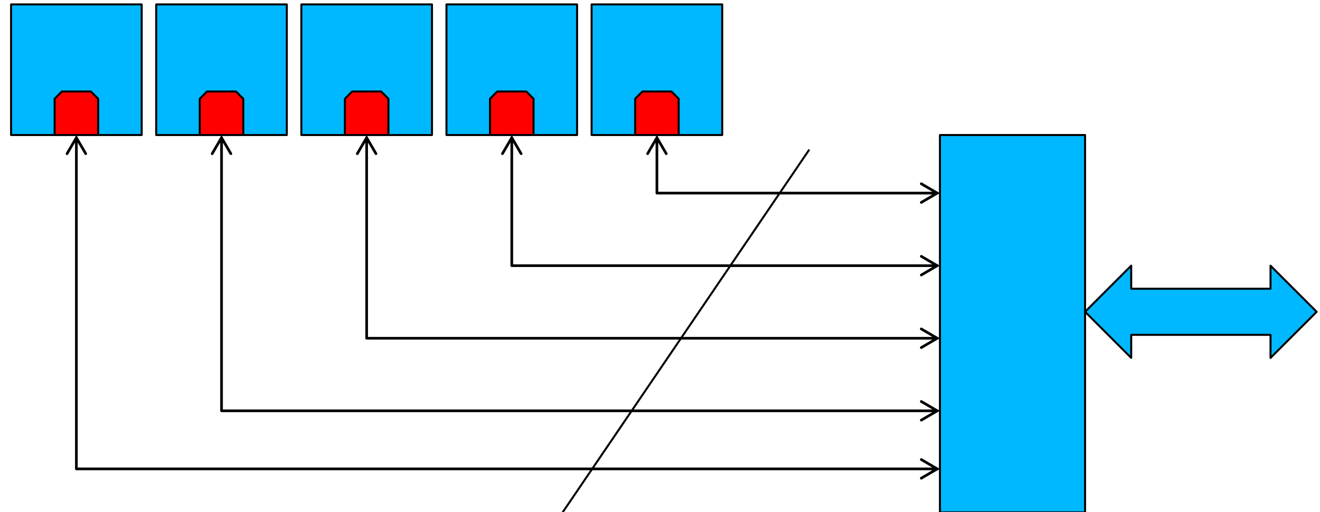


- ***FE-I4 has no route through the IBM front-side stack***
- ***Active metal everywhere under and surrounding the pad***
- ***Connection only possible from etching the back-side of the wafer***
- ***Complications arise to pinch through dielectric/poly-Si sandwich to contact metals***

- ***FE-I3 offers an easier route to developing a TSV process***
- ***FE-I3 represents a more realistic approach to integrating TSVs in terms of manufacturability (high yielding TSVs)***
- ***Process test structures and ET test structures to be developed in parallel***
- ***Process development on FE-I3 to be used in next FE-Ix chip and a clear definition of TSV-ready given***

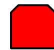


Quad modules



1 pair/Module
Carry clk-cmd-data
Start to consider cable design

EoS card
Multiplexing?



Contains: output data multiplexer & manchester decoder & (half-)duplexer