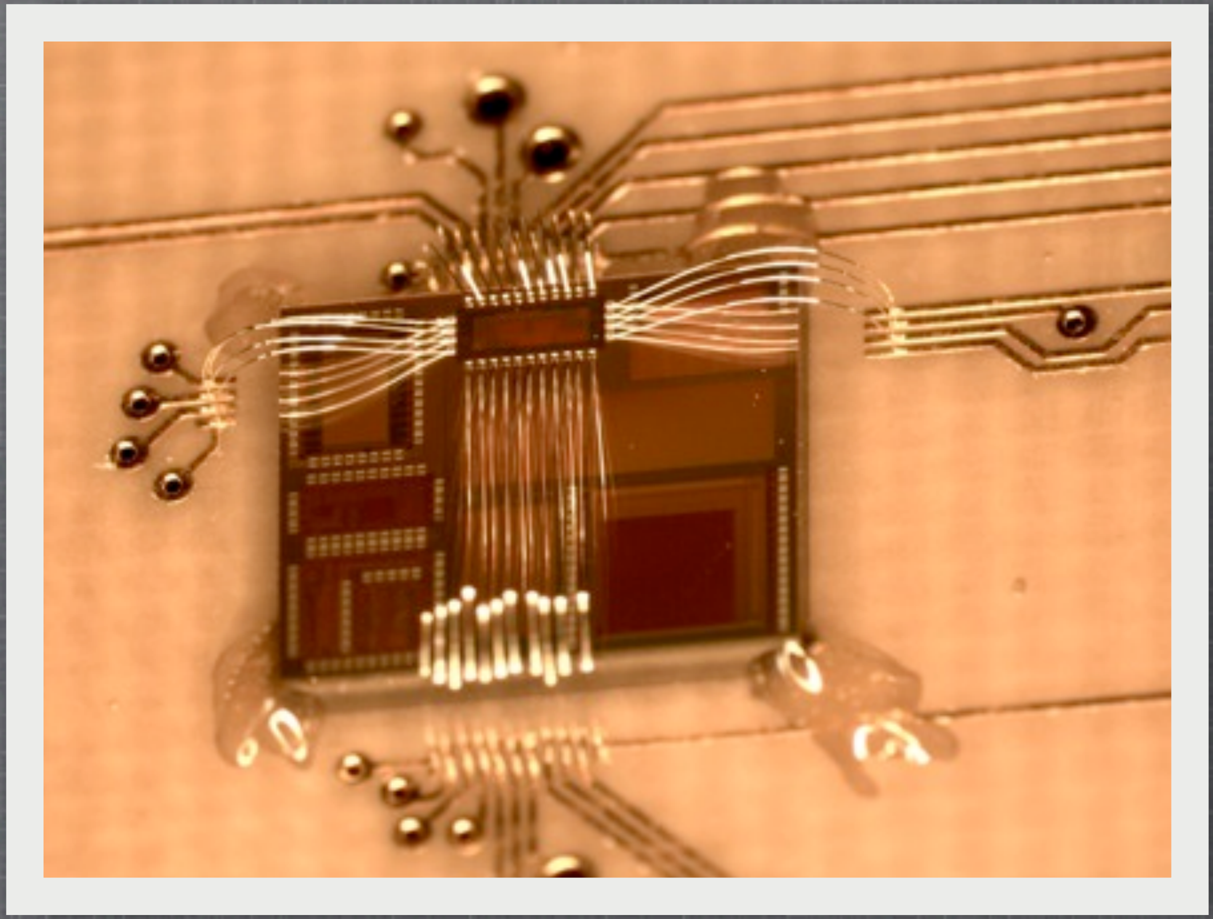
ADVANCES IN THE DEVELOPMENT OF PIXEL DETECTOR FOR THE SUPERB SILICON VERTEX TRACKER

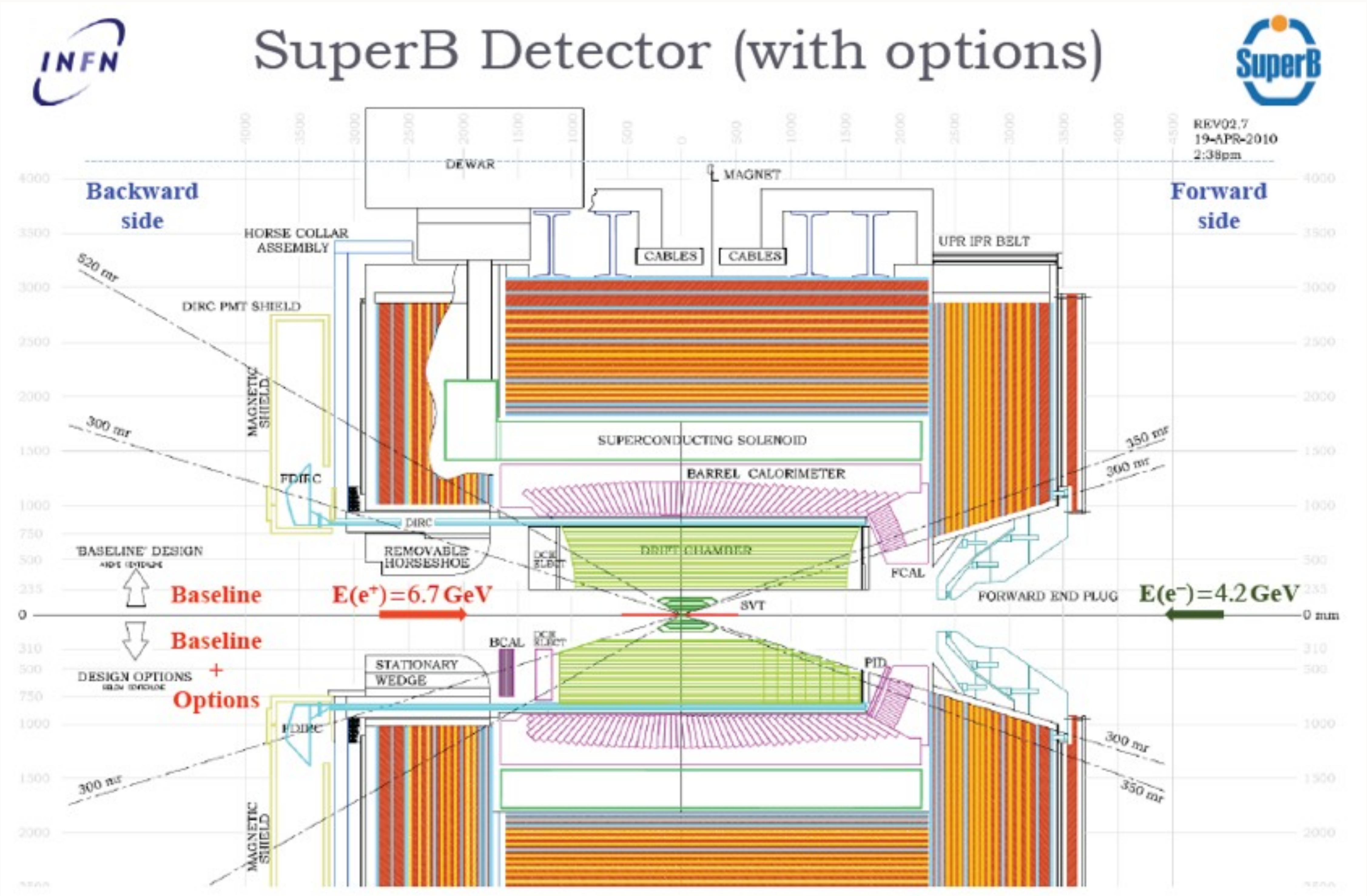


Eugenio Paoloni
(INFN & Università di Pisa)
on behalf of the SVT-SuperB group

Talk Outline

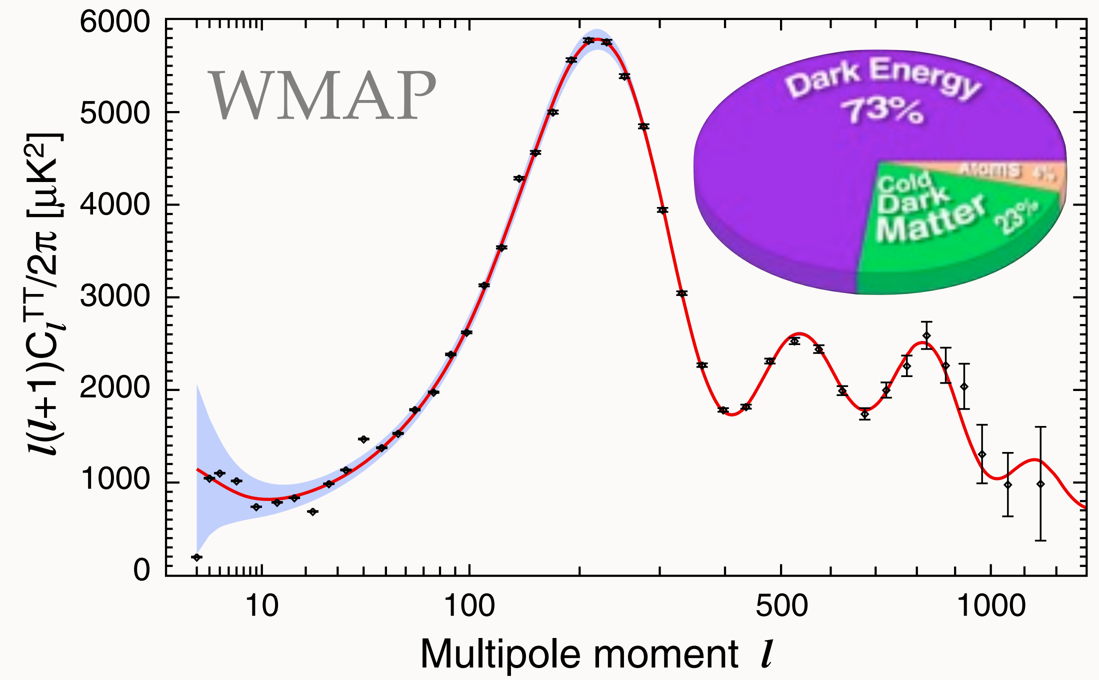
- Super*B*: *quick* outlook of the detector & machine
  - Main parameters, constraints for the detector, backgrounds
- Requirements for the Super*B* SVT layer0
- Detector options for the SVT layer0
  - CMOS Monolithic Active PixelS (MAPS)
  - INMAPS
  - 3D CMOS MAPS

The SuperB Detector

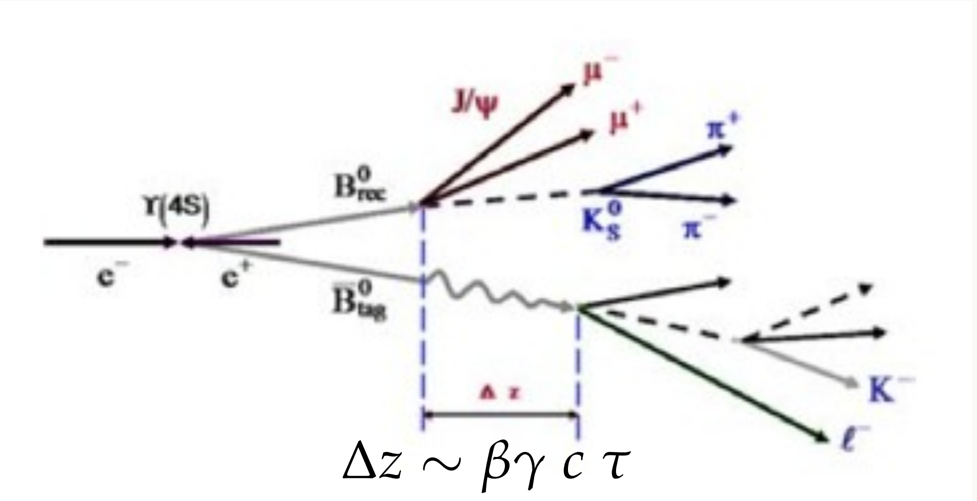


The SuperB Research Program

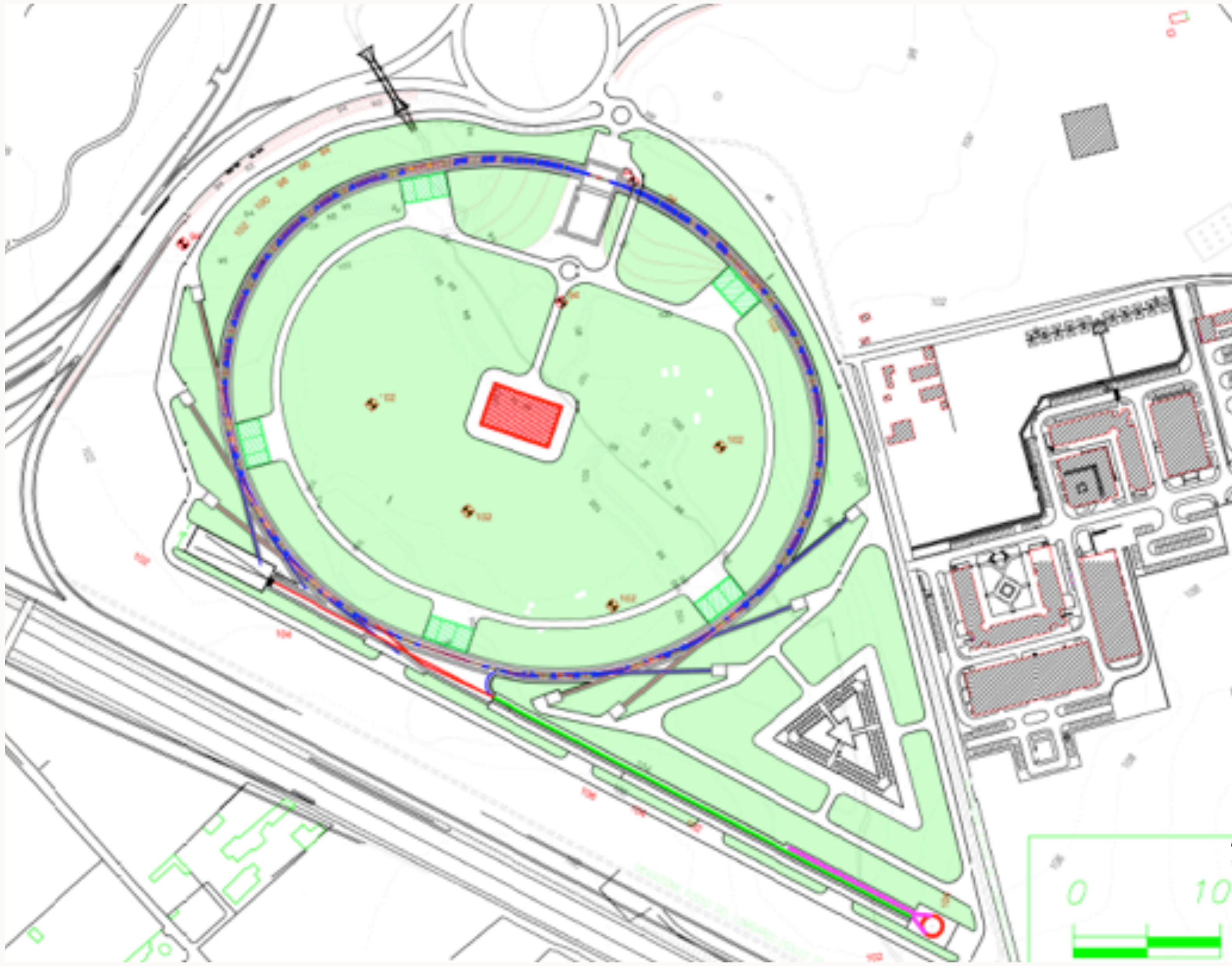
- Cosmological observations are providing us sound evidence of Physics beyond the Standard Model
  - General consensus that the SM CP violation cannot explain the matter-anti matter asymmetry of the universe
  - Micro wave background anisotropy points to non SM matter + Dark energy



- BaBar and Belle *confirmed* the SM and posed *tight constraints* on the energy scale and flavor structure of the Physics beyond the SM
- Super*B* and Belle-2 research plan is complementary to the LHC one
  - The New Physics structure can be (hopefully) inferred by the behavior of Nature at low energy looking for discrepancies among the SM predictions and the actual world
  - A crucial piece of this program relies on the spatial resolution of the vertex detector



The SuperB Collider In Tor Vergata



	Units	HER	LER
Release		V12	
Circumference	m	1258.4	
Frequency turn	Hz	2.38E+05	
# bunch		978	
Frequency collision	Hz	2.33E+08	
Full crossing angle	Rad	0.060	
Energy	GeV	6.7	4.18
Energy ratio		1.60	
βx	cm	2.6	3.2
βy	μm	253	205
coupling		0.0025	0.0025
εx	nm	2.07	2.37
εy	pm	5.175	5.925
Bunch length	cm	0.5	0.5
Current	A	1.89	2.44
# particles		5.08E+10	6.56E+10
σx	micron	7.34	8.71
σy	nm	36.2	34.9
Piwinsky angle		20.45	17.23
Horizontal tune shift	%	0.21	0.33
Vertical tune shift	%	9.89	9.55
Luminosity	Hz/cm^2	1.00E+36	

- SuperB is a $e^+ e^-$ collider based on 2 separates storage rings operating at the Y(4S) peak.
- The luminosity leap w.r.t to BaBaR (x 100) is obtained by cranking down the vertical size of the beam @ the Interaction Point (35 nm)

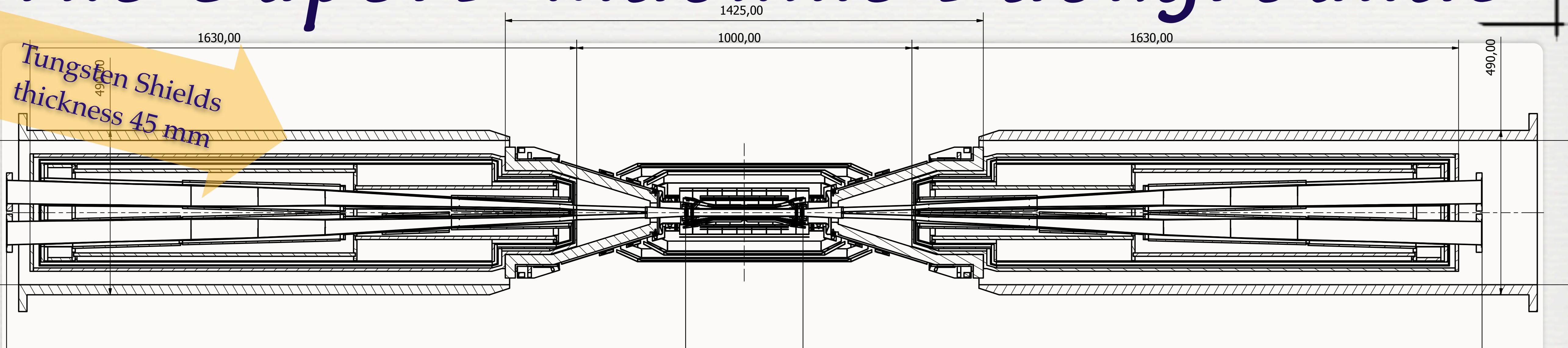
The SuperB Collider In Tor Vergata

- 2007 : Conceptual Design Report published
- 2010 : Approved by the Italian Government
  (250 M€ allocated for the Infrastructures)
- 2011 : Site established: Roma Tor Vergata
  - Cabibbo Lab consortium (INFN, Uni Tor Vergata) management structure established
- 2012: Accelerator costing review in progress
  Detector Technical Design Report

- SuperB is a $e^+ e^-$ collider based on 2 separates storage rings operating at the Y(4S) peak.
- The luminosity leap w.r.t to BaBaR (x 100) is obtained by cranking down the vertical size of the beam @ the Interaction Point (35 nm)

	Units	HER	LER
Release		V12	
Circumference	m	1258.4	
Frequency turn	Hz	2.38E+05	
# bunch		978	
Frequency collision	Hz	2.33E+08	
Full crossing angle	Rad	0.060	
Energy	GeV	6.7	4.18
Energy ratio		1.60	
βx	cm	2.6	3.2
βy	µm	253	205
coupling		0.0025	0.0025
εx	nm	2.07	2.37
εy	pm	5.175	5.925
Bunch length	cm	0.5	0.5
Current	A	1.89	2.44
# particles		5.08E+10	6.56E+10
σx	micron	7.34	8.71
σy	nm	36.2	34.9
Piwinsky angle		20.45	17.23
Horizontal tune shift	%	0.21	0.33
Vertical tune shift	%	9.89	9.55
Luminosity	Hz/cm^2	1.00E+36	

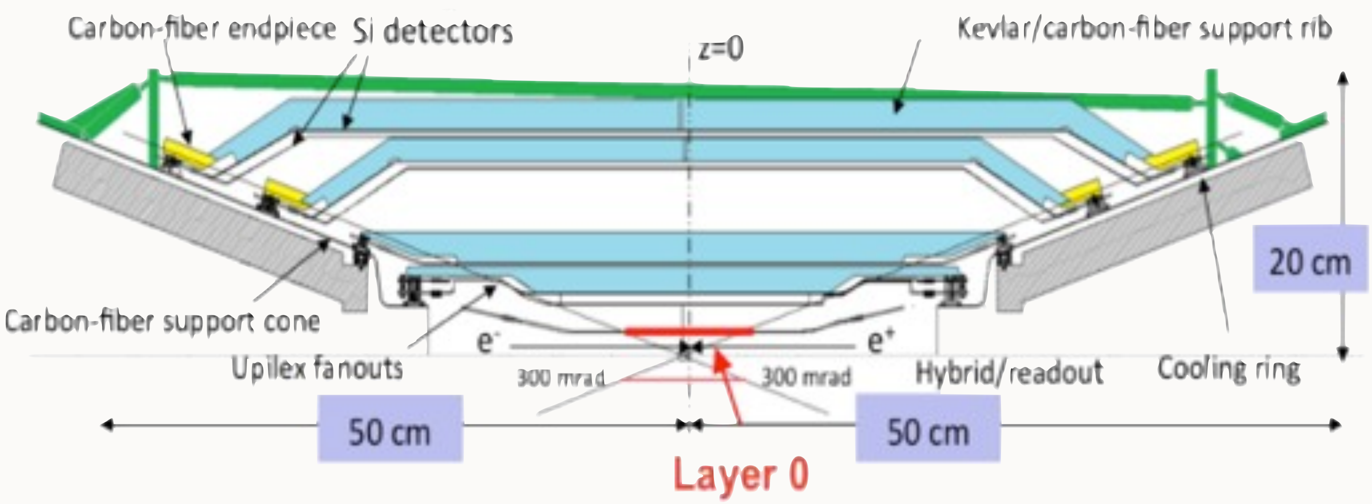
The SuperB Machine Backgrounds



Tungsten Shields thickness 45 mm

	Scattering Cross section	#Evt / crossing	*Scattering* Rate	
Radiative Bhabha $e^+ e^- \rightarrow e^+ e^- \gamma$	~340 mbarn (Eγ/Ebeam > 1%)	~1400	0.34 THz	Luminosity lifetime driving term
Radiative Bhabha $e^+ e^- \rightarrow e^+ e^- \gamma$	~150 mbarn (Eγ/Ebeam > 10%)	~630	0.15 THz	Losses “near” the IP contained by W shields
pair production $e^+ e^- \rightarrow e^+ e^- e^+ e^-$	~7.3 mbarn	~31	7.3 GHz	
e^+e^- production (seen by L0 @ 1.4 cm coverage 300 mRad)	~ 80 μbarn	~0.34	80 MHz	Main & irreducible SVT L0 Background
Elastic Bhabha	O(10^{-4}) mbarn (Det. acceptance)	~420/Million	100 KHz	~L1 Trigger rate
Υ(4S)	O(10^{-6}) mbarn	~4.2/Million	1 KHz	*B* mesons Physics

The SuperB Silicon Vertex Tracker



Based on the BaBar design

- 5 Layers of double-sided Si strip sensor
- Low material budget. (typical $P_t < 2.7 GeV$)
- Stand-alone tracking for soft particles.
- Resolution ~15 μm at normal incidence

The CM boost is reduced by a factor 2:

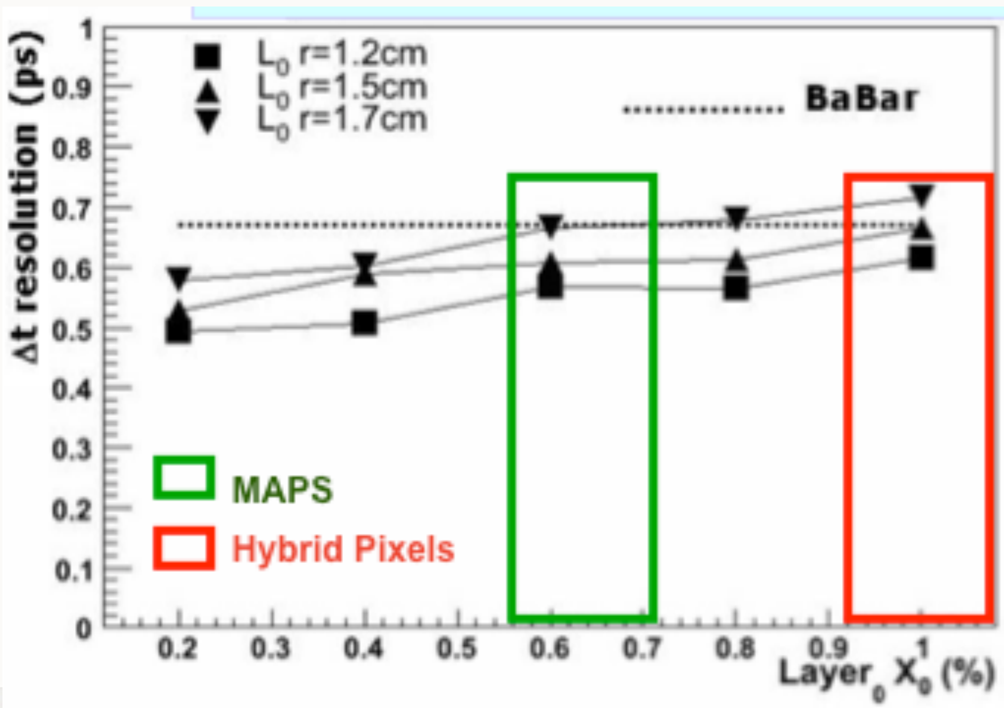
Super*B*: 6.7 GeV e^+ on 4.18 GeV e^-

BaBar : 9 GeV e^- on 3.1 GeV e^+

$B \to \pi^+\pi^-$: resolution on Δt vs L0 X/X_0

$\beta\gamma = 0.28$ Beam pipe $X/X_0 = 0.42\%$

Hit resolution 10μm

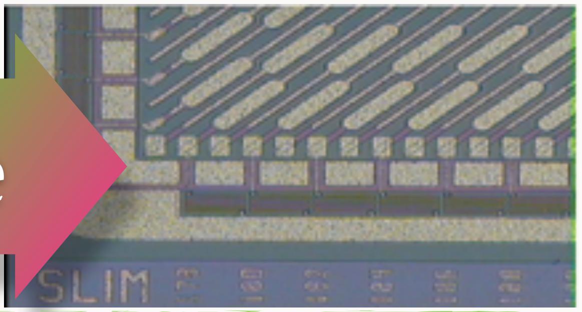


- Layer0 closer to the I.P. to reduce the leverage of the multiple Coulomb scattering on the impact parameter
  - Layer 0 radius ~ 1.2 - 1.5 cm
  - Very tight material budget < 1% X_0
  - Fine granularity 50 μm x 50 μm
- Very high backgrounds from the process $e^+ e^-$ to $e^+ e^- e^+ e^-$
  - The rate of this process is a steep function of the L0 radius: good resolution <=> High background! : (

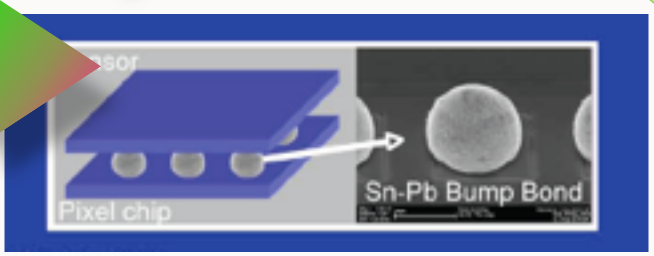
Options For The Layer 0 Detector

- ***Striplets:*** Baseline for the beginning of the data taking (i.e. low lumi & bkg.)
  - Mature technology, but:
    Rates @ 10^{36} Hz/cm^2 ~ 20 MHz/cm^2
  - Upgrade to pixels when the nominal luminosity will be reached

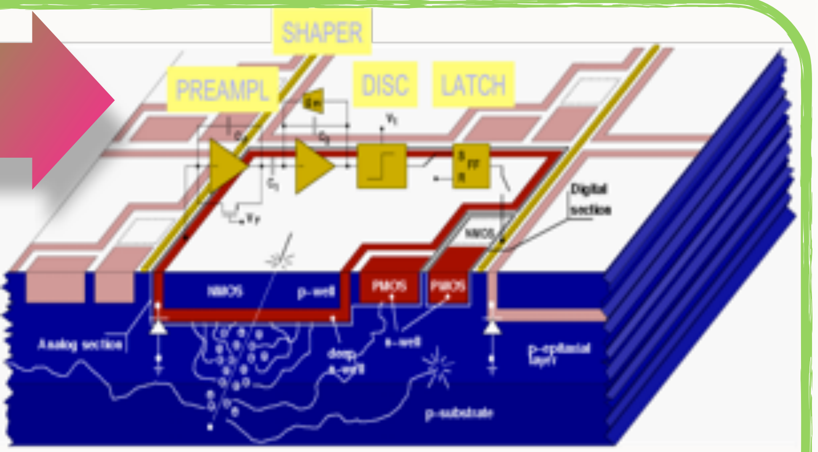
Baseline



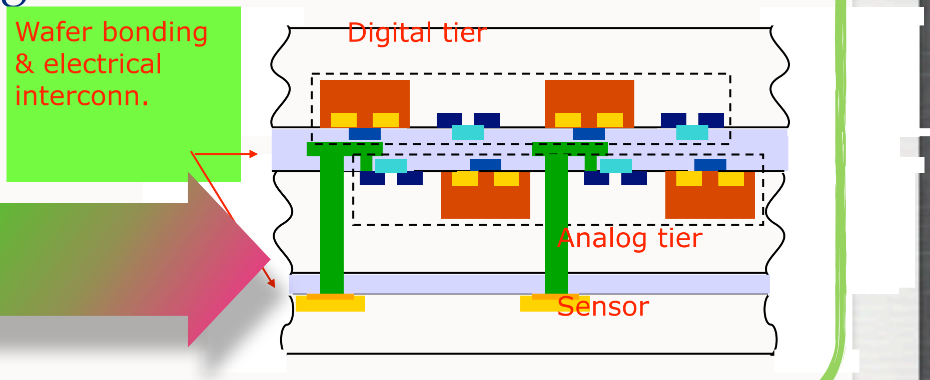
- ***Hybrid pixels:*** viable, but…
  the material budget is tight $X/X_0 \leq 1$ % and the pixel pitch is fine 50 µm
  - Superpix0 - FE prototype chip with 50x50 µm^2 pitch & fast data push readout (4k pixels, ST 130 nm) successfully tested on the SPS beam



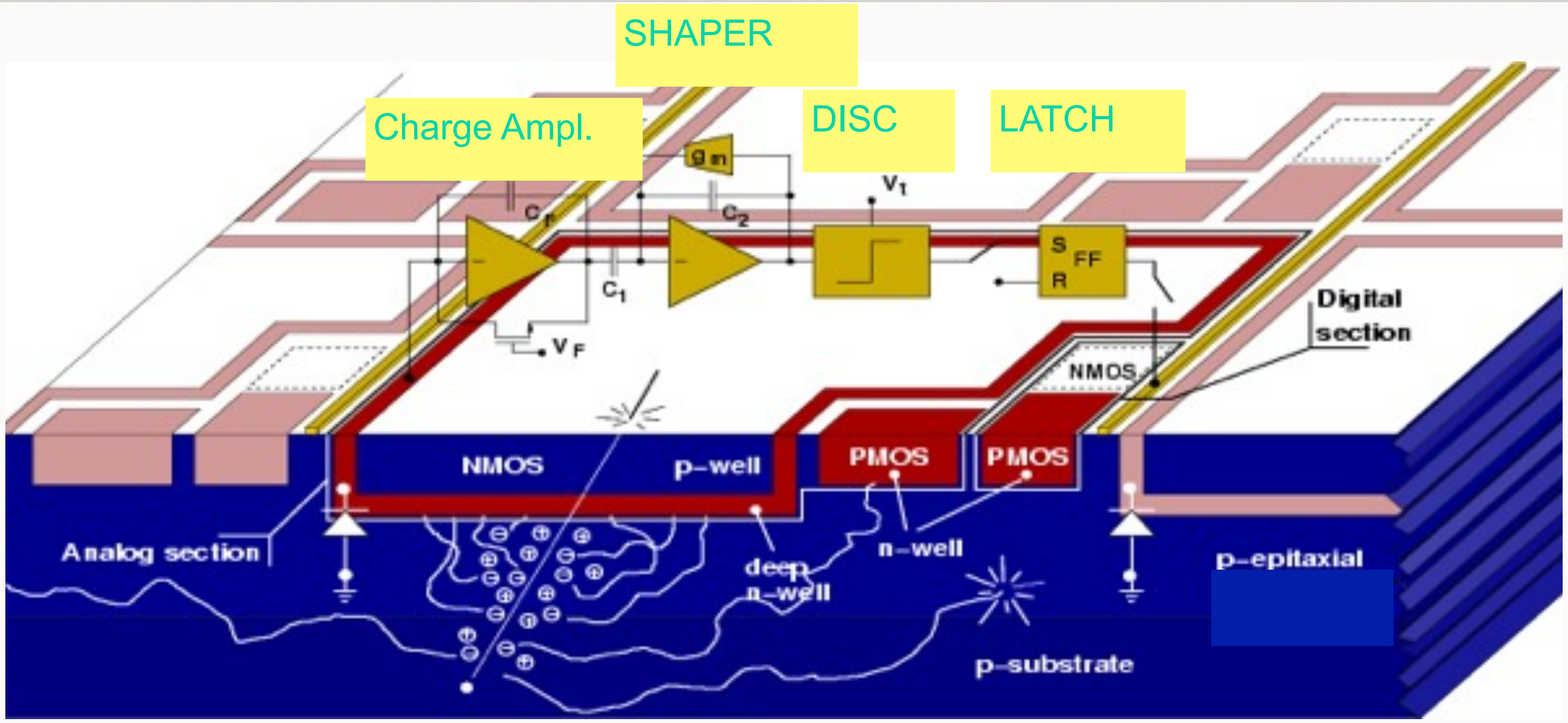
- ***CMOS MAPS:*** charming & challenging solution
  - Sensor + readout in a 50 µm thick chip
  - Deep N-well devices 50 x 50µm^2 with in-pixel sparsification.& fast readout architecture successfully tested
  - Evolution to quadruple well (INMAPS process)

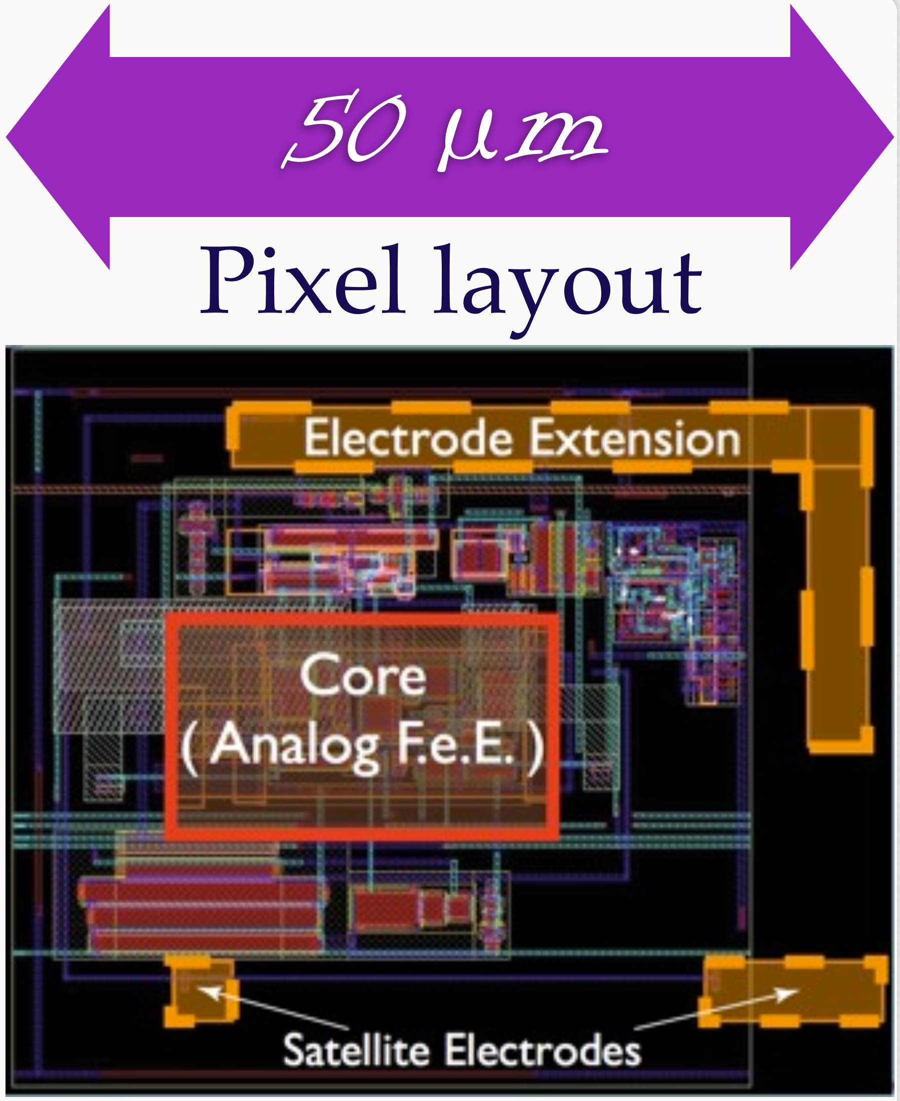


- ***Thin pixels with vertical integration:*** the more appealing and the tougher
  - Improved performance with higher functional density.
  - Two options are being pursued (VIPIX – INFN Collab.)
    - DNW MAPS with 2 tiers
    - Hybrid Pixel: FE chip with 2 tiers + high resistivity sensor



Monolithic Active Pixel Sensor Concept

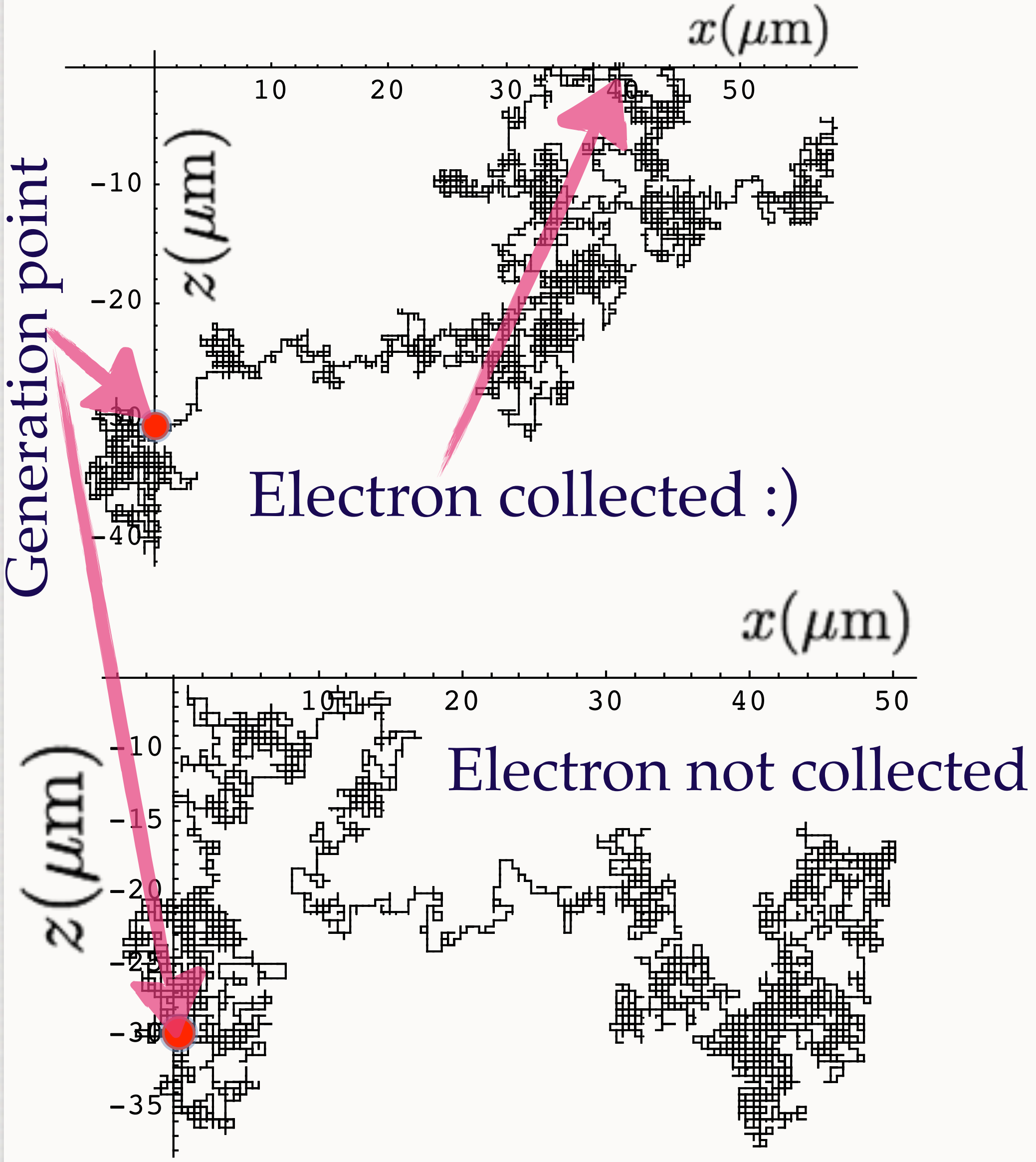


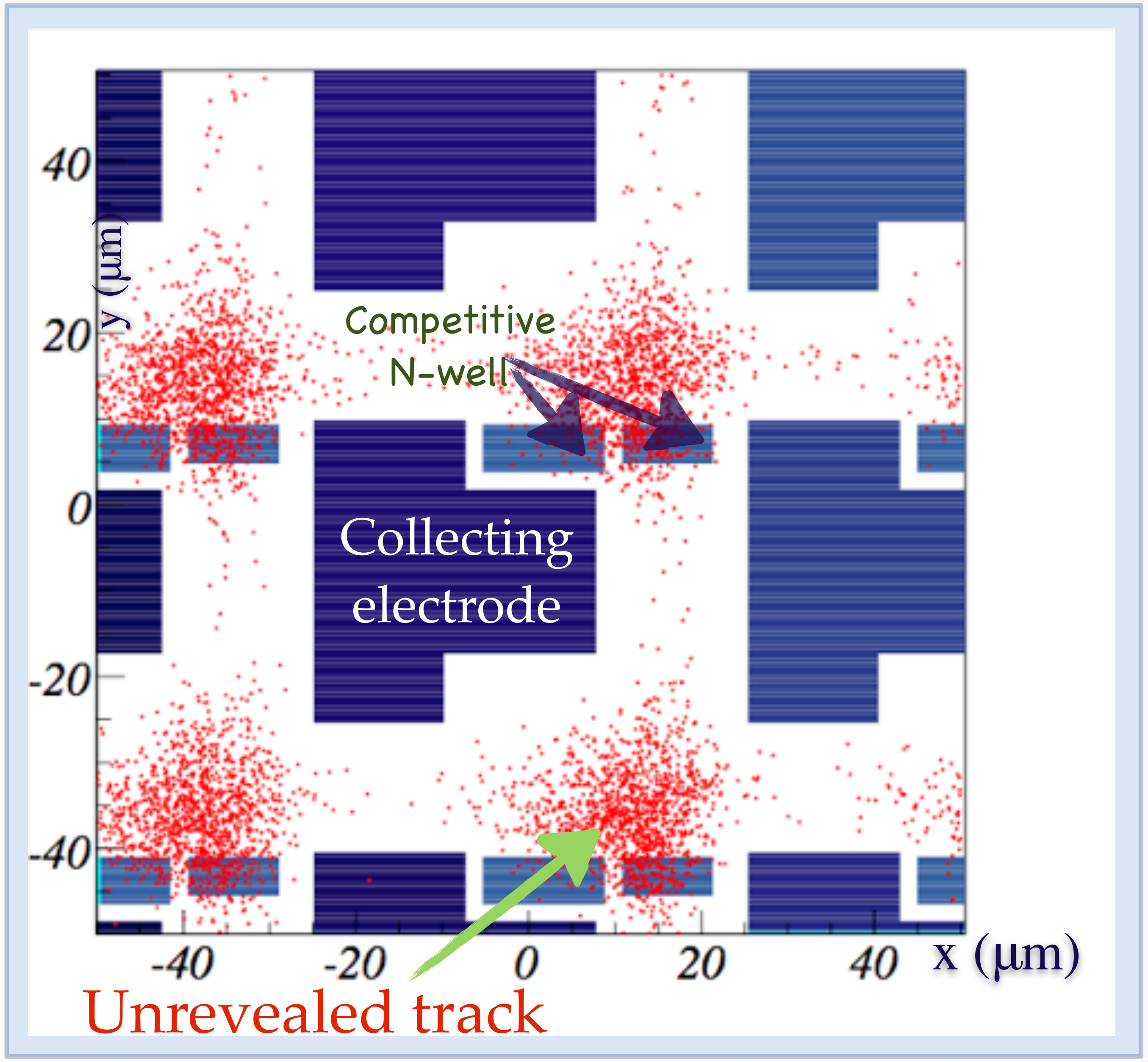


- The classical optimum signal processing chain for capacitive detector can be implemented at pixel level using modern VLSI triple-well processes at 130nm
- Charge-to-Voltage conversion done by a charge amplifier
- The collecting electrode (Deep N-Well) can be extended to obtain higher single pixel collected charge, reducing charge loss into competitive N-wells where P-mos are located.

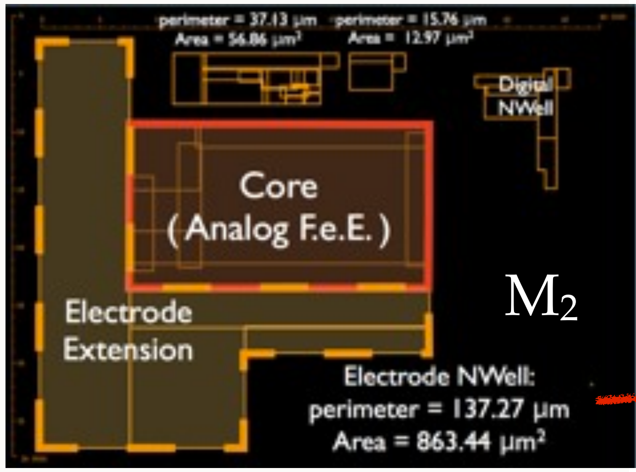
Collecting Electrode Geometry Optimization

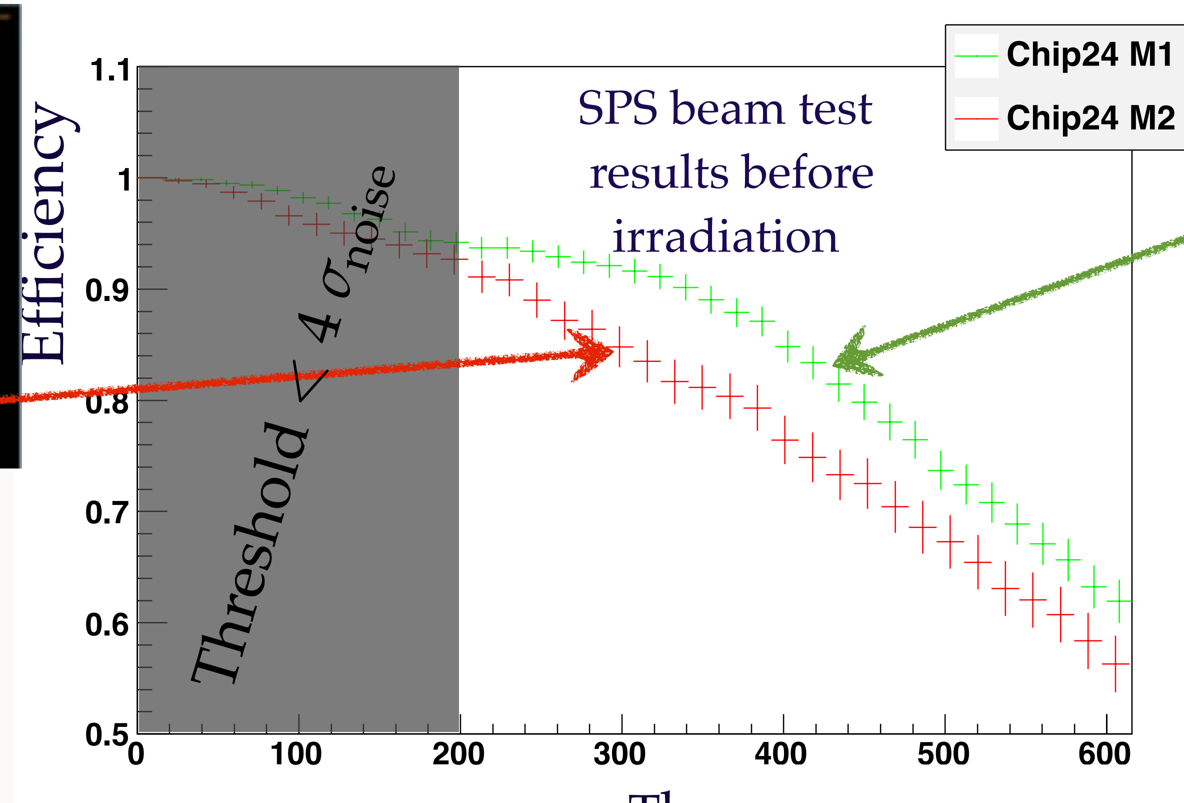
- A fast simulation tool had been developed to simulate the pairs generation by ionization and the sub sequent diffusion of the electrons
  - Continuous diffusion approximated with a discrete random walk



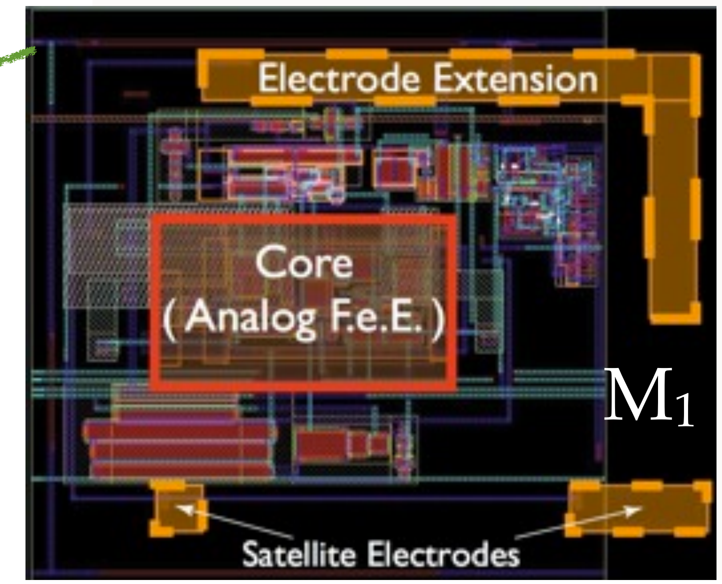


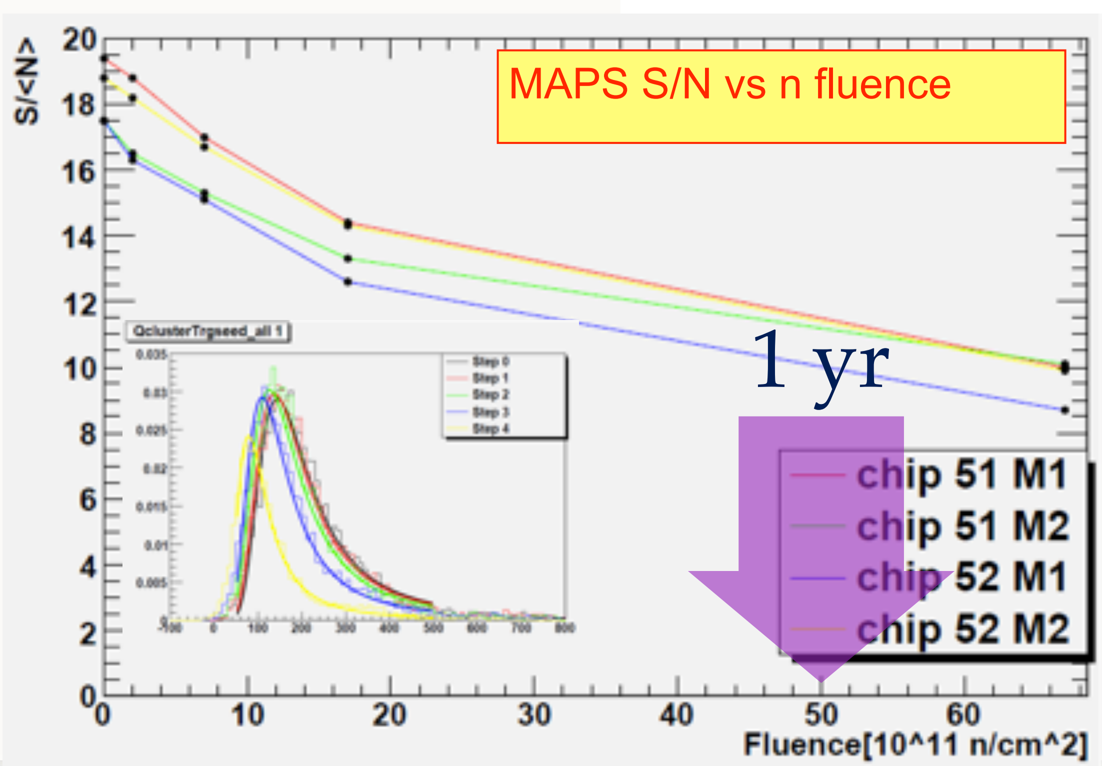
Triple Well MAPS Performances & Radiation Hardness

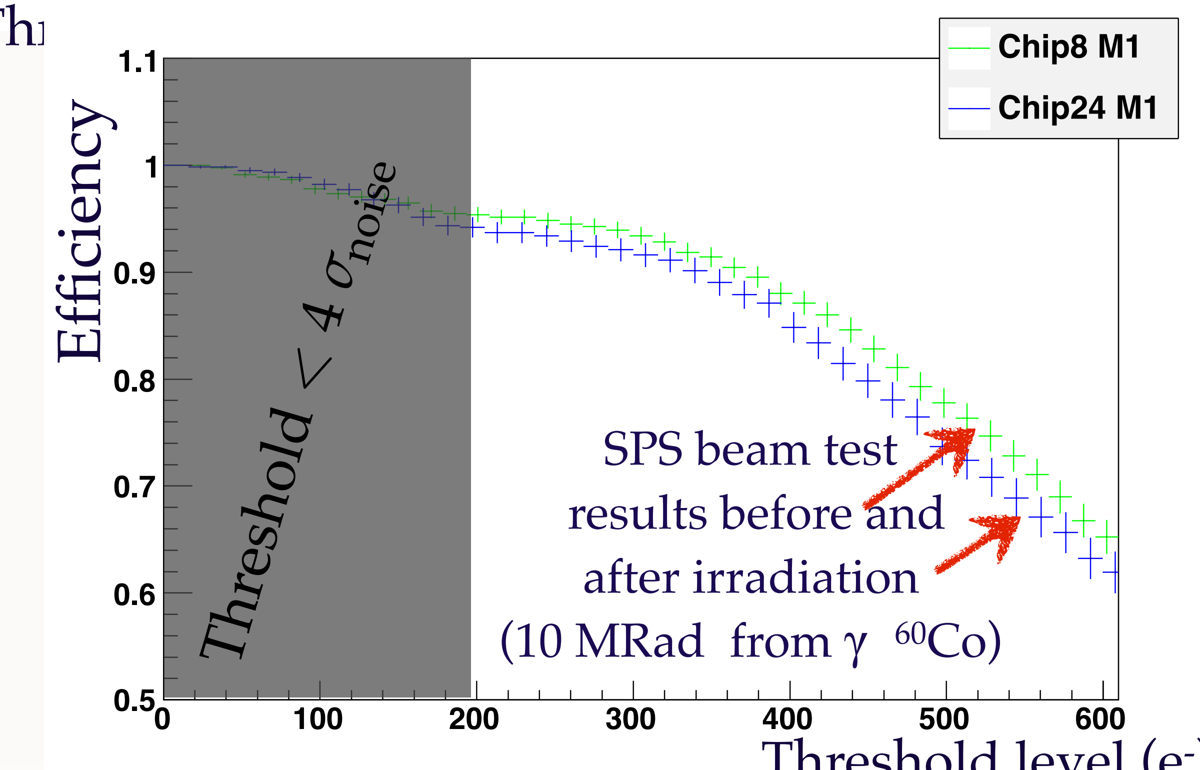




Optimization result

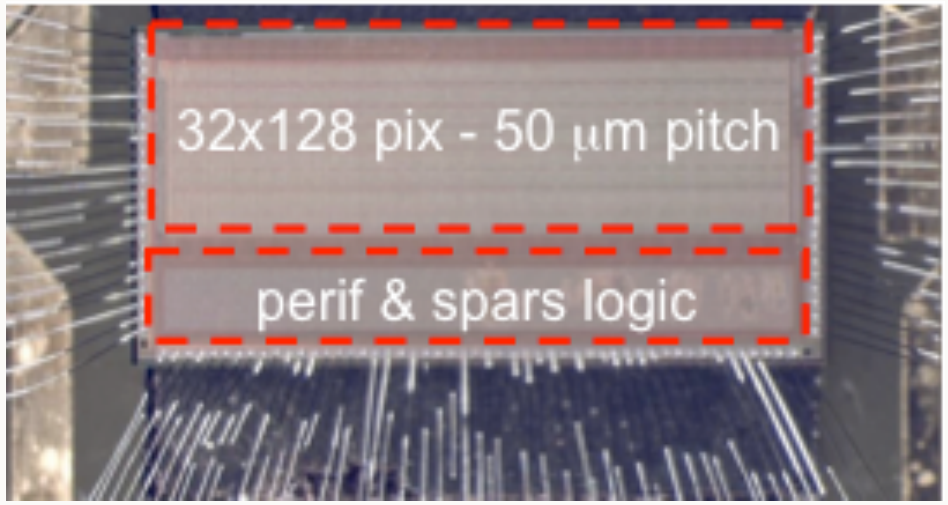






Beyond The Triple Well MAPS

Apsel4D - Triple well MAPS

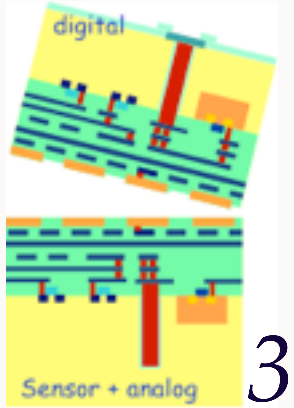


The main limitation of the triple well MAPS for SuperB arise from the charge collection efficiency

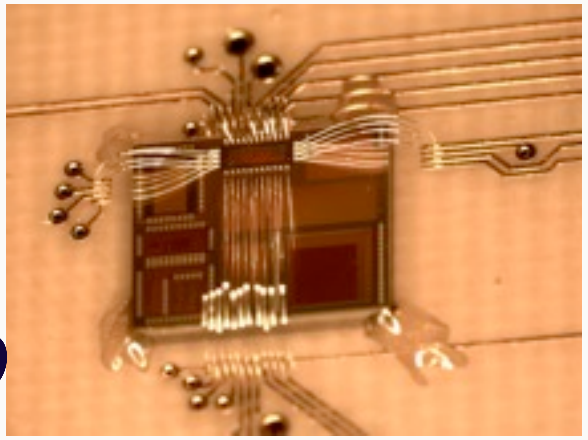
- The charge collection efficiency is reduced by radiation damage
- The detrimental effects of the competitive N-Well increases with the in pixel logic complexity

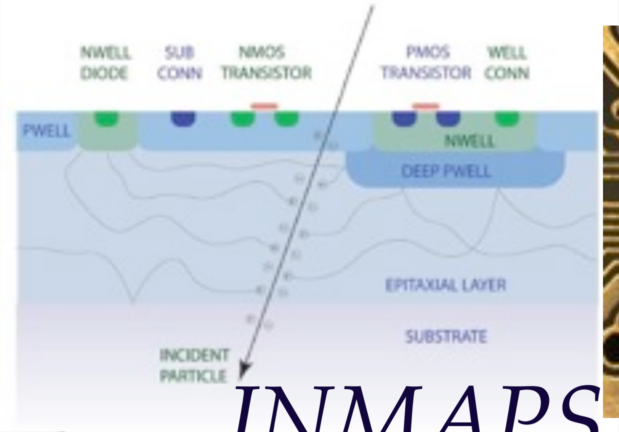
Two approaches to overcome these limitations

- 3D MAPS with vertical integration
  - 2 tiers (1 for the sensor & analog FE + 1 for digital RO)
  - Limited surface occupied by competitive N-well
  - More space available for in-pixel logic
- 2D MAPS with INMAPS 180 nm
  - competitive N-well detrimental effects neutralized by a deep P-well
  - high resistivity epitaxial layer also available
    - Higher charge collection efficiency and radiation hardness

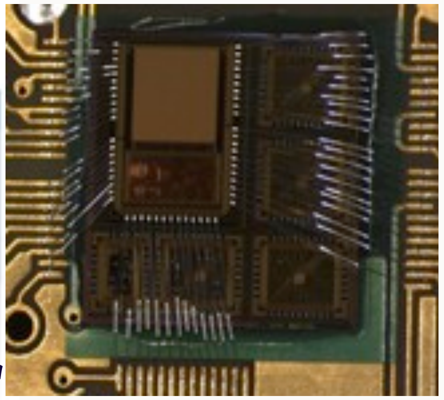


3D

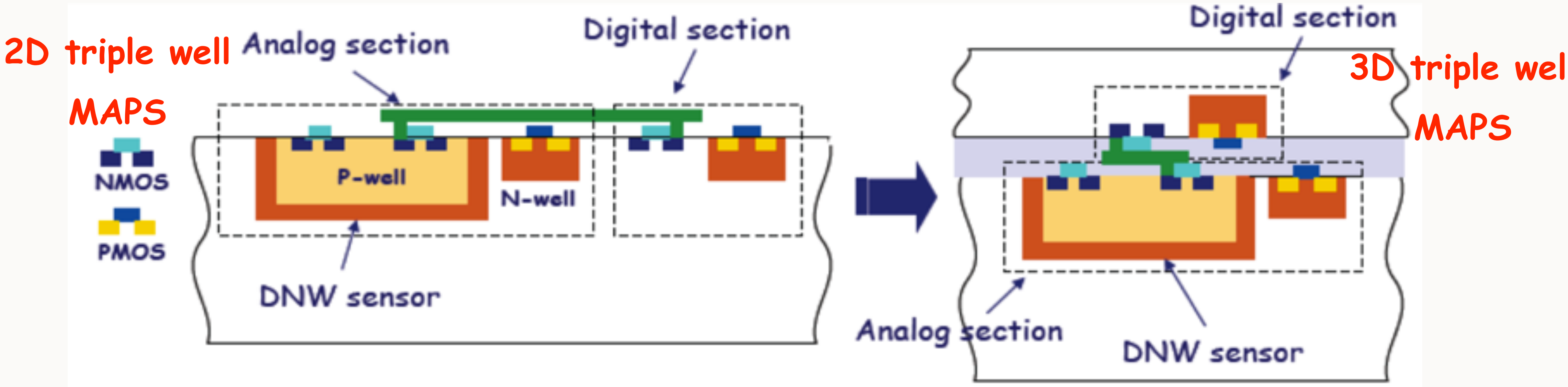




INMAPS



3D MAPS: Test Of The Analog FE.

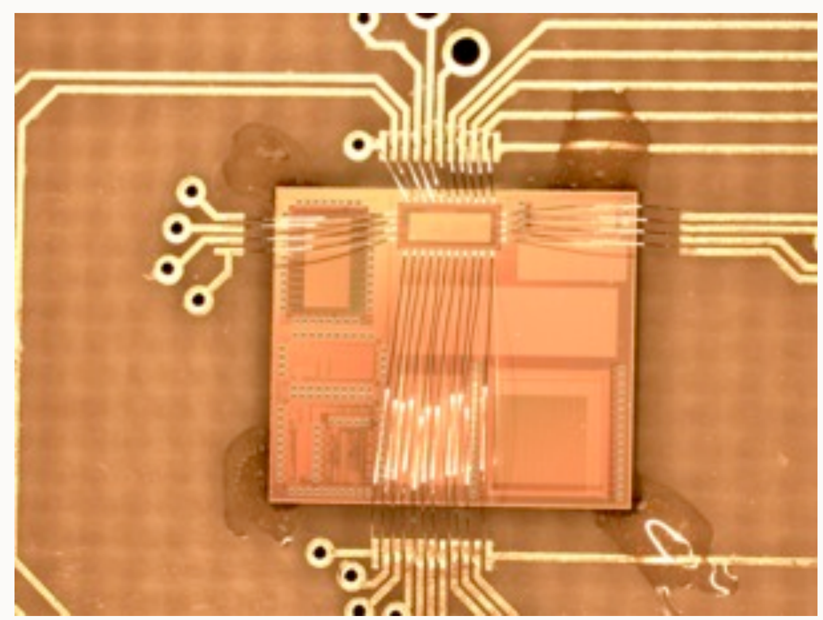


First APSEL-like DNW MAPS (2 tiers) realized within the 3DIC Consortium to explore the 130 nm Chartered/Tezzaron process.

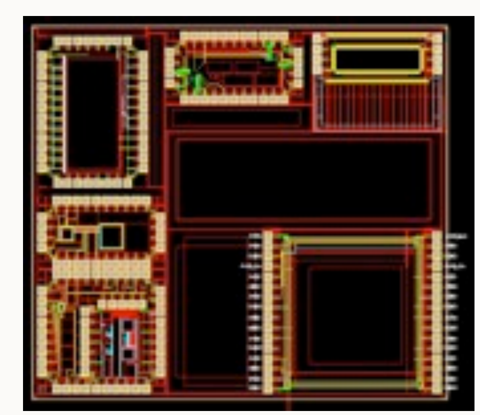
- Several problems with 3D interconnection (bad alignment …)
- While still waiting for good 3D chips:

→ test of the sensor+analog layer confirmed the expected improvement in collection efficiency related to improved fill factor

→ prepare new 3D run Tezzaron/ GlobalFoundries technology (organized by CMP/MOSIS)



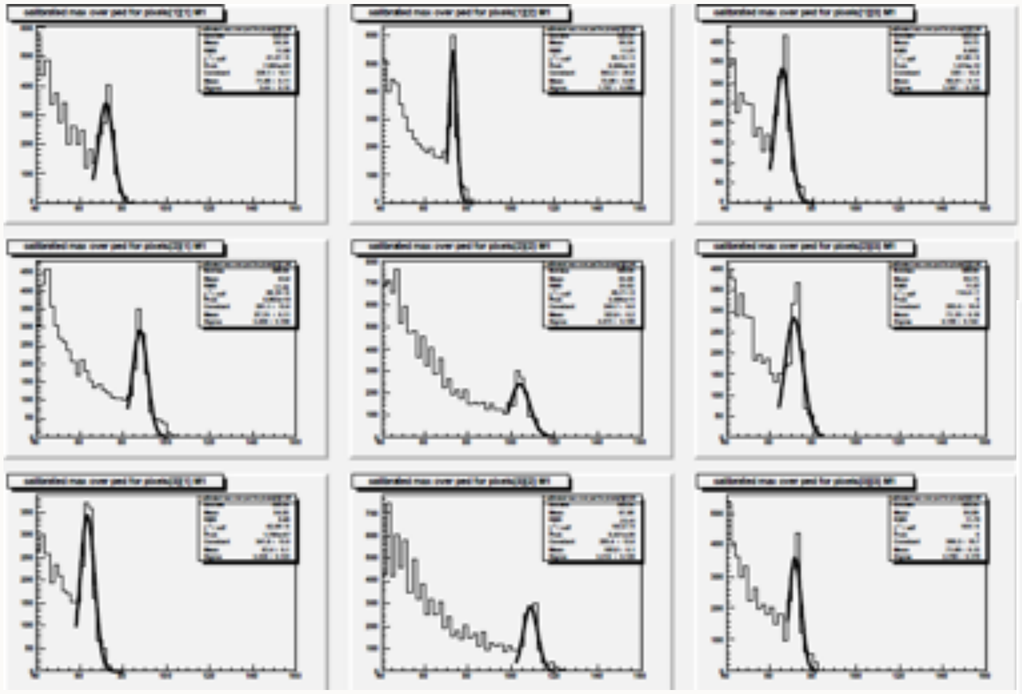
Digital layer

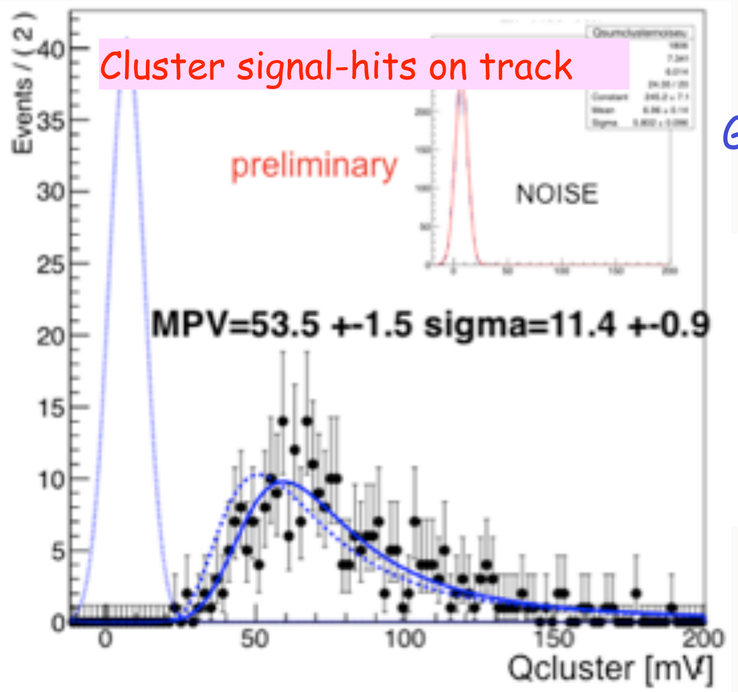


Sensor + analog

3D MAPS Measured Performances

Fe^{55} γ (5.9 keV) – 3x3 matrix



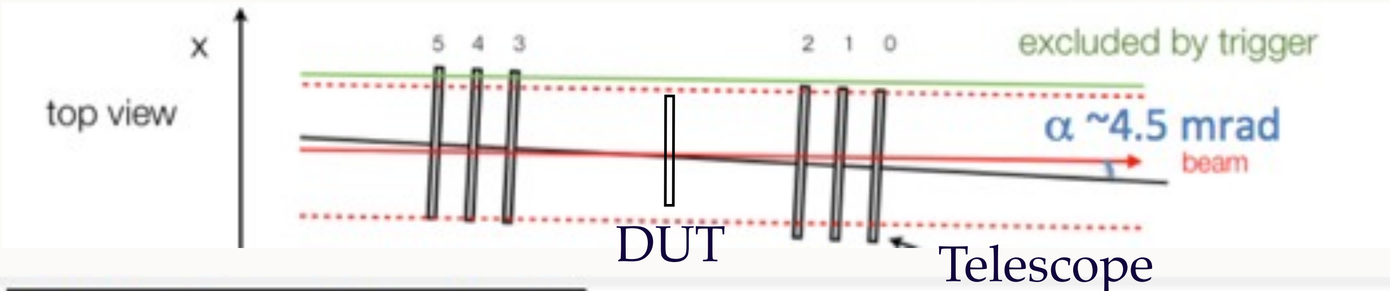


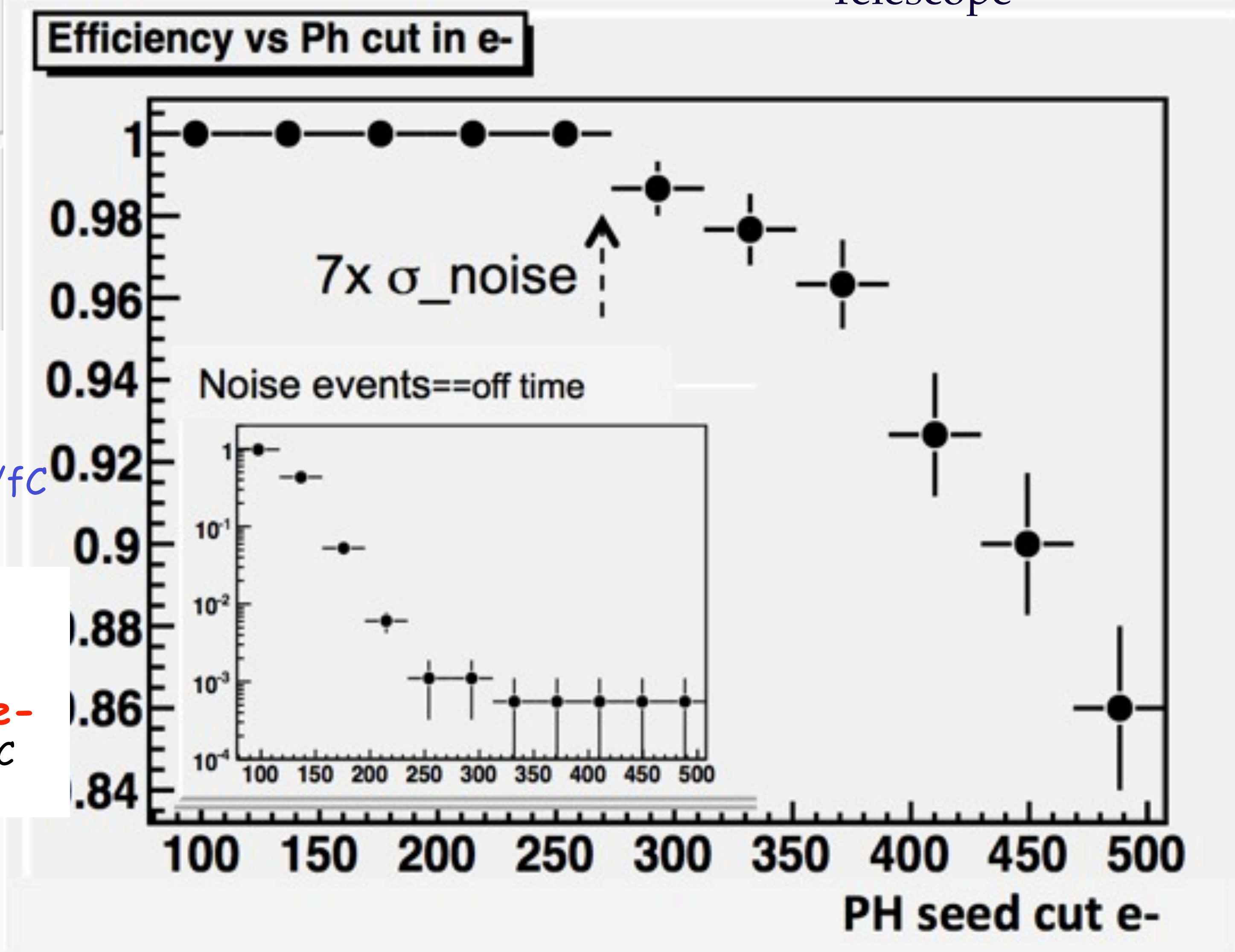
ENC = 45e$^-$

Gain = 320 mV/fC

SPS MIPS
S/N=23
MPV=1044 e-
Gain =320 mV/fC
(Fe55)

SPS beam test

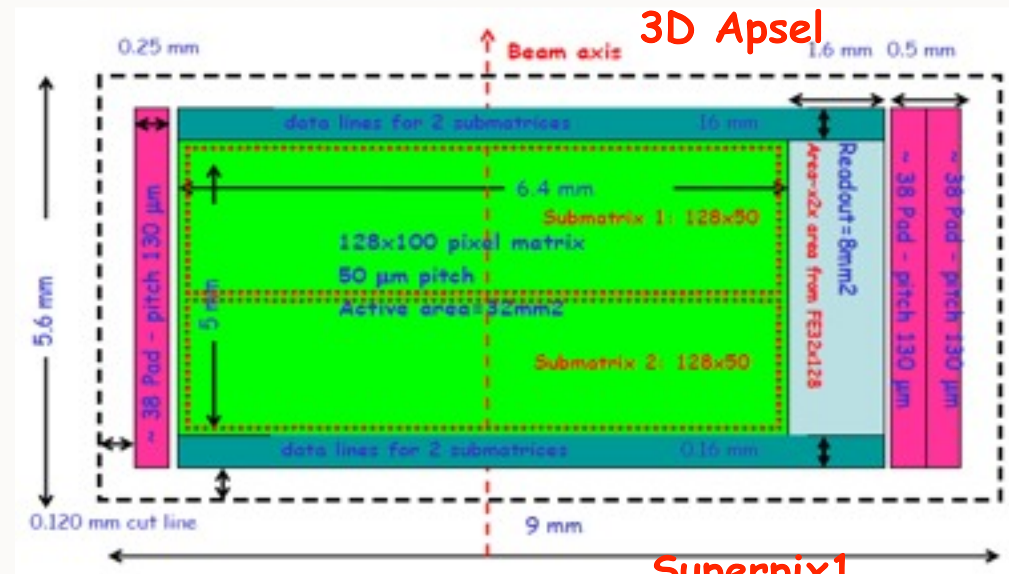


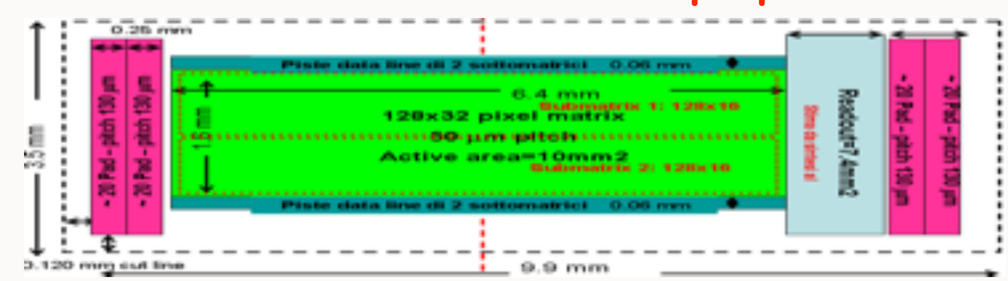


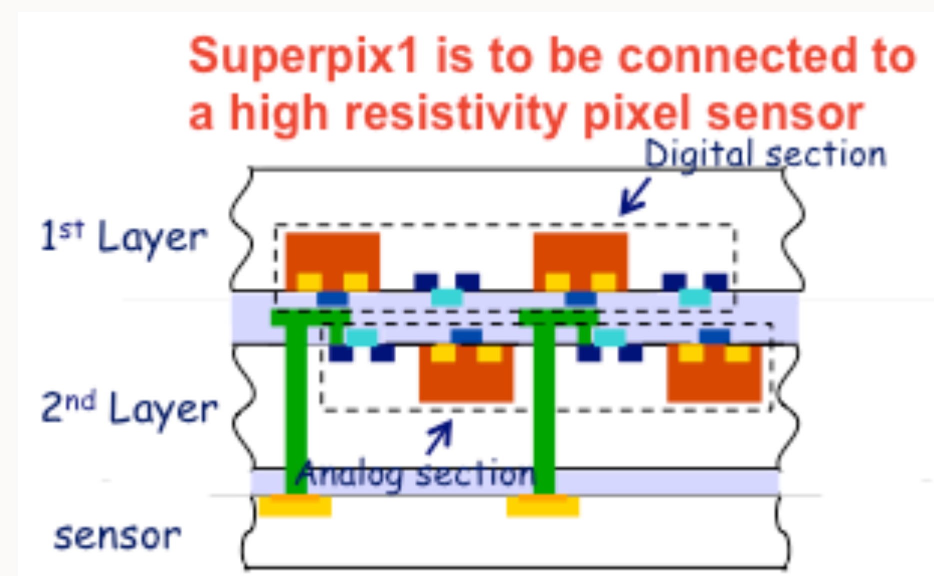
Next 3D Devices

- In the next 3D run (Tezzaron/GlobalFoundries) two pixel chips for SuperB Layer0 application:
  - **3D APSEL** larger CMOS MAPS matrix (128x100)
  - **Superpix1** FE chip for hybrid det. (128x32)
- Both chips share a new readout architecture: flexible: : data push & triggered version

	3D Apsel	Superpix1
Charge sensitivity	850 mV/fC	48 mV/fC
Peaking time	320 ns	260 ns
ENC	34 e rms	130 e rms
Threshold dispersion before/after correction	103/13 e	560/65 e
Analog power consumption	33 μW/pixel	10 μW/pixel
Detector capacitance	300 fF	150 fF
Matrix size	128x100	128x32
Pixel pitch	50 μm	50 μm







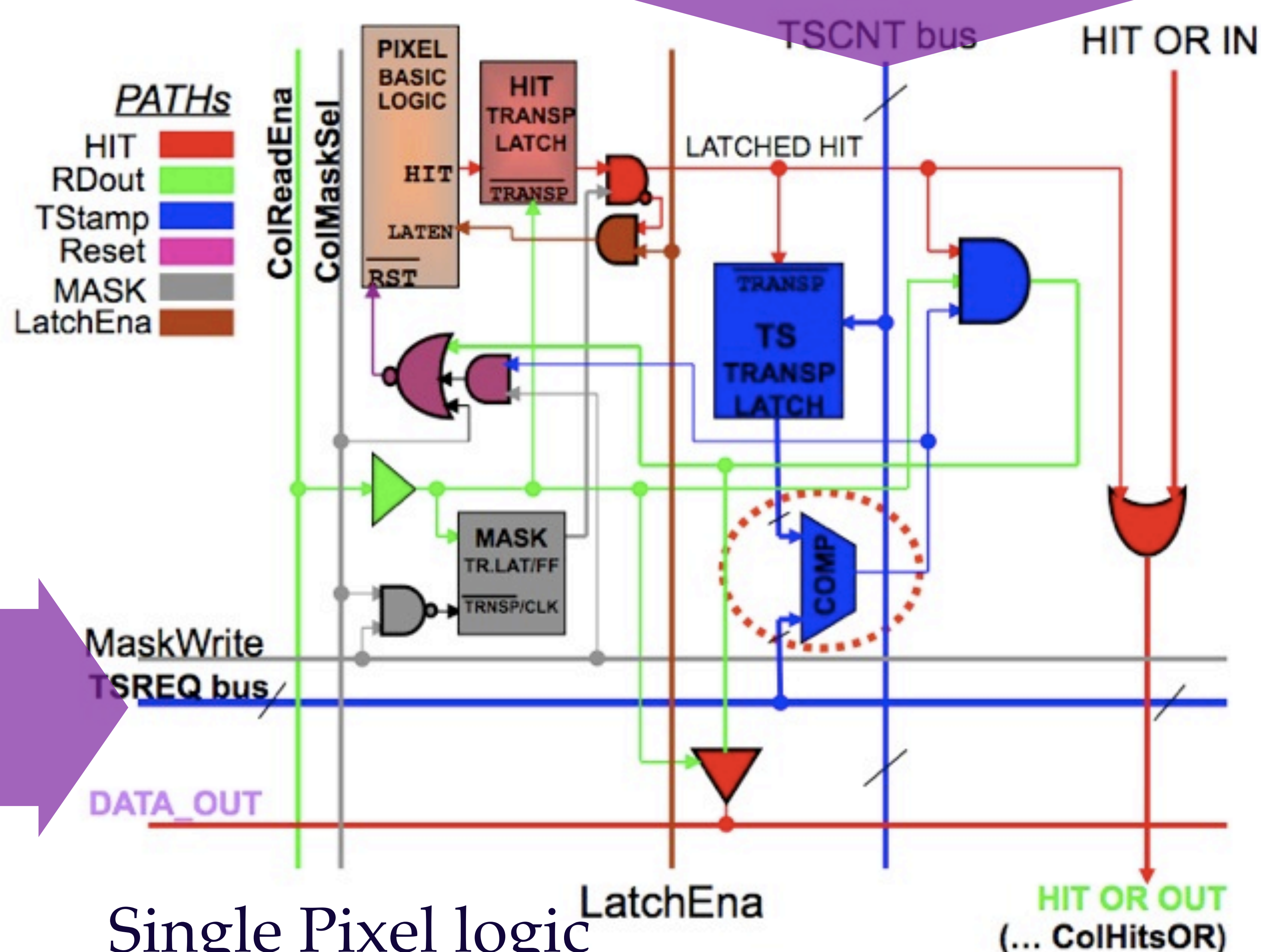
Flexible Read Out Architecture: Data Push *Or* Triggered

Matrix readout in Triggered mode is time stamp ordered

- The time stamp of the hit is stored at the pixel level and an HIT-OR-OUT is generated for columns with hits associated to that TS
- A column is read only if HIT-OR-OUT=1
- DATA_OUT is generated for pixels in the active columns with hits associated to that TS.

Time stamp broadcast to the whole matrix

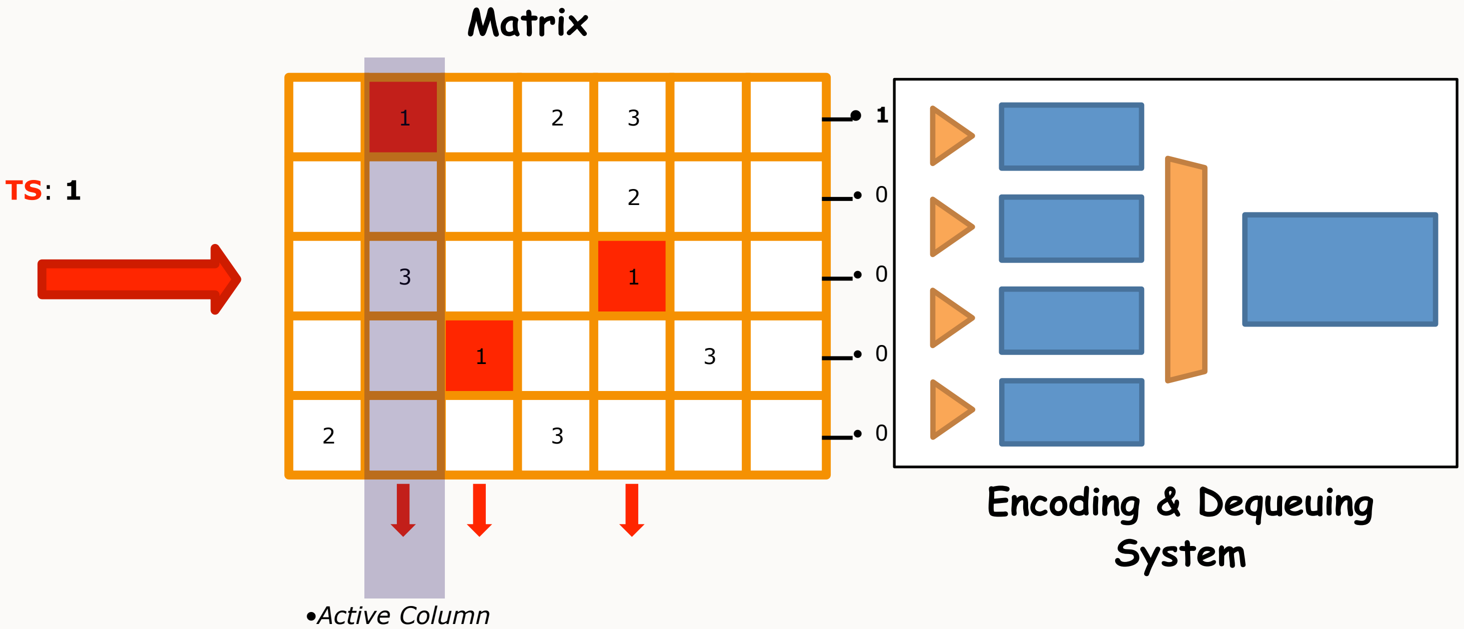
Time stamp of the requested hit

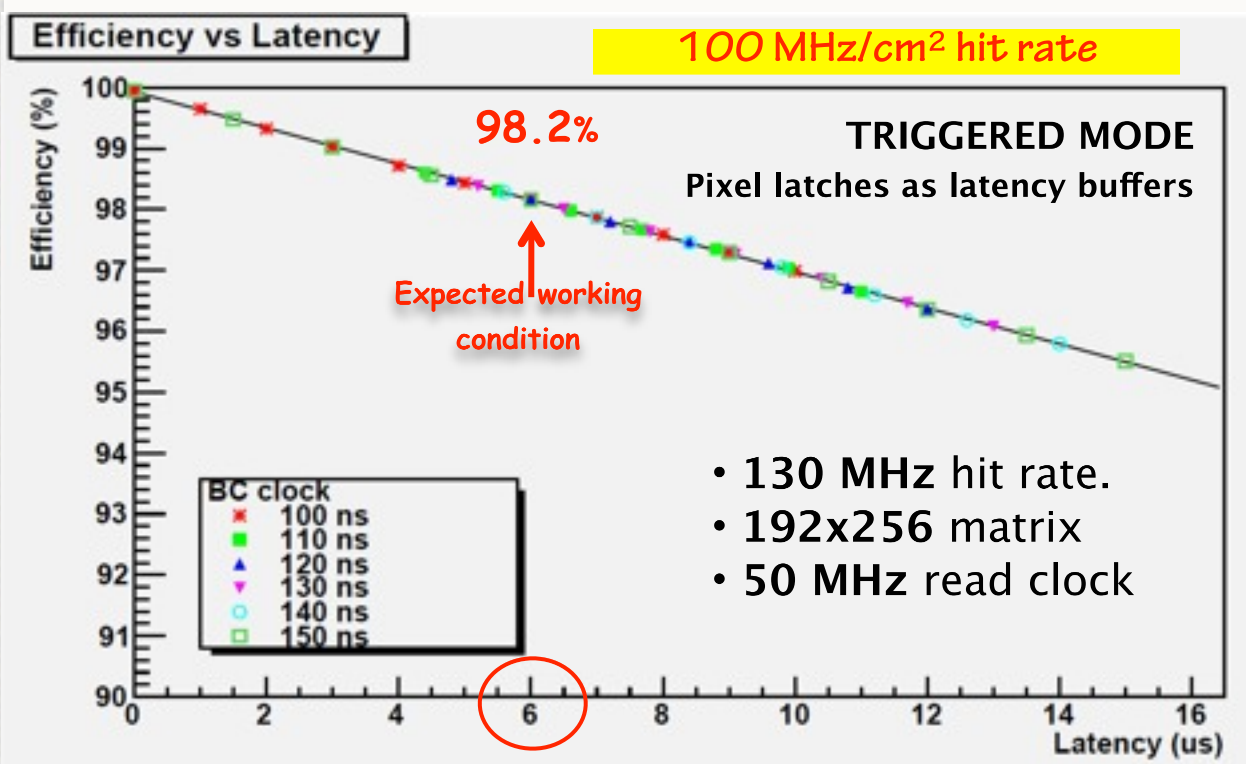


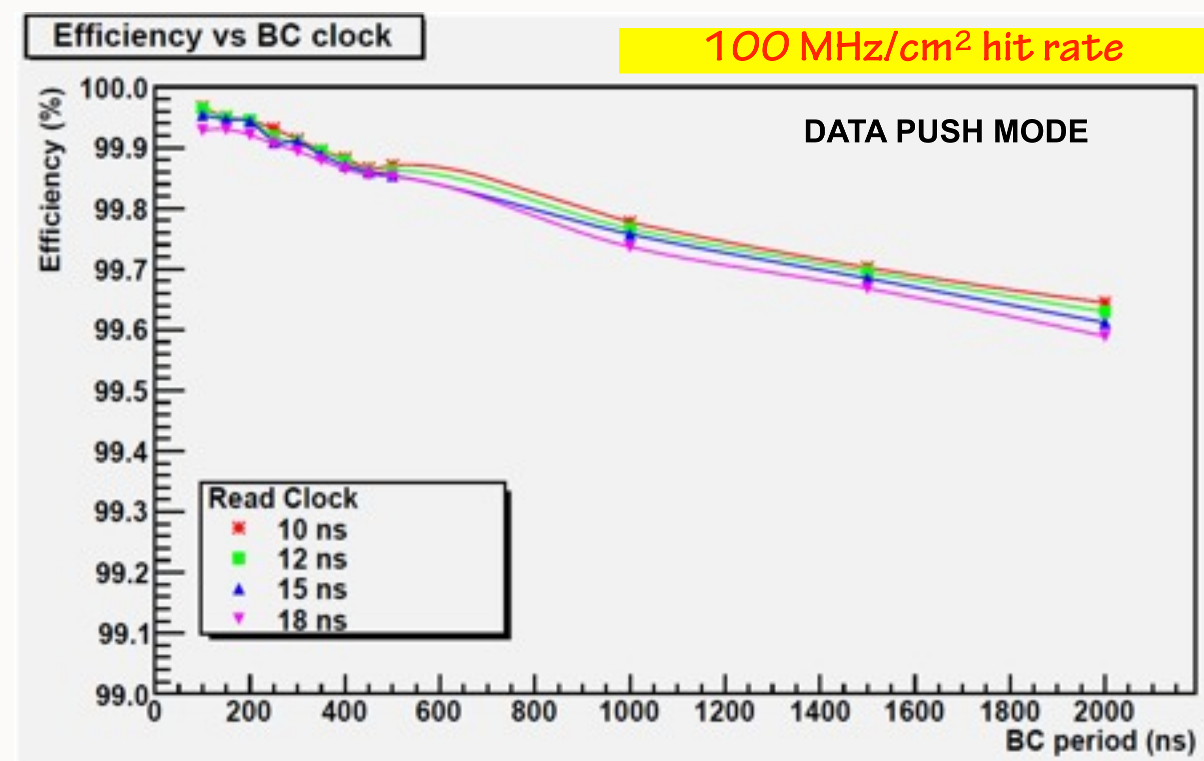
Single Pixel logic

Readout Architecture

- Both triggered and Data-Push mode
- Implemented in our INMAPS chips & ready for next 3D submissions
- Only active-FastOR columns are enabled in sequence. (i.e. if 10 active column FastORs then the whole matrix is read in 10 clock cycles)



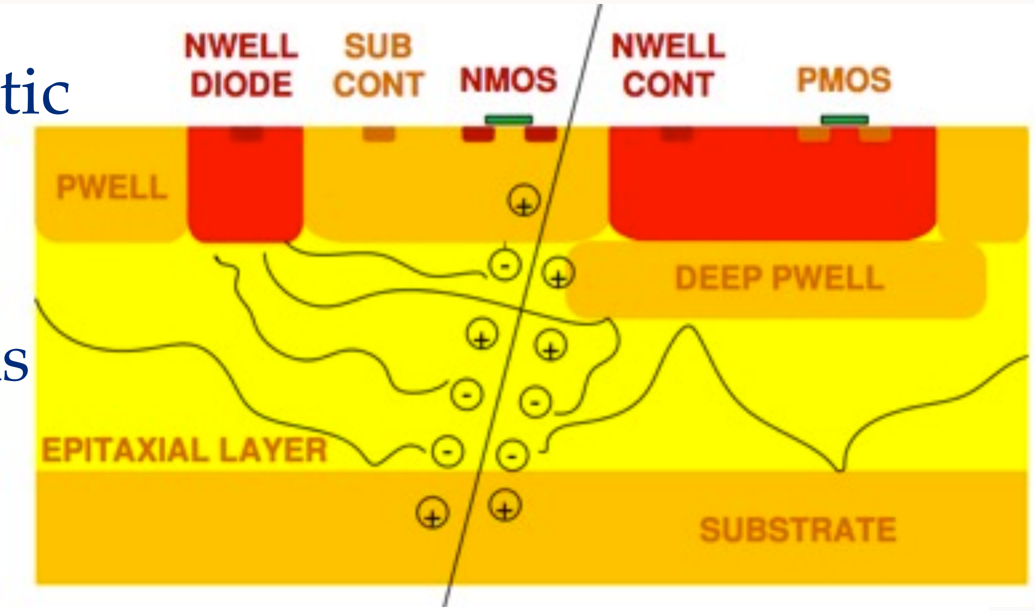




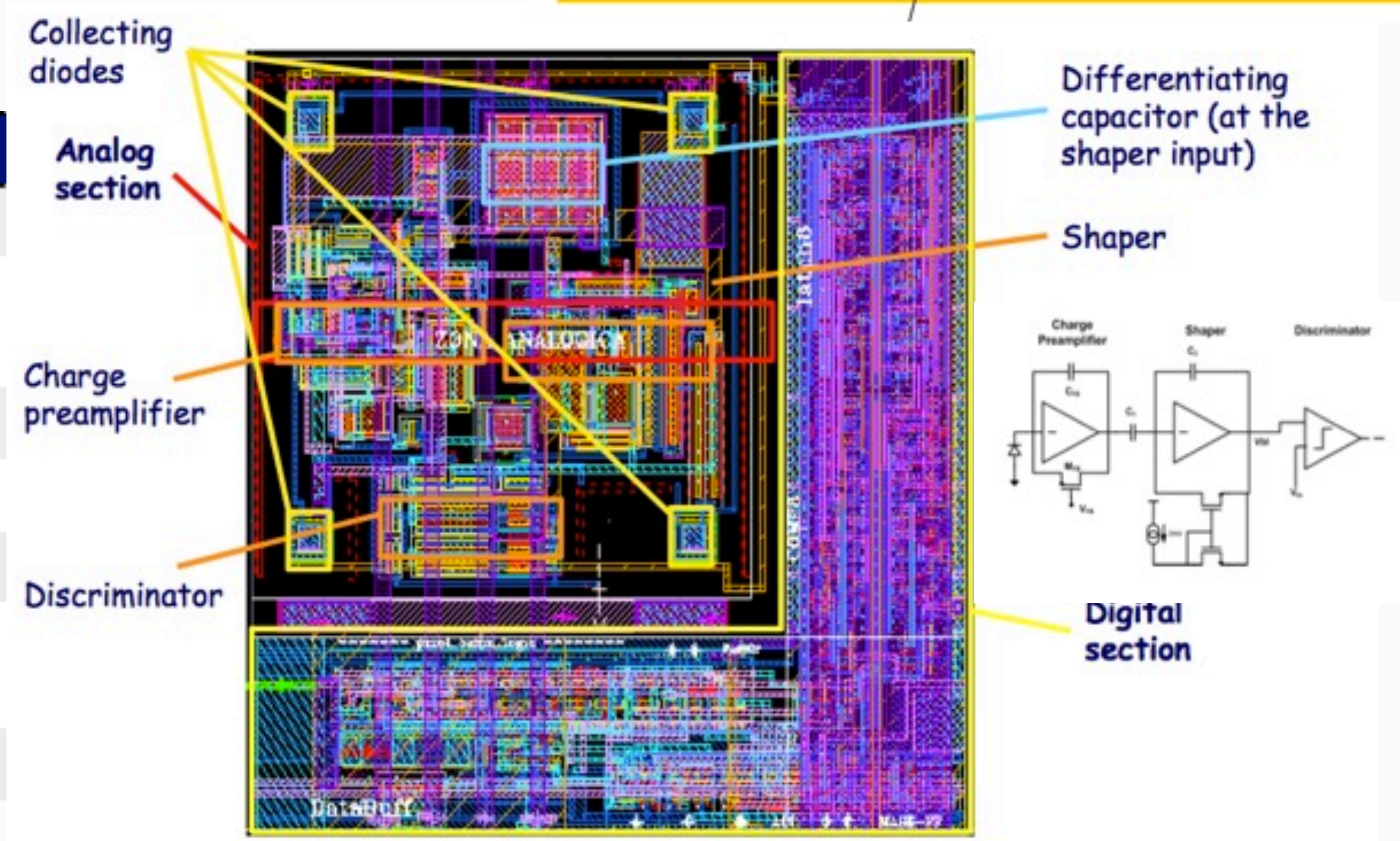
INNMAPS Developments

- Prevents the electrons to be collected by parasitic N-well by enclosing it in a deep P-well

- Improved charge collection efficiency by means of high resistivity epitaxial layer (~1 kΩ cm)



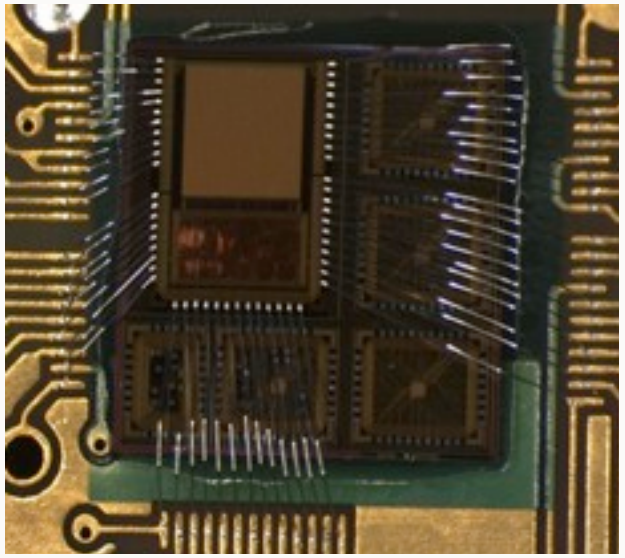
Apsel4well - Post Layout Simulation	
Charge sensitivity	930 mV/fC
t_p @ 800 injected electrons	240 ns
ENC (C_D = 30 fF)	26 e-
Threshold dispersion	23 e-
NLI (@ 2000e-)	1%
Analog Power consumption	18 μW/pixel
Pixel pitch	50 μm

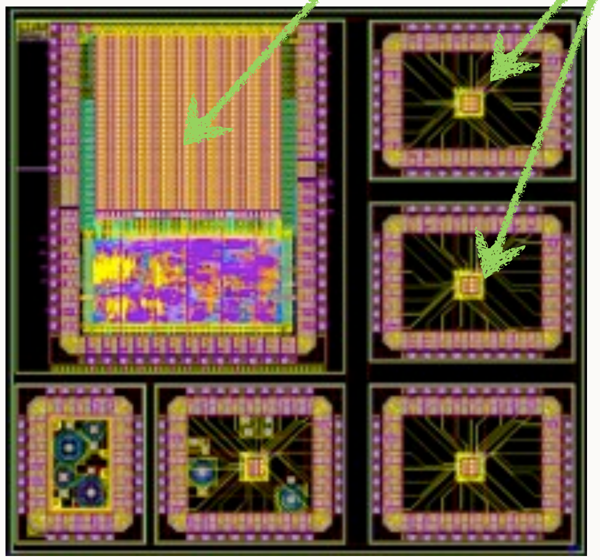


INMAPS Performances (3x3 Matrix)

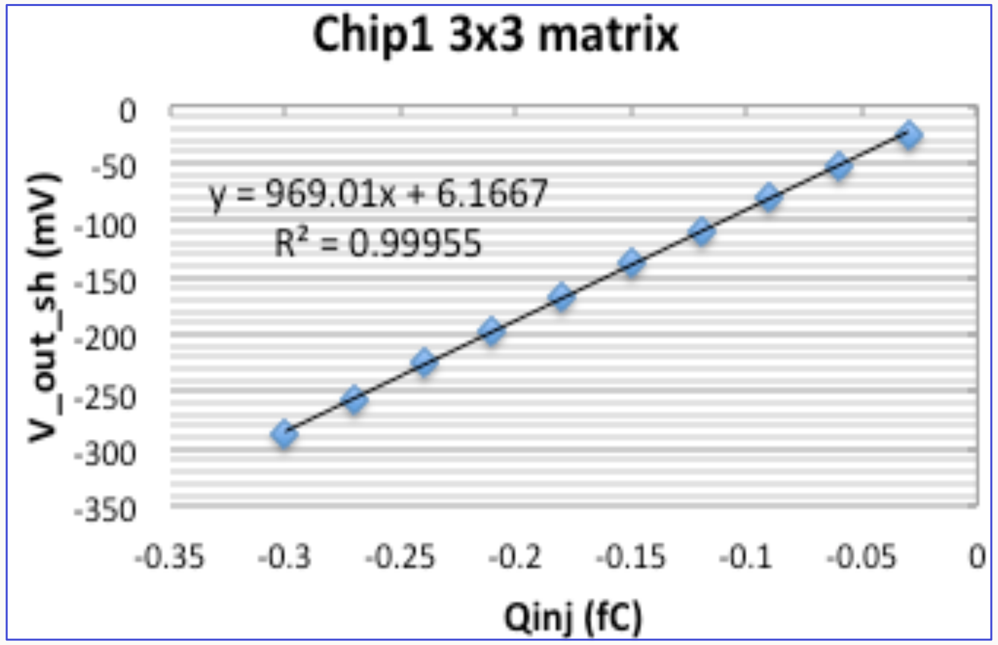
32x32 matrix with Digital R.O.

3x3 analog matrices





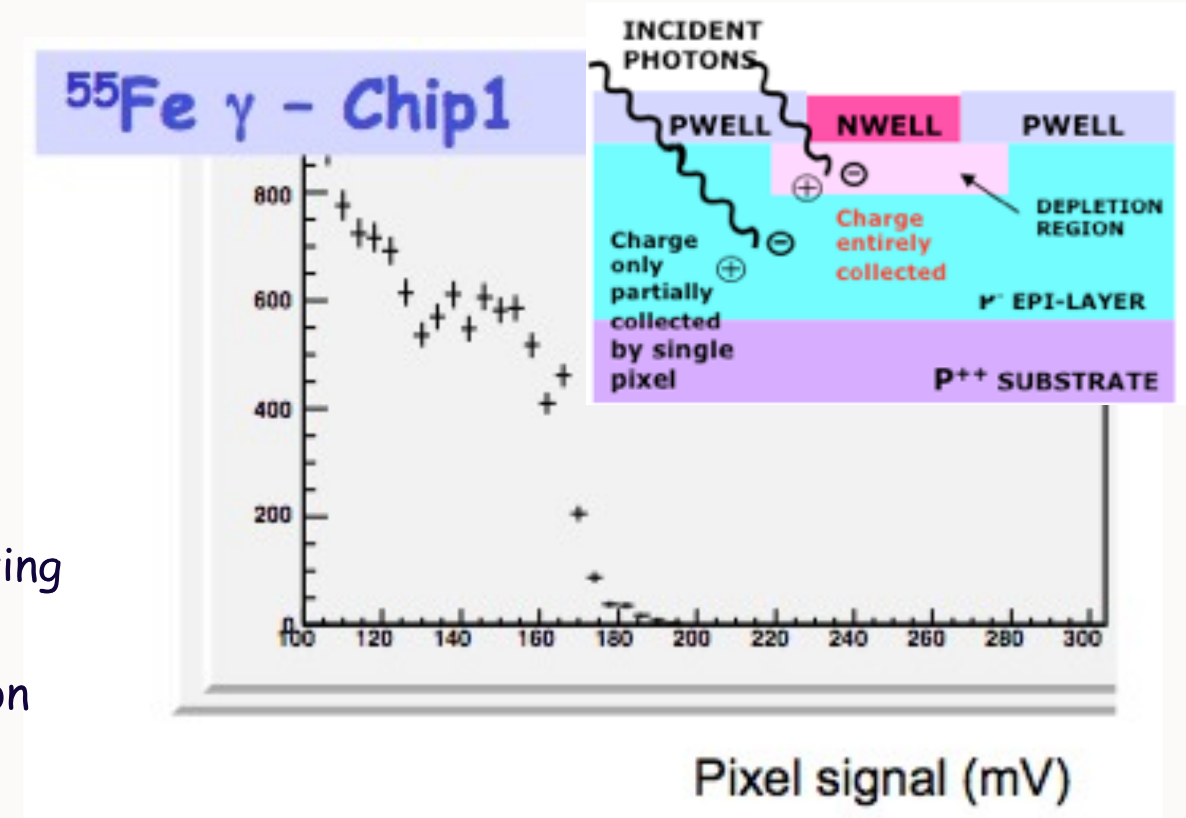
First chips under test now



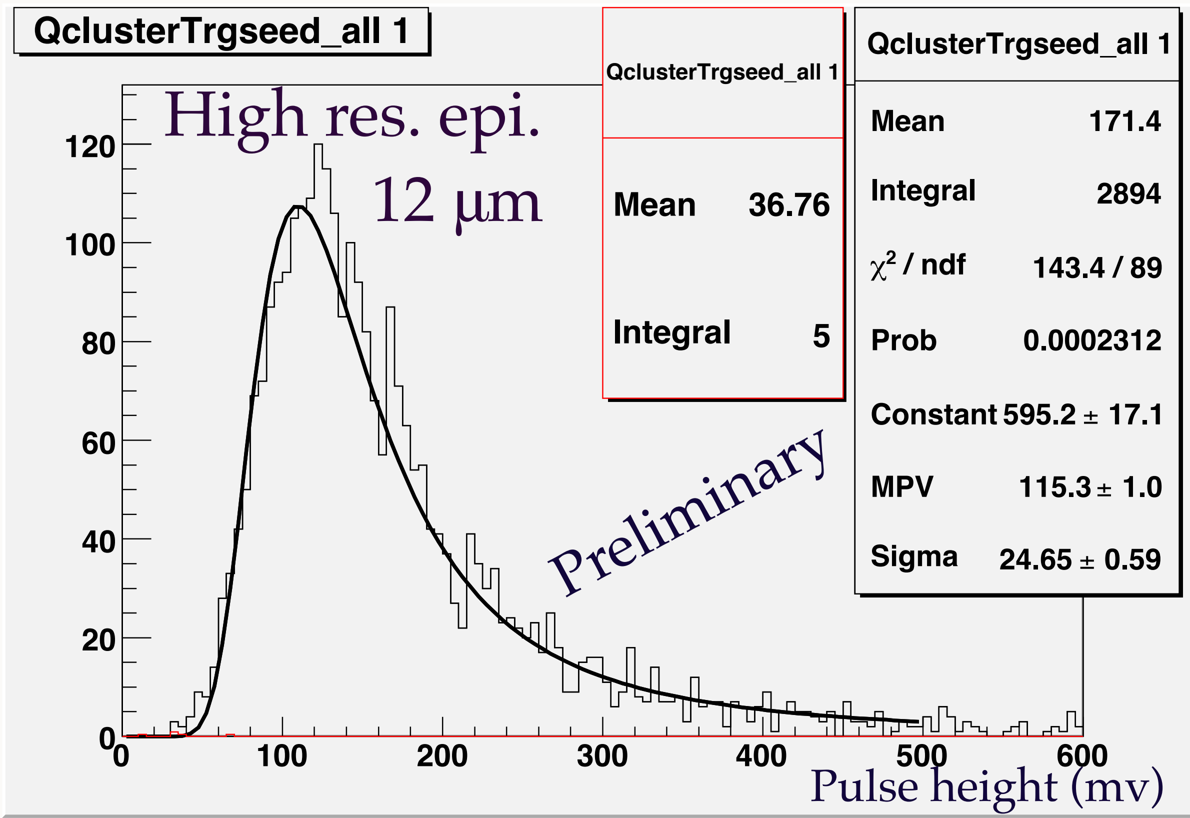
Noise and gain measured in 3x3 analog matrix in good agreement with PLS:

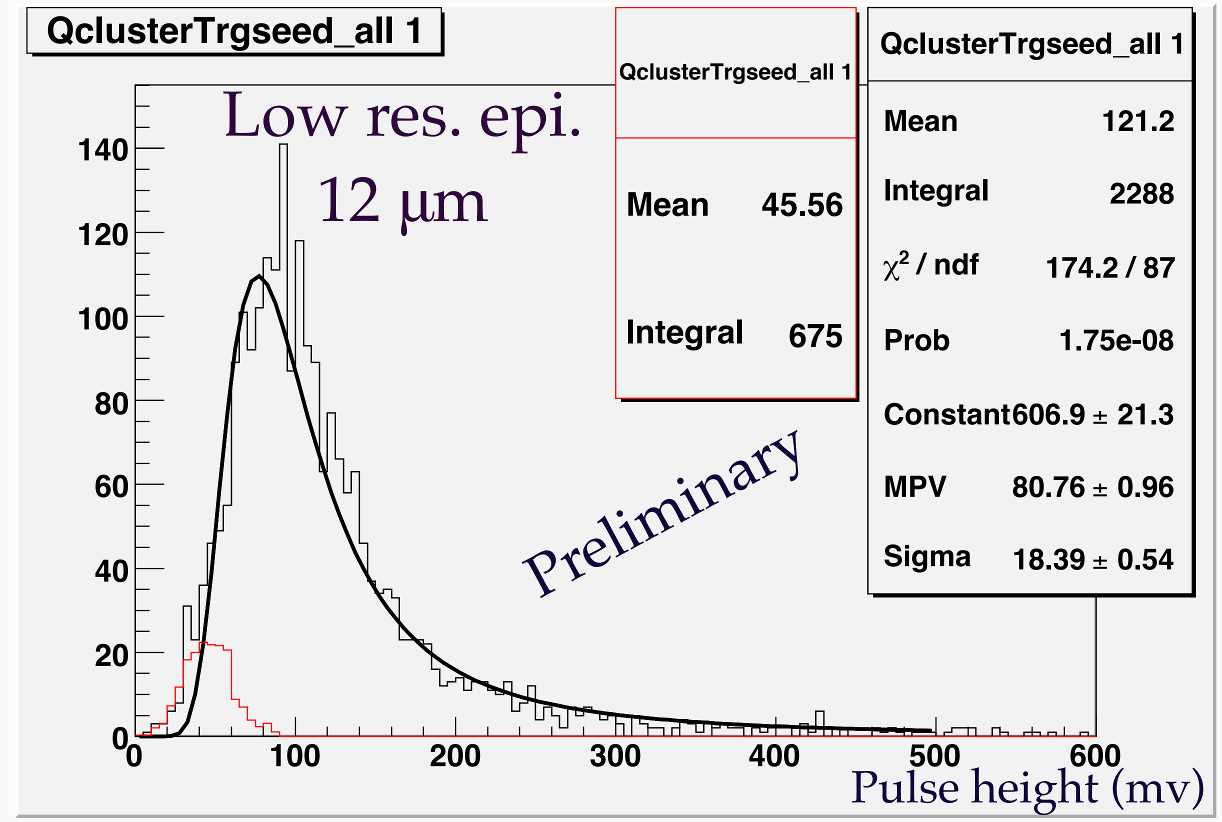
- ENC = 30 e- (~20% dispersion)
- Gain=920 mV/fC (~10% dispersion)

- ^{55}Fe γ: 5.9keV foto peak hardly visible due to very small diode area.
  - The charge is totally collected only for the γ interacting in the small depleted volume below the diode.
    End point (5.9 keV + 3 σ noise) used for gain evaluation (agreement within 10% with Cinj)

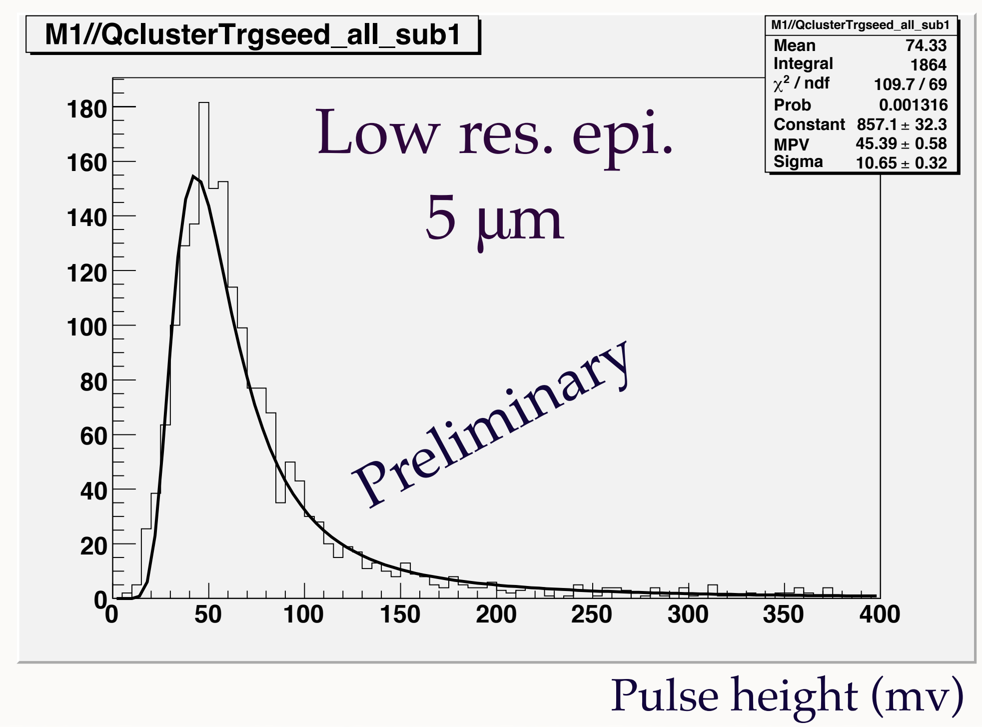


INMAPS ^{90}Sr Test Results



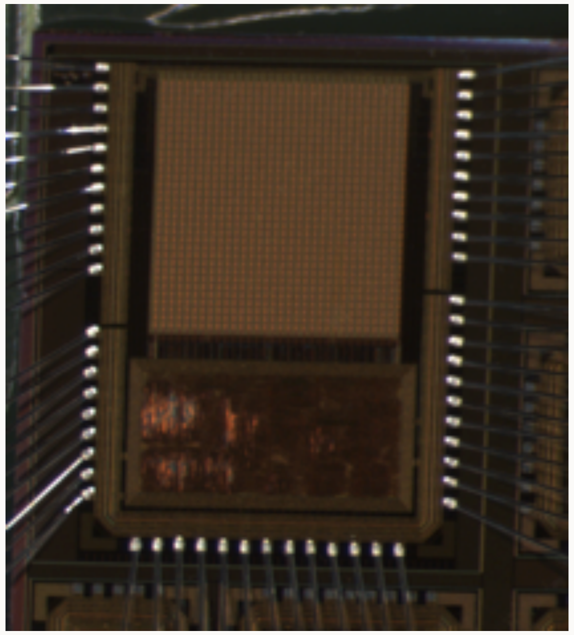


- The high resistivity INMAPS pixel collects ~ 800 e^-
- Beam test at CERN scheduled in November to test these devices with MIPS



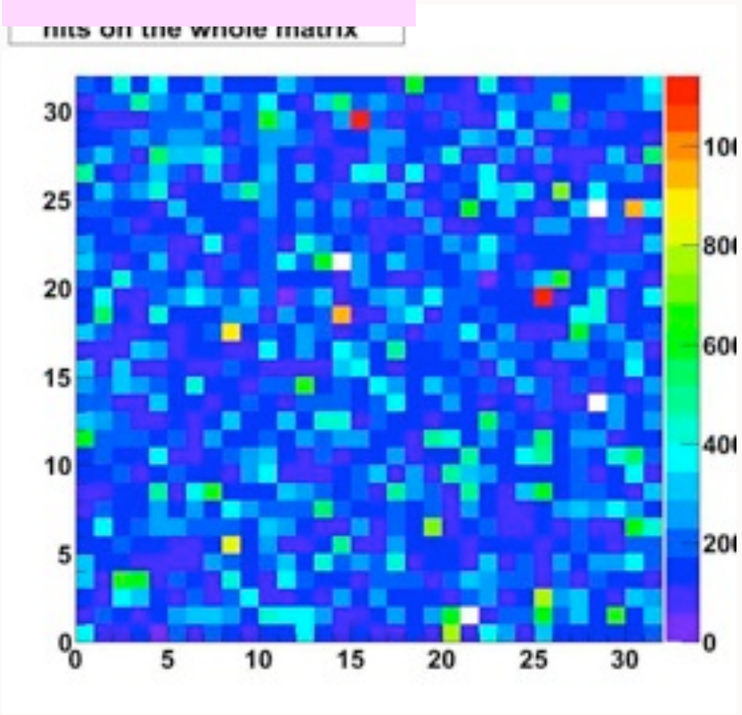
INMAPS 32x32 Digital R.O. Matrix

- Few dead pixels: ~ 0.3% (on 3 chips 32x32)
- Threshold and noise dispersion inside matrix measured with noise scans (occupancy vs discriminator threshold)
  - Threshold dispersion = 7mV (~ 2 xσ_noise)
  - Noise (+gain) dispersion ~ 35-40%
  - Further tests to evaluate the gain dispersion with the ^{55}Fe end point are ongoing.

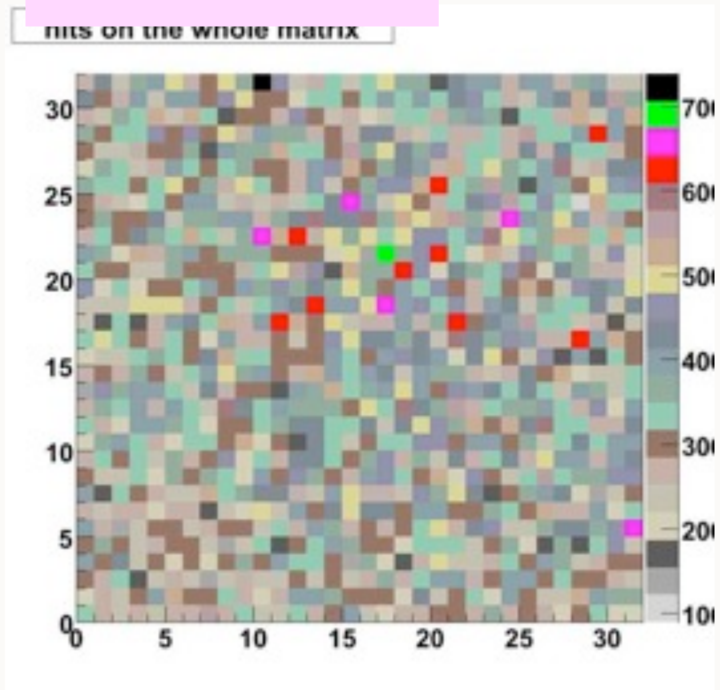


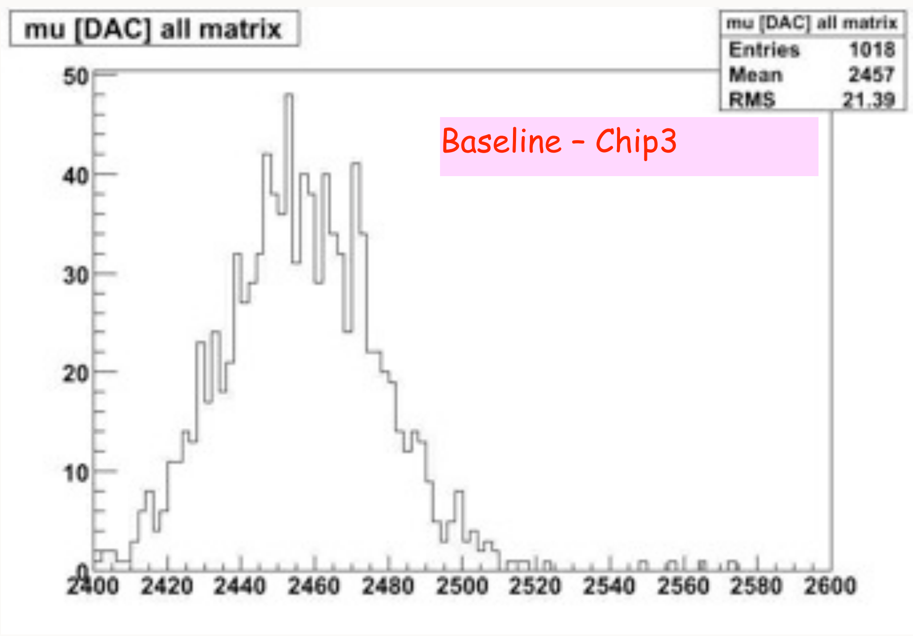
Preliminary

Noise hits - Chip3



^{90}Sr hits - Chip1

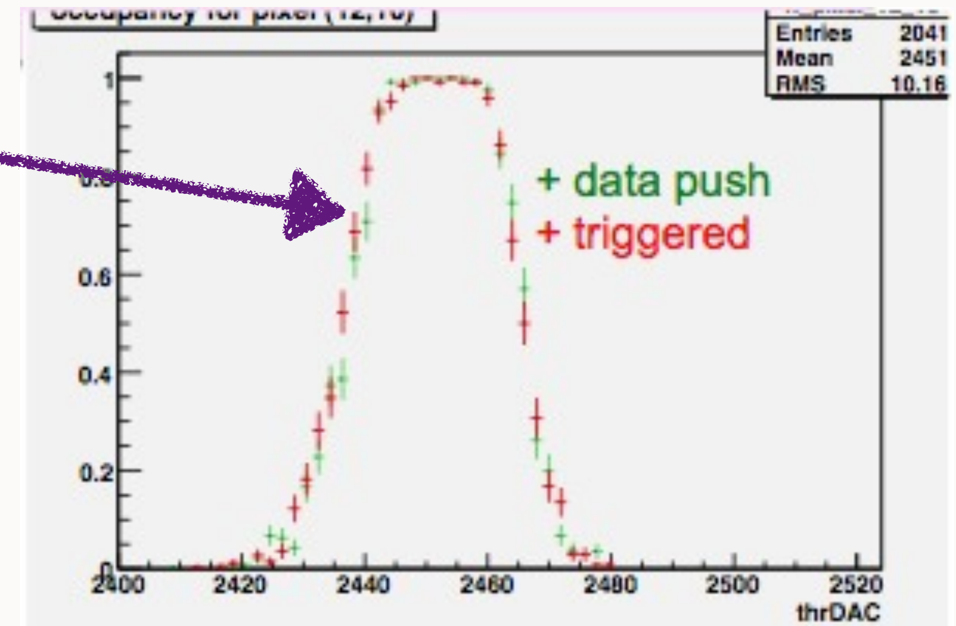




First Test Of The New Readout Architecture

- Standard functionality of new readout architecture verified in the two operation modes available on chip: data push (all TS readout) and triggered (only selected TS readout).

  1. Threshold scans almost identical in both operation modes
  2. Triggered mode also verified with specific test retrieving data injected at selected TS.



1. Pulse injection @ TS = 0
   → high threshold
      → no noise hits above threshold
2. Trigger arrives @ TS =2 with trigger latency setting = 3 TS
   → **triggered event TS = 0**
3. Data out stream info:
   - TS =0:1 fired pixel in submatrix1
   - TS =0: 0 pixels in submatrix0

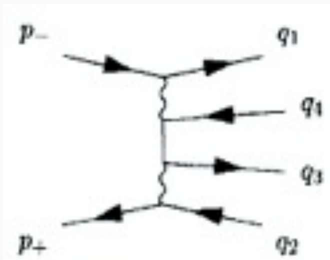
Conclusions

- The Super*B* project is proceeding together with the Cabibbo Lab to finalize both the Detector and Machine design
- The challenging requirements set on the SVT Layer 0 by physics measurements and background conditions can be met by the baseline option (striplets) but a more performant detector is highly desirable
  - tight material budget, read-out speed, radiation hardness
  - hybrid or CMOS MAPS are our present best candidates
- CMOS MAPS with triple-well process successfully realized and tested, but the overall efficiency and radiation hardness demonstrated to be marginal for SuperB
- The needed charge collection efficiency & readout performances improvements
  - 3D MAPS: good results on sensor+analog layer chips BUT can we access this technology in a reliable and stable way for the SuperB timeline?
  - 2D INMAPS devices can solve main limitations of DNW MAPS (collection efficiency and rad. hardness) with a reasonable R&D timeline for SuperB: … more test with beams and irradiations in next months!

APPENDICES/BACK UP

Pairs Production

$$\sigma \sim \frac{\alpha^2 r_e^2}{\pi} \left(\frac{28}{27} \ln^3 \frac{s}{m^2} - 6.59 \ln^2 \frac{s}{m^2} - 11.8 \ln^2 \frac{s}{m^2} + 104 \right)$$



$$e^+ e^- \rightarrow e^+ e^- e^+ e^-$$

- In this scattering event there is:
  - 1 track that hits the L0
  - this track fires 2 clusters in the L0
  - each cluster will be composed by one or more hits