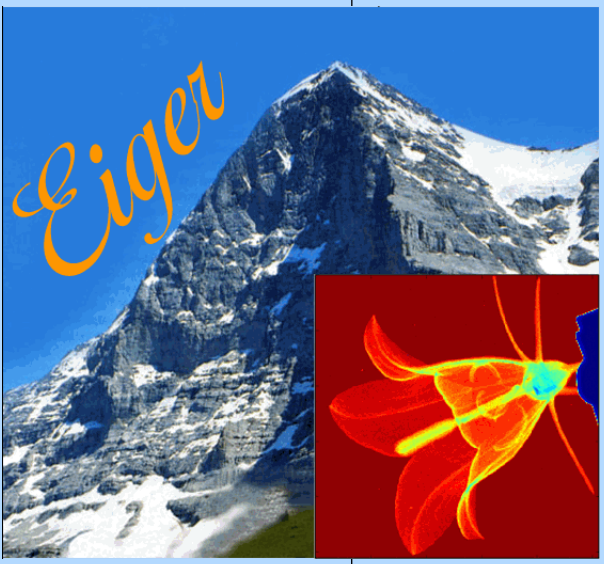
PAUL SCHERRER INSTITUT

PSI

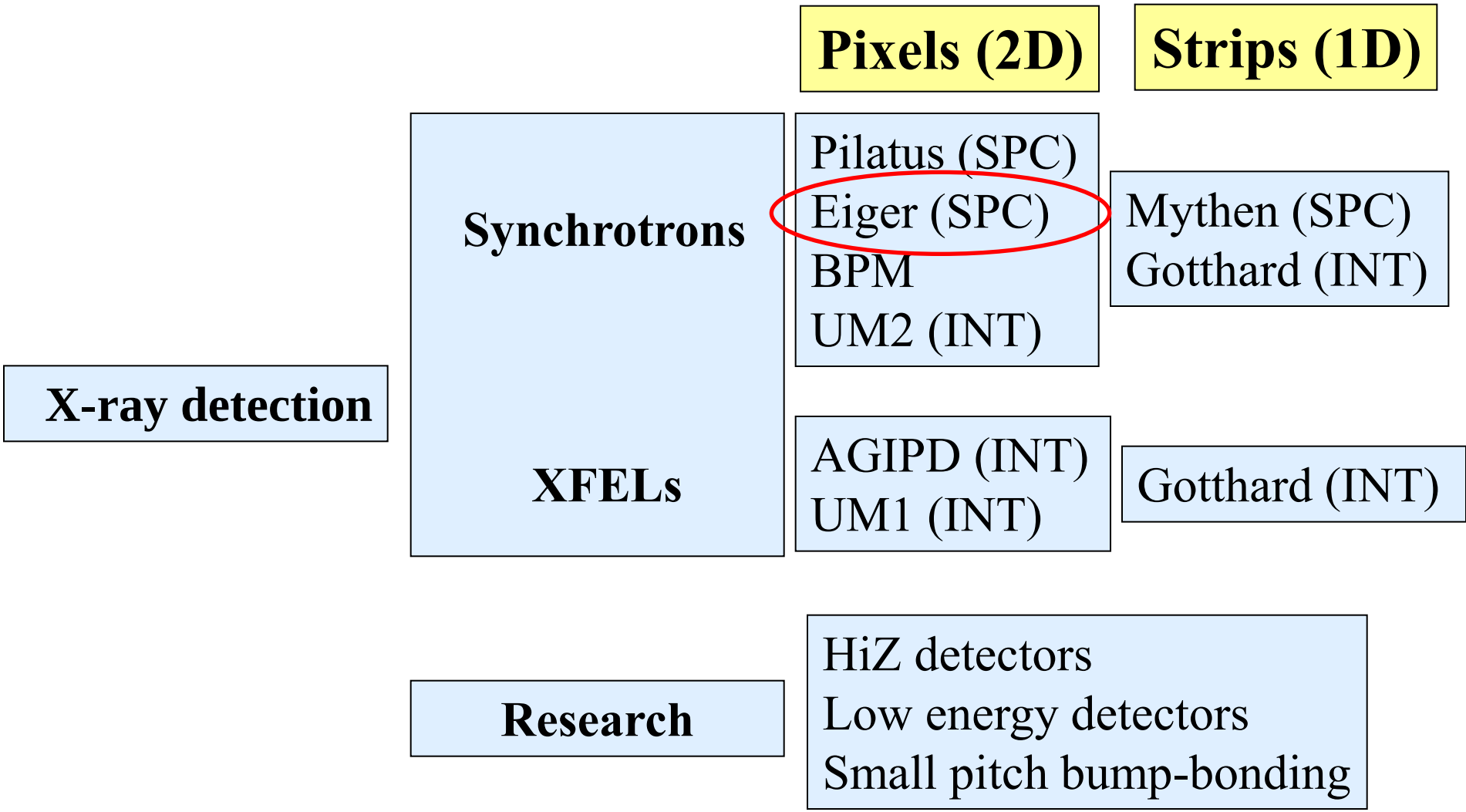
Wir schaffen Wissen – heute für morgen



Paul Scherrer Institut
Roberto Dinapoli roberto.dinapoli@psi.ch

EIGER characterization results

Chip design at the SLS Detector Group

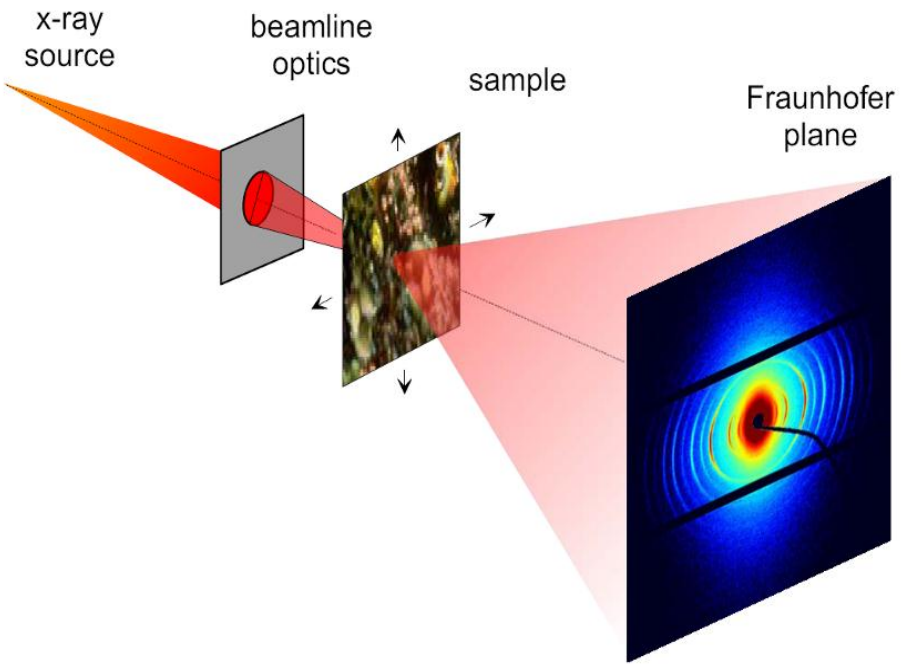


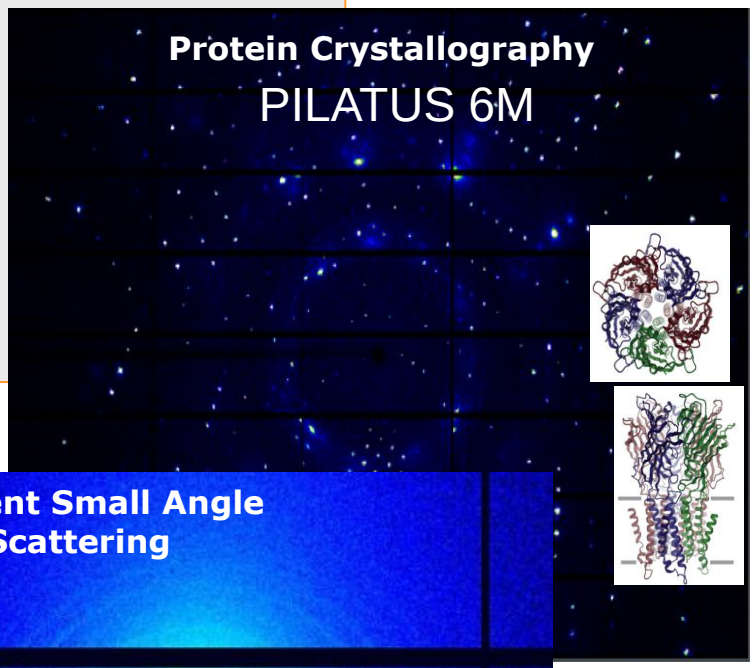
SPC= single photon counting; INT=charge integration
UM=unknown mountain, BPM= beam position monitor

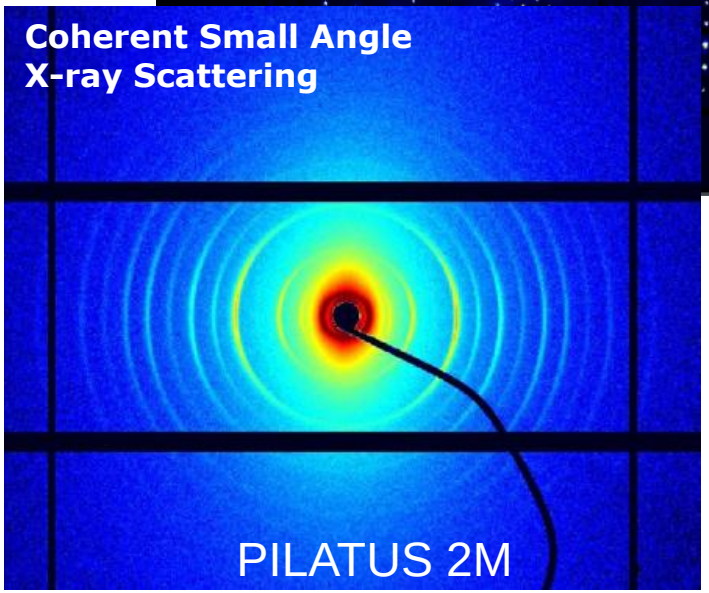
Applications of single photon counting detectors at the SLS

Single photon counting hybrid pixel detectors for synchrotron applications are aimed towards diffraction experiments

- Applications at CSAXs:
  - Scanning Coherent Small Angle X-ray Scattering
  - Coherent Diffractive Imaging
  - X-ray Photon Correlation Spectroscopy
- Protein Crystallography







Requirements for an ideal detector

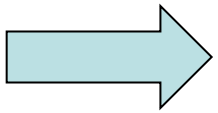
- Single photon resolution
- No spatial distortion and uniform response
- Large dynamic range
- Large area

→ PILATUS

No of Modules	60
Module size	487 x 195 pixels (90k)
Detector Size	431 x 448 mm^2
No of Pixels	2527 x 2463 pixels
	(6.2 * 10^6 pixels)
Spatial resolution	0.172 x 0.172 mm^2
Dynamic range:	20bits
Readout time	~2ms
Frame rate	5-10 Hz
Rate	1 MHz/pixel
Spatial distortion	Flat geometry
Dead area	~8.4 %

Requirements for an ideal detector

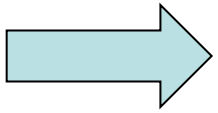
- Single photon resolution
- No spatial distortion and uniform response
- Large dynamic range
- Large area



PILATUS

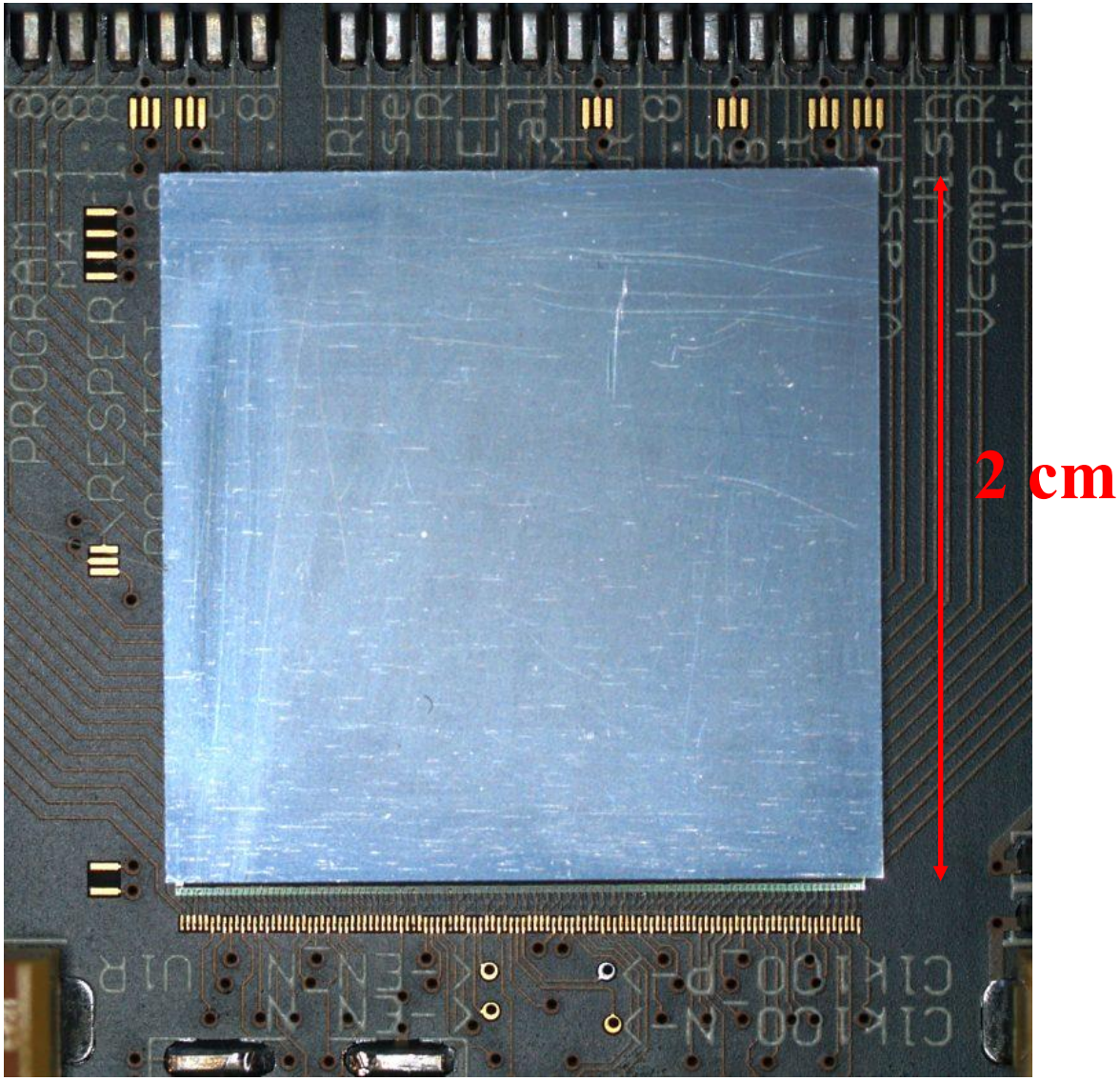
+

- Small pixel size
- Small dead area
- Fast Frame Rate
- Simultaneous exposure and readout
- Negligible dead time
- High count rate of incoming photons



EIGER

EIGER



EIGER main features (I)

Technological process	**UMC 0.25 µm**
Radiation tolerance	**Full radiation tolerant design (>4Mrad)**
Analog Parameters	**30 ns peaking time** **~150 ns ret. Zero** **8.8 µW/pixel = 2.3 /** **Gain: 44.6 µV/e-**
Chip size	**19.3 x 20.1 mm^2 (active 19.2x19.2mm^2)** **> 2 x**
Pixel size	**75 x 75 µm^2** **= / 5.3**
Pixel array	**256 x 256 = 65536** **= 11.3 x**
Count rate	**3.4 x 10^9 x-rays/mm^2/s = 5.3 x** **(1-2 Mcounts/pixel/s)**
Transistors, Matrix: **Periphery:** **Transistors density:**	**28.44M = 9.5 x** **>120 000** **430/pixel, ~5 x**

In red:
Improvement factor with respect to PILATUS

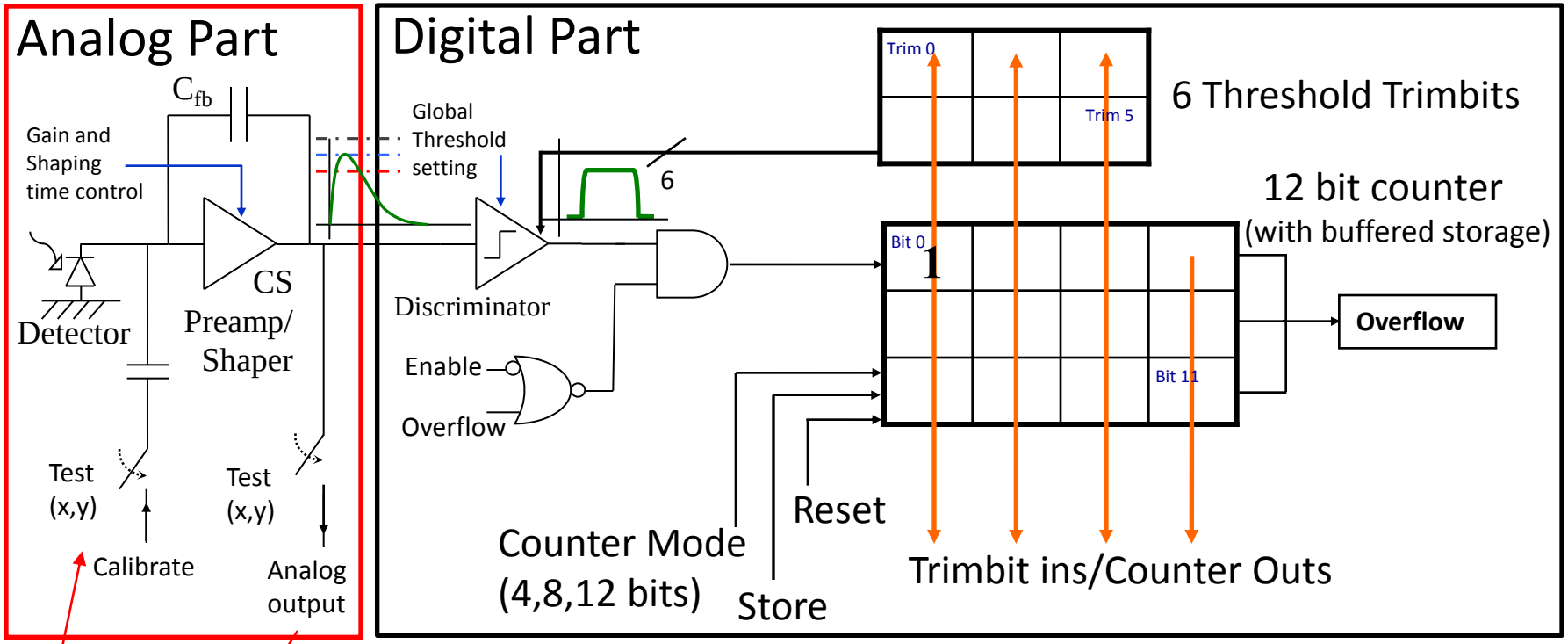
EIGER main features (II)

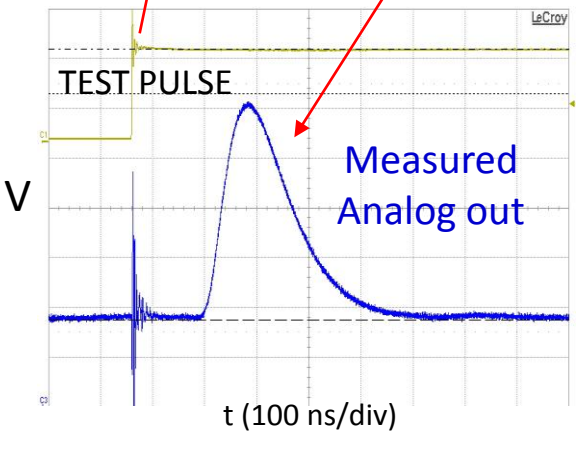
Nominal power supplies	**1.1 V (analog), 2V (digital), 1.8V (I/O)**
Counter	**12 bits, binary, configurable (4,8,12 bit mode), double buffered**
Continuous readout	**yes**
Detector readout speed	**~11 KHz @ 8 bit mode, (22 @ 4 bit)** **Detector size doesn't matter** **= up to ~2000 x (Clock=100 MHz DDR)**
Threshold adjustment	**6 bit DAC**
XY-addressable analog out for testing	**yes**
Overflow control	**yes**

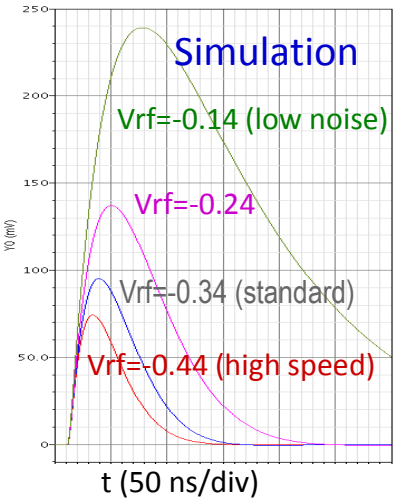
Both the chip and the readout electronics were totally redesigned, and almost all chip blocks are on silicon for the first time.

Project start: 02.2005, chip design as a one man project

The EIGER pixel

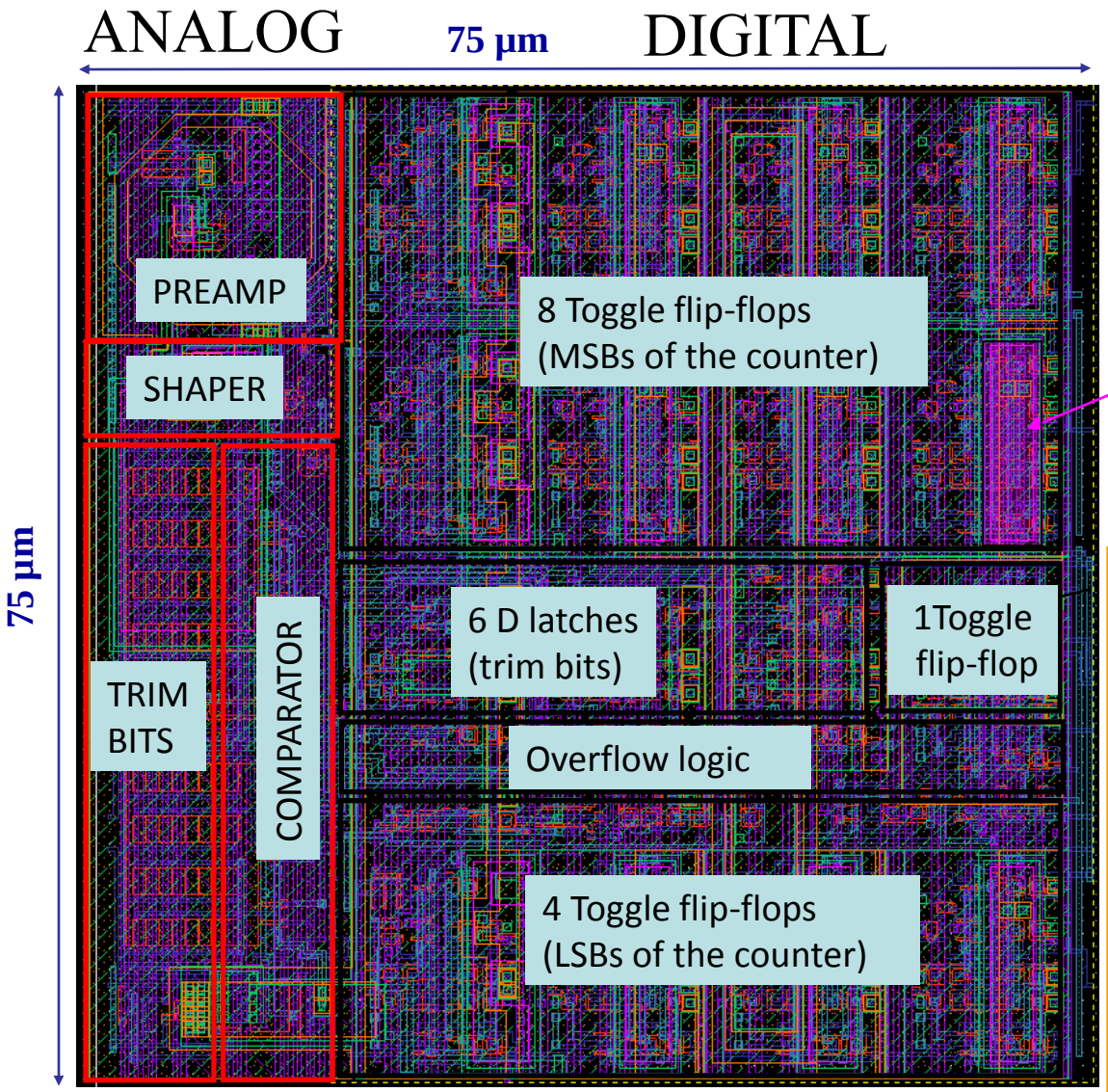




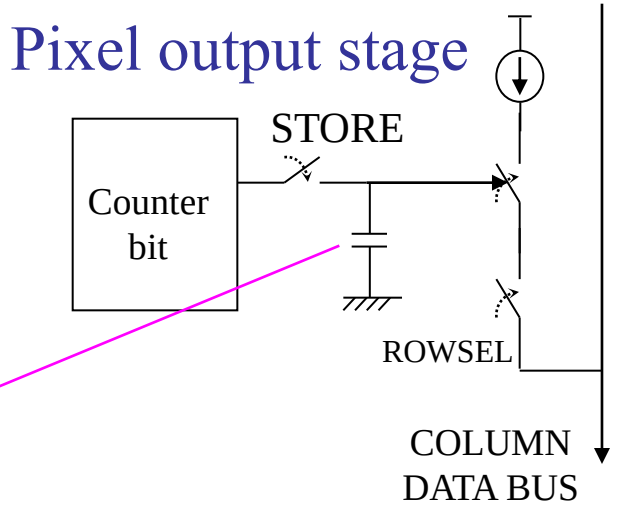


Gain	**44.6 µV/e-**
Timing	**151 ns (Ret.to 0 @ 1%)**
Noise (simul.)	**135 e-rms**
Static power	**8.8 µW/pixel (~0.6W/chip)**
Pixel counter	**12 bits, binary, double buffered (cont. readout), configurable (4,8,12 bit mode)**
Threshold adj.	**6 bit DAC/pixel**

The EIGER pixel on silicon

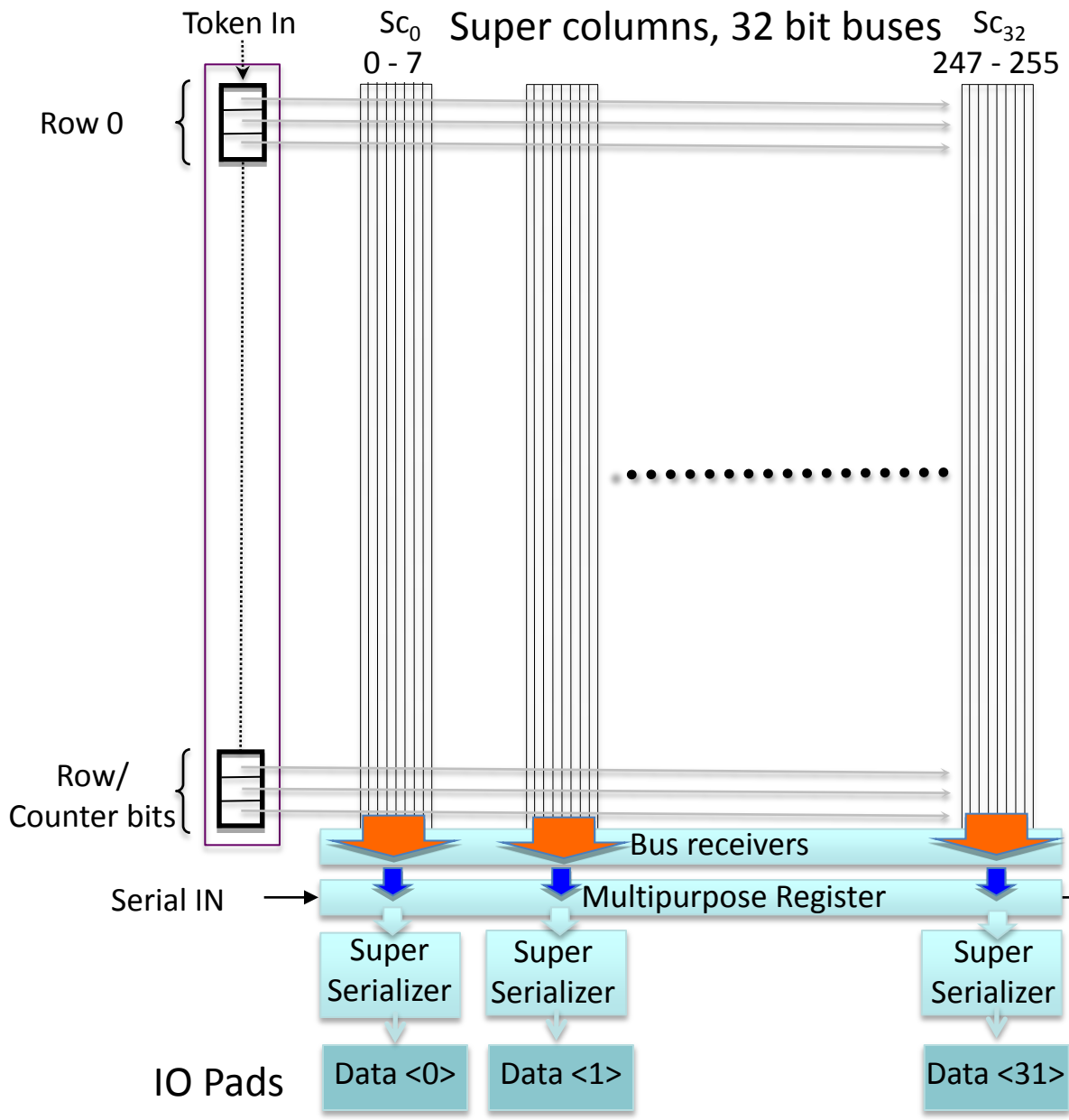


UMC 0.25 µm Technology, full radiation tolerant layout



- Bump bond connection
- Preamp (TWELL)/shaper
- Comparator
  - Global threshold plus pixel trimming (6 bits)
- 12 bit counter
  - Counter logic
  - Buffered storage
  - Trim latches
  - Overflow logic

EIGER readout architecture



Super column structure

- 8 columns/super column
- 32 super columns
- Current mode data buses

Token Shift Register

- Connects 4 bits of the counter storage cells or trimbits of a row to the bottom register

Bus receivers

- Perform I/V conversion

Multipurpose register

- Configurable serial/parellel I/O

Super serializers

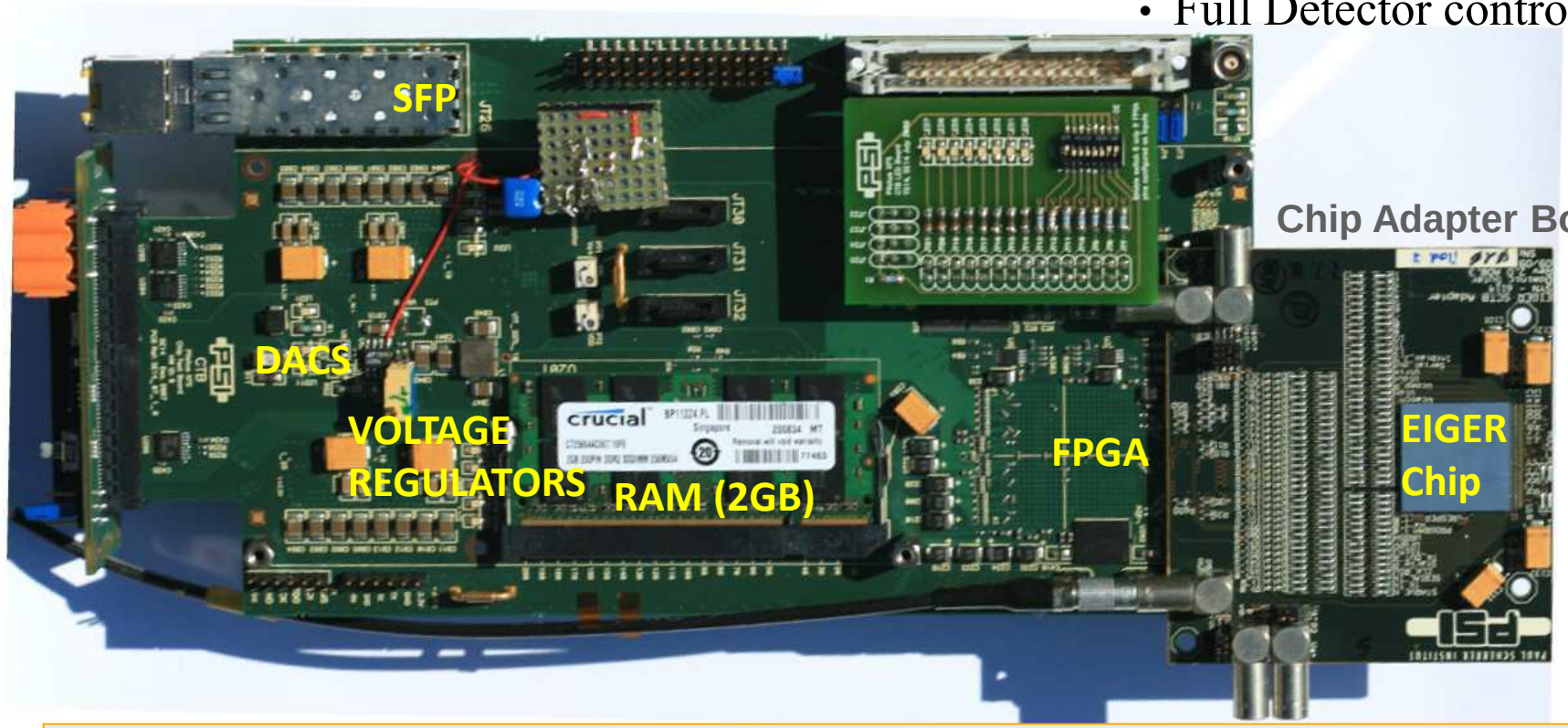
- Serialize data sent to the pad

32 Data pads

- 100 MHz DDR,TWELL

Single chip test setup

- Pattern generator
- Python scripts
- Full Detector control GUI



ALL WAFERS FROM FIRST FOUNDRY LOT WERE OFF SPECS!
Vth-P +100mV off, Vth-N +60mV off the nominal value.
We received 4 replacement wafers (for free, LOT 2) which meet the specs (and work much better)

Single chip calibration plan

❑ The samples

- several single **chips** tested with an **XRay tube and Fluorescence samples** for Trimming and Calibration.

- **1 chip tested** at the **PSI-Optics beam line** in two different periods (25-27/02/2011 and 17-21/03/2011). E=10-16KeV

Identify three modes of operation

- ➢ Fast
- ➢ Standard
- ➢ Low Noise

❑ Single Chip Calibration Plan

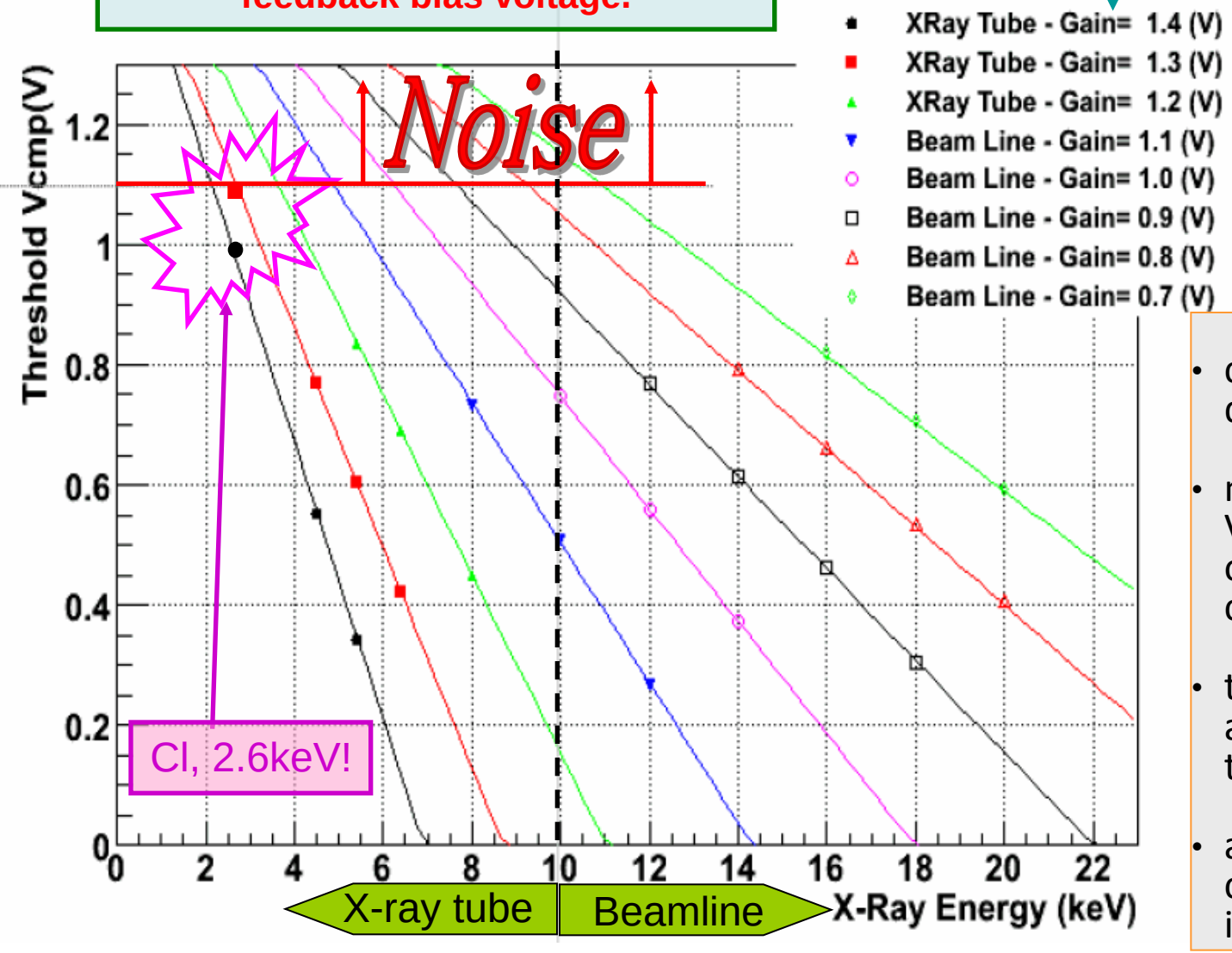
Start with DACs settings from simulation
Optimize the DACs
Define a threshold trimming procedure
Measure different detector characteristic

- Energy calibration
- Noise
- Threshold dispersion
- Rate Capability
- Minimum Energy
- Radiation tolerance

Irradiation tests performed at the beam line with LOT 2 show that the chip is still operational after several tens of Mrad with minor re-biasing

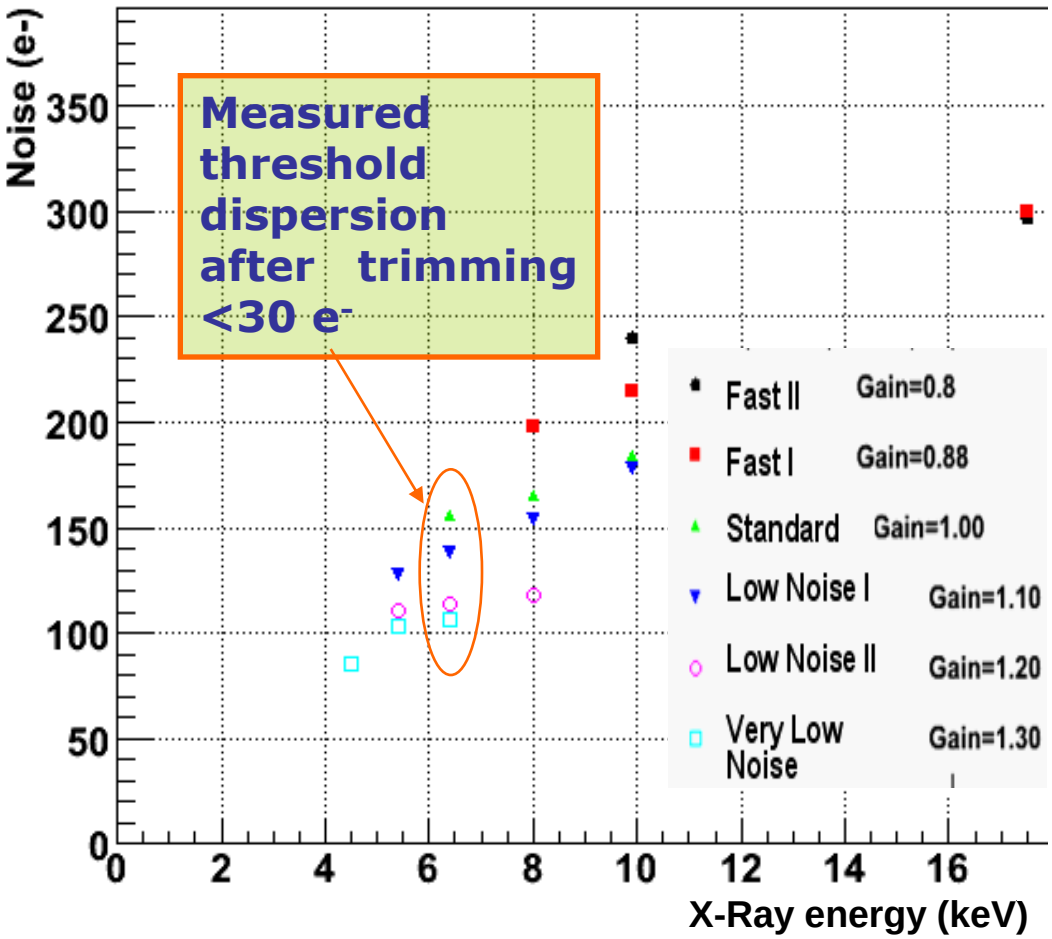
Threshold calibration and low energy operation

Gain: setting of the preamp feedback bias voltage.



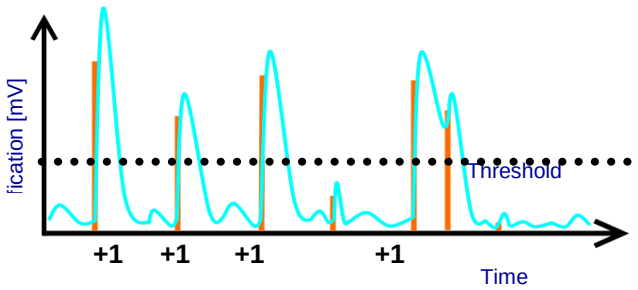
- comparator is linear down to low energies
- minimum threshold Vthr ~1.1V; safe operation of the comparator @ 1V
- threshold energy as low as 2.5keV can be set in the highest gain mode
- a further higher gain could also be investigated

Noise and threshold dispersion



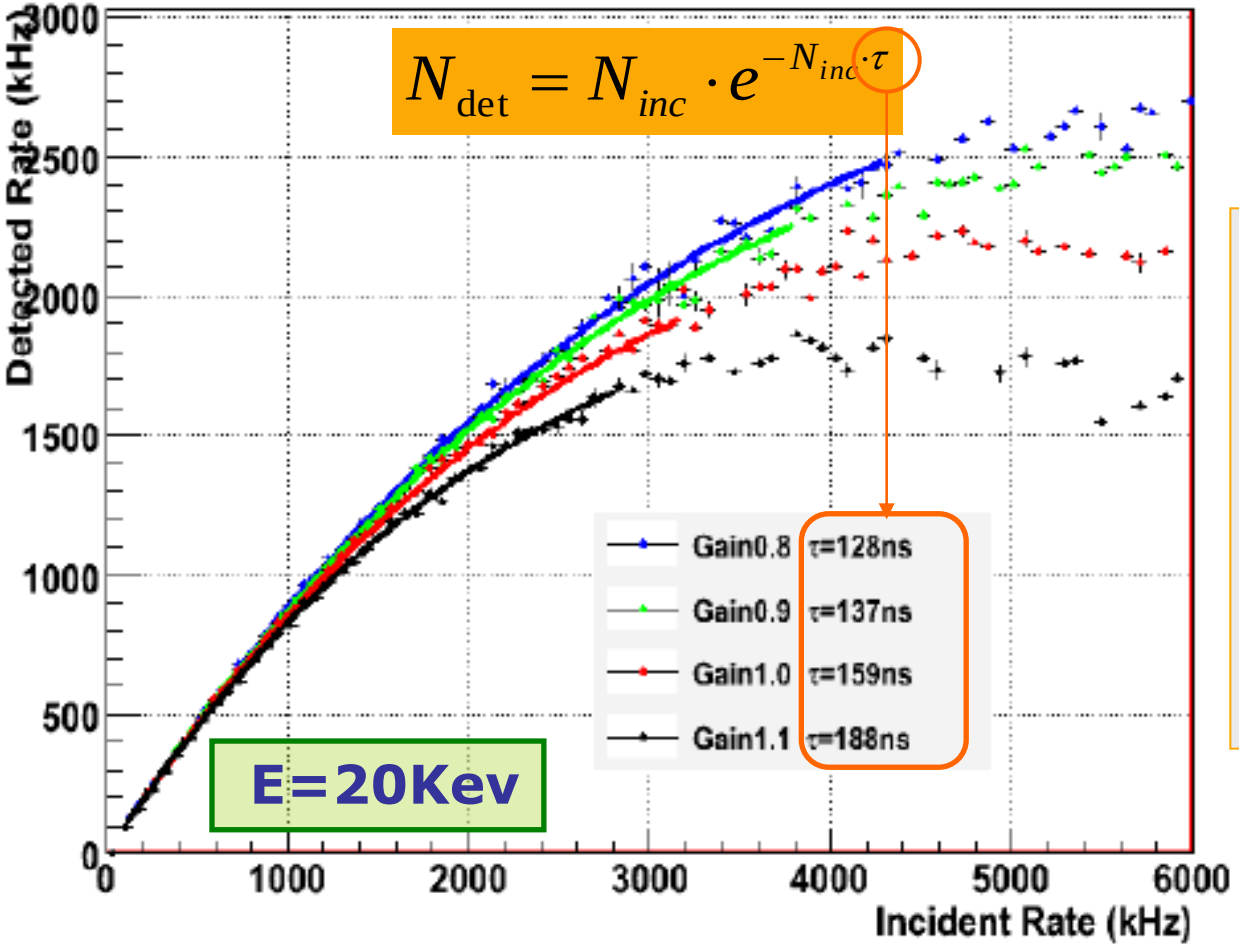
The plot shows the noise performance as a function of the photon energy for different preamp settings. In "very low noise" mode the chip has a noise of ~100 e-. Threshold dispersions of <30 e- were also measured.

Rate Capability



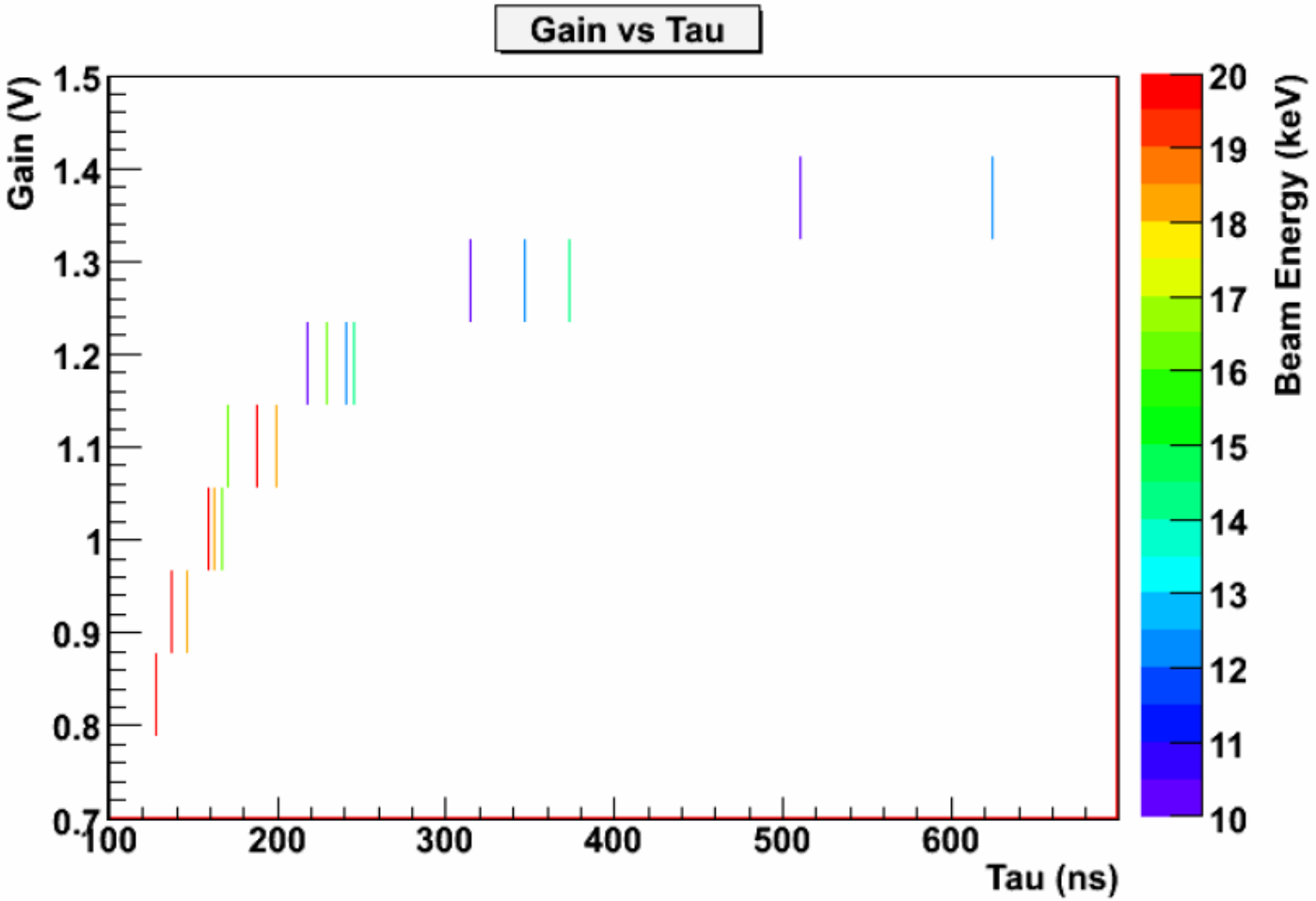
RATE CAPABILITIES

$$N_{\det} = N_{inc} \cdot e^{-N_{inc} \cdot \tau}$$



- **Rate Capability:** monochromatic beam 20KeV
- Scattering of direct unfocused beam
- Al. filters to reduce the flux
- In each mode of operation Vcmp set @ half energy

Eiger Calibration



X-ray Images, single chip

Dried anchovy

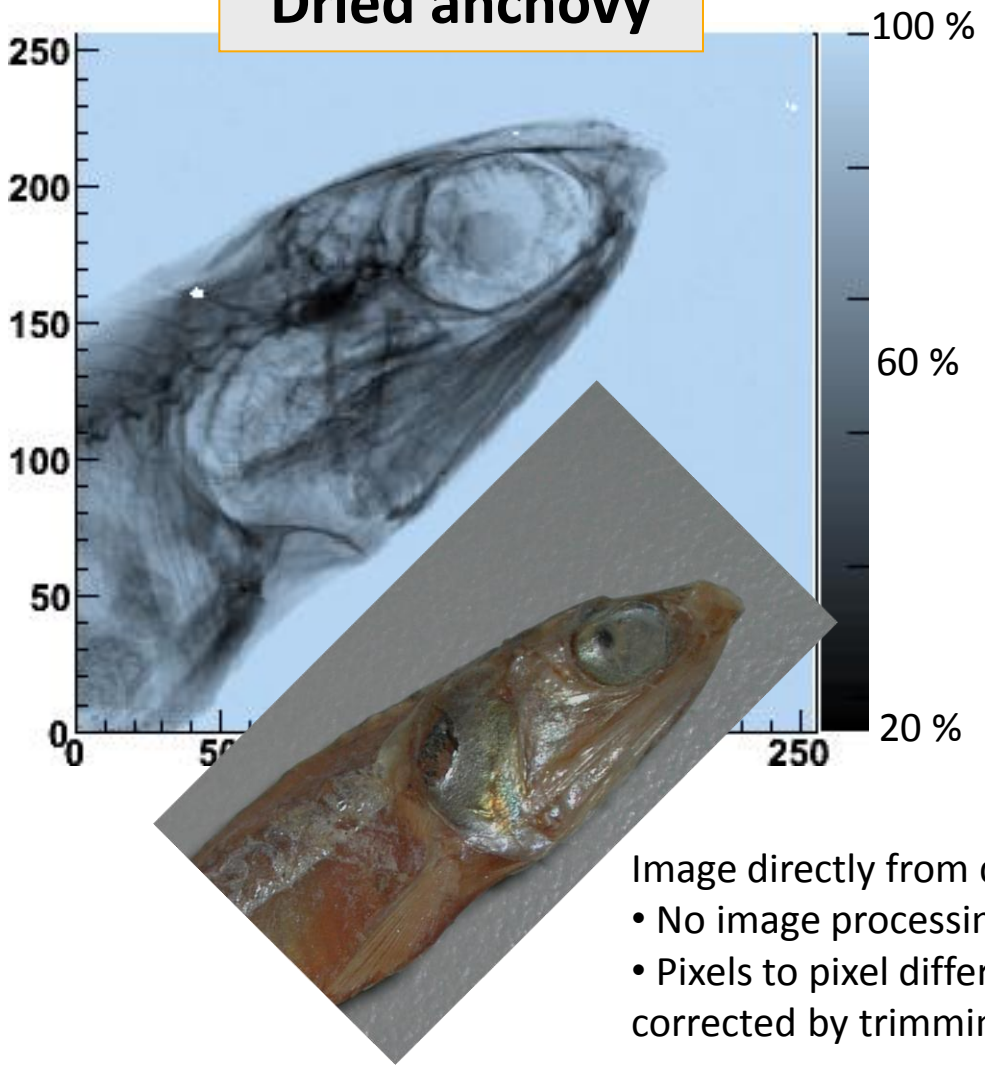
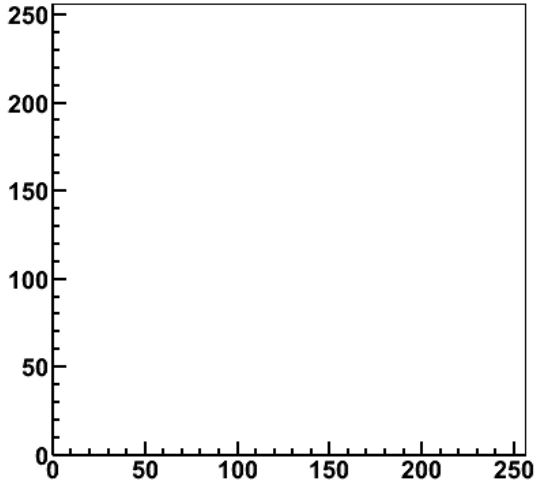


Image directly from detector
- No image processing
- Pixels to pixel differences corrected by trimming

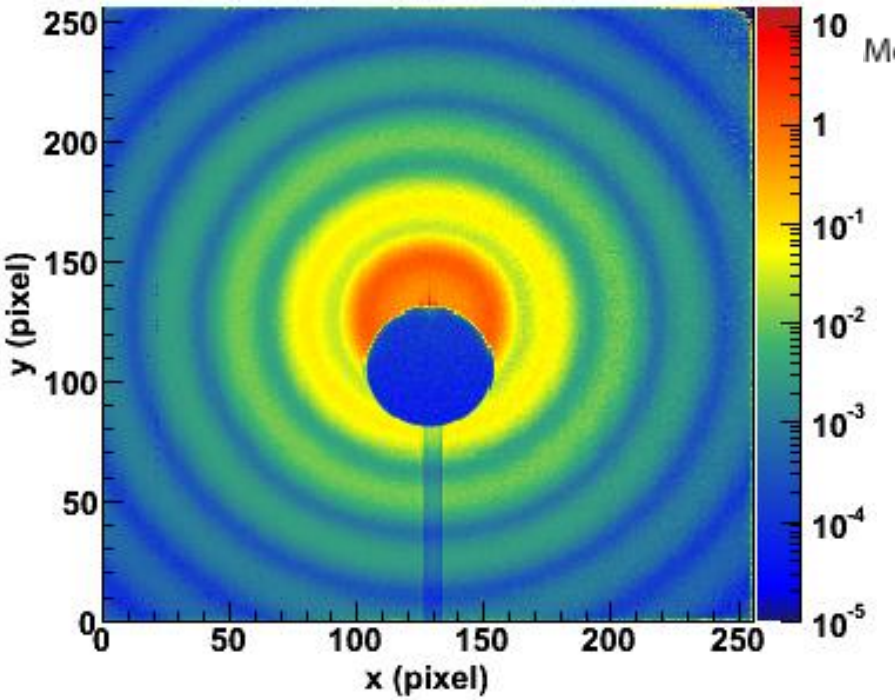
CPU fan

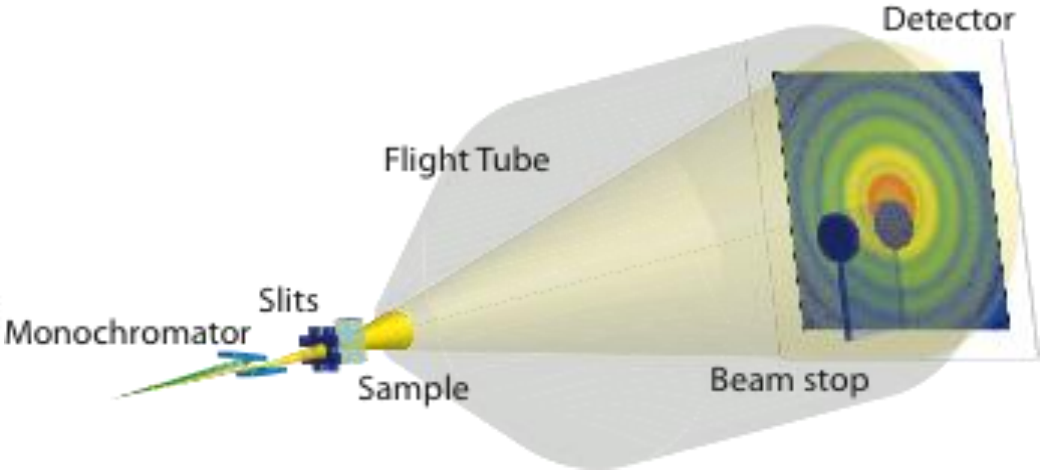


V = 50KV, I = 1 mA
Chip in 8 bit Mode
Exposure time 85µs
Dead time 3µs
Frame rate 11.4 kHz
Fan speed 100Hz

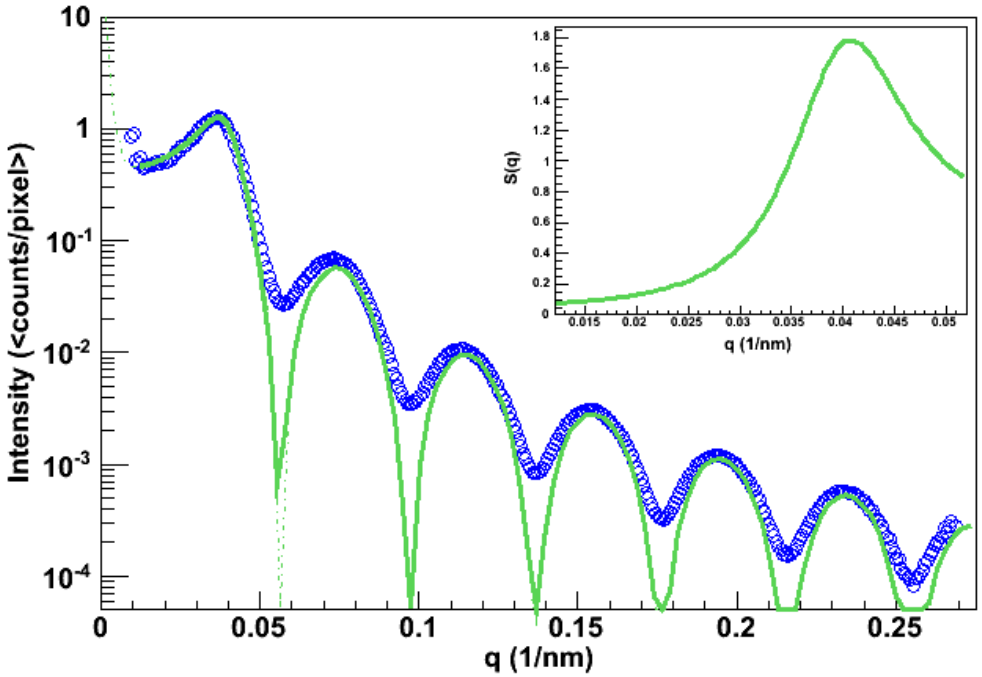
Investigating colloidal suspensions with Eiger

Average Diffraction Pattern
Thousands of 50 us exposures





Structure and Form factors



Analysis: Ian Johnson

Probing the dynamics, Photon Correlation Spectroscopy

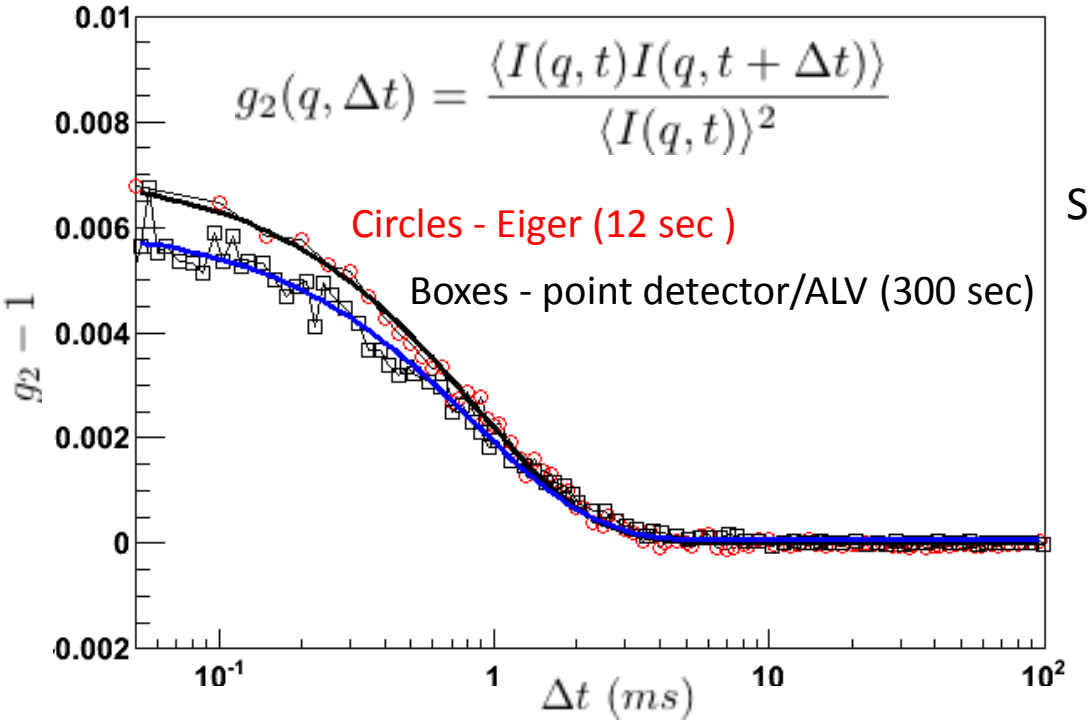
Eiger fast frame rate:

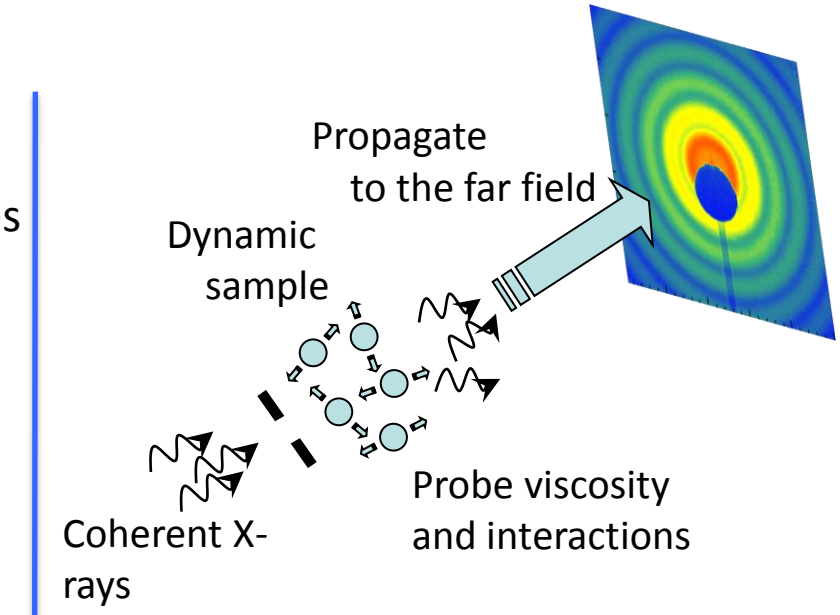
Second long exposure series @ 20 kHz

45 us exposure and 5 us dead time between frames

Intensity Fluctuations to probe the dynamics

Intensity-Intensity Auto Correlation Function





Siegert relation,

$$g_2(q,\Delta t) = 1 + \beta|g_1(q,\Delta t)|^2$$

Normalized field correlation function

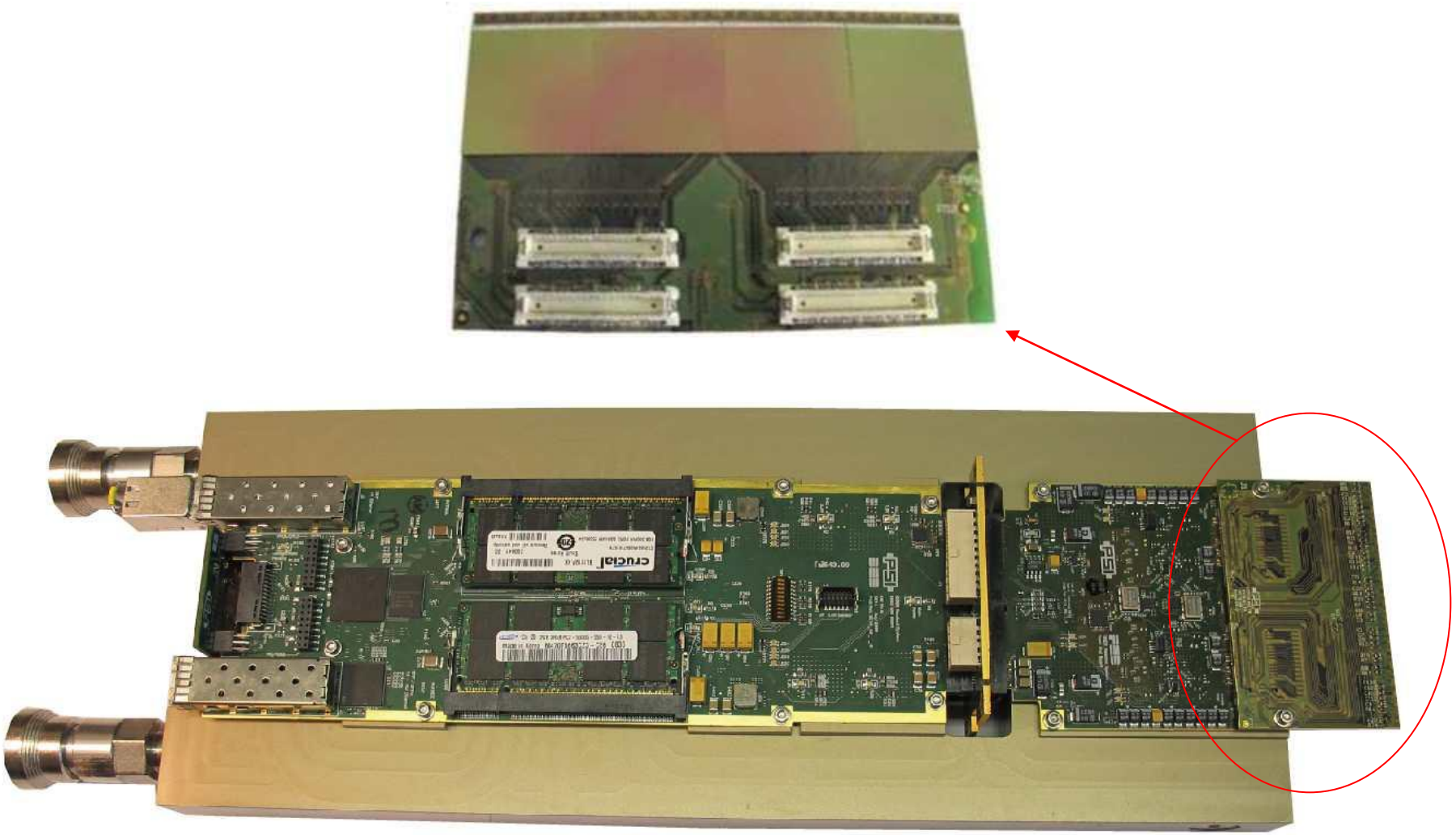
$$g_1(q,\Delta t) = e^{Dq^2\Delta t}$$

Brownian motion,

$$D = D_0 = \frac{kT}{6\pi\eta r}$$

Analysis: Ian Johnson

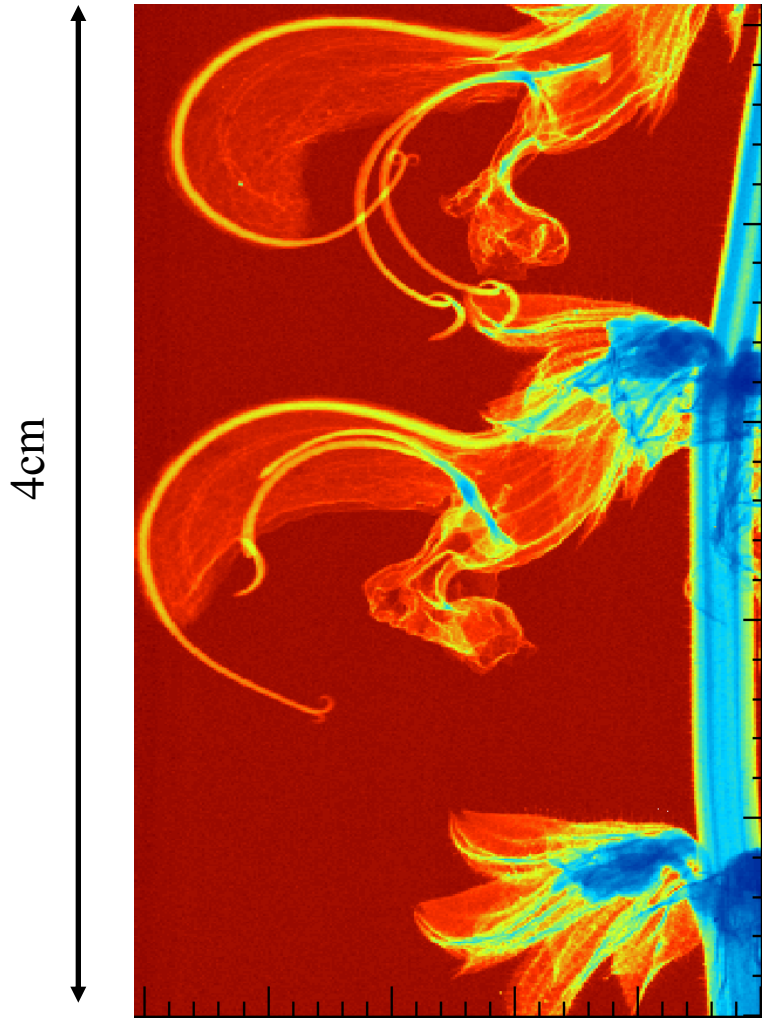
Half Module System



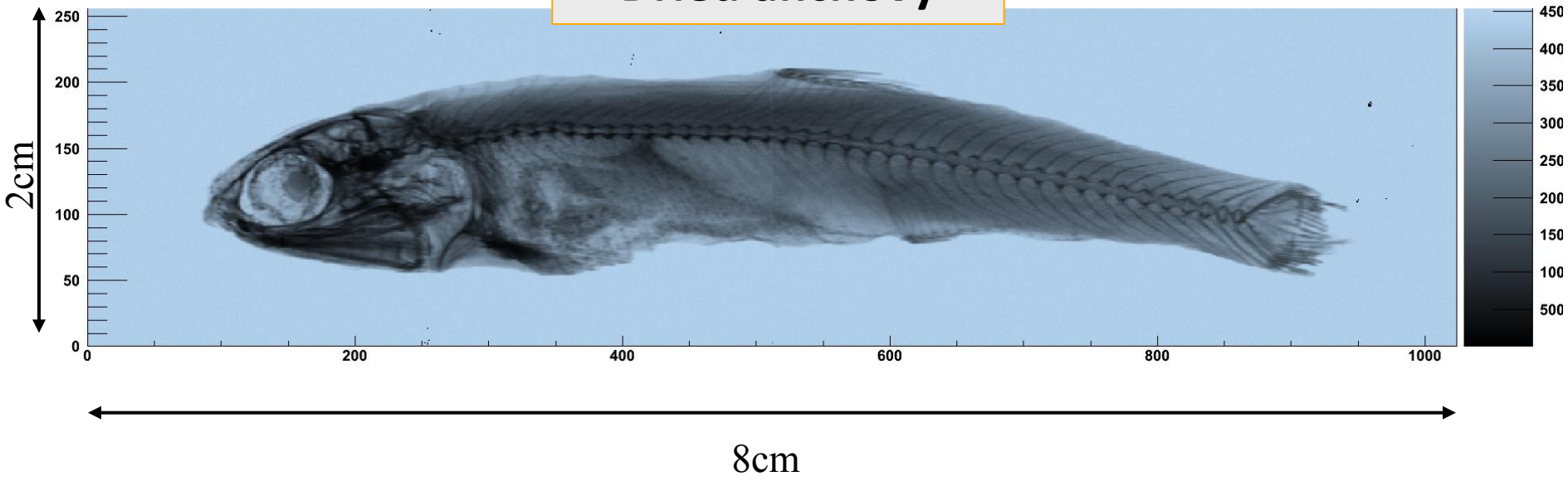
X-ray Images, two chips

Wild flower

No stitching, no trimming, with background correction



X-ray Images, half module

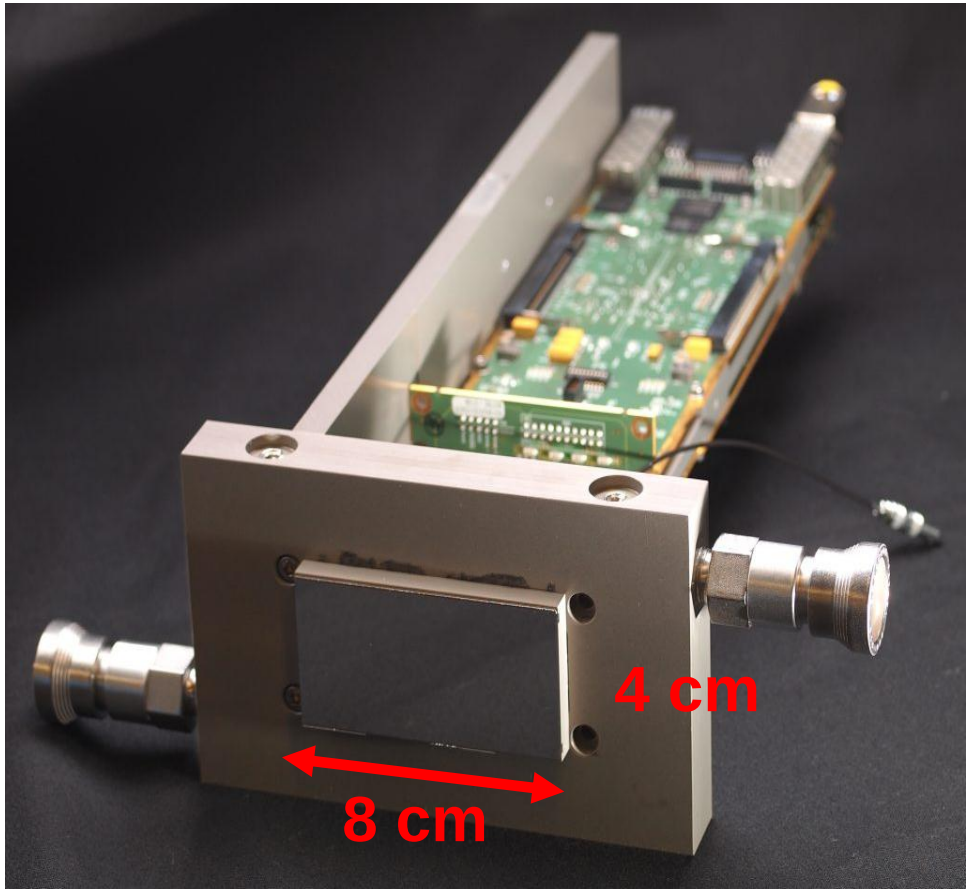


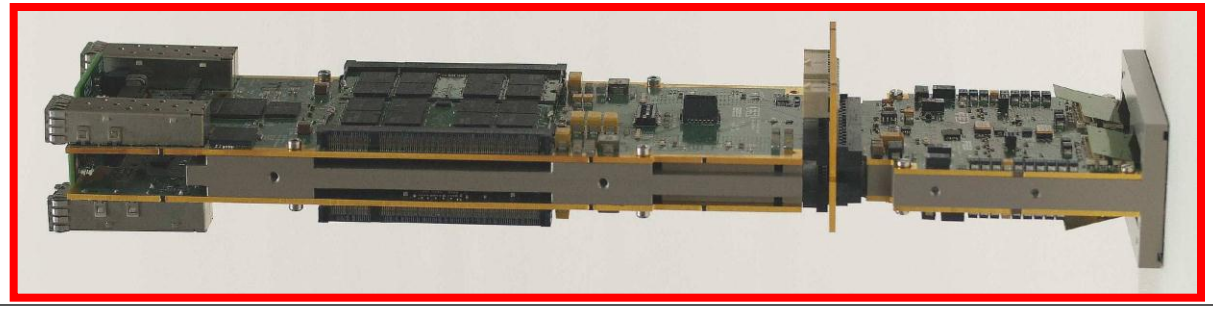
No stitching, no trimming, with background correction

Full module

500 k pixel Modules

- 38 X 77 mm^2 Sensitive area (Pilatus size)
- Parallel readout on half module base
- 8 GB on module data storage
- Front and Backend Boards
  - Boards have been produced and tested
  - Firmware and software is under development, almost ready
- Full Module High Density Interconnect
  - Flex PCB received and working
- Full module working!
- Bump bonding issues being addressed

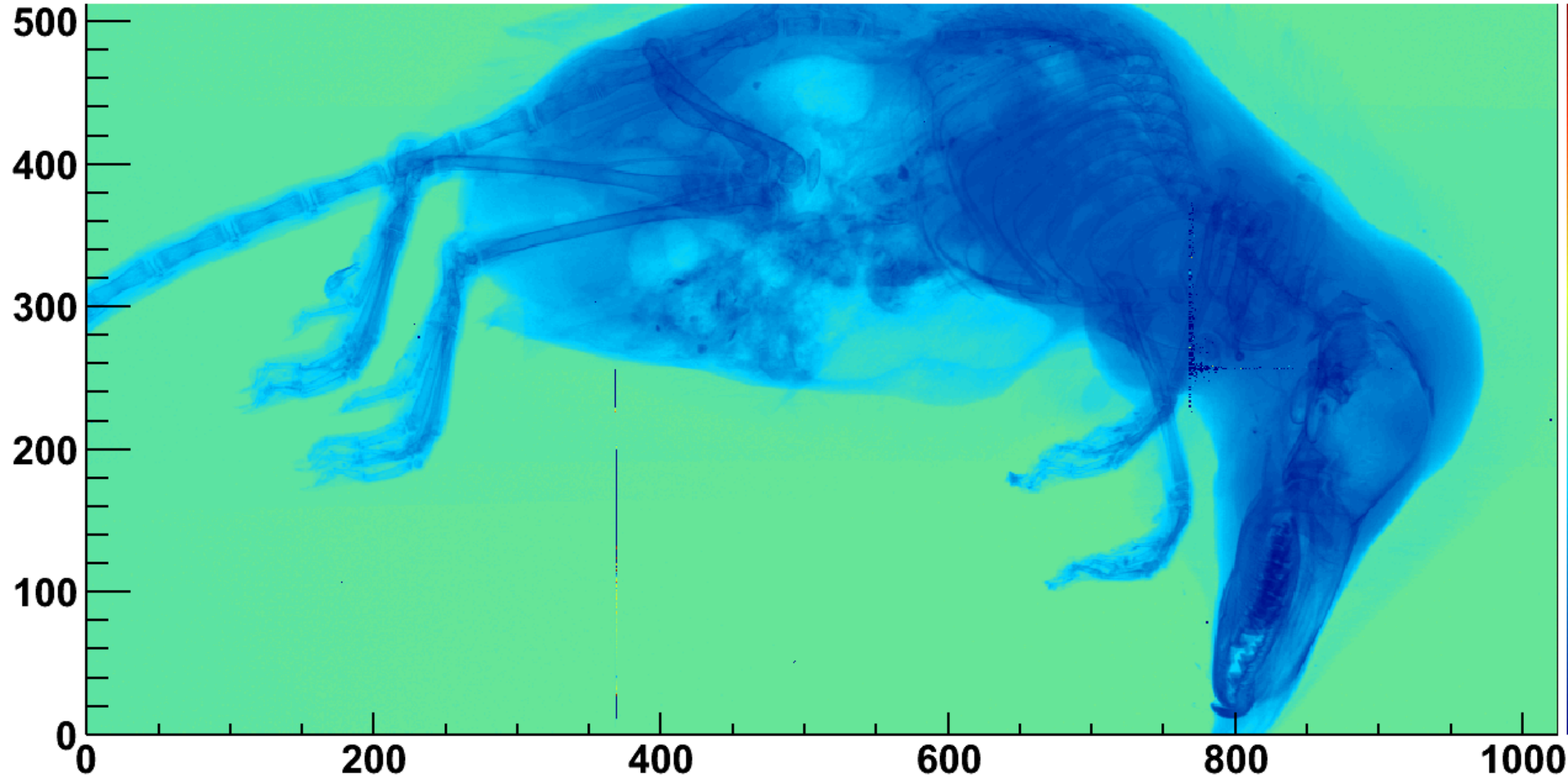




X-ray Images, full module

First working module after recovery from bump-bonding disaster.
No stitching, no trimming, no setup optimization, with background correction. New module.

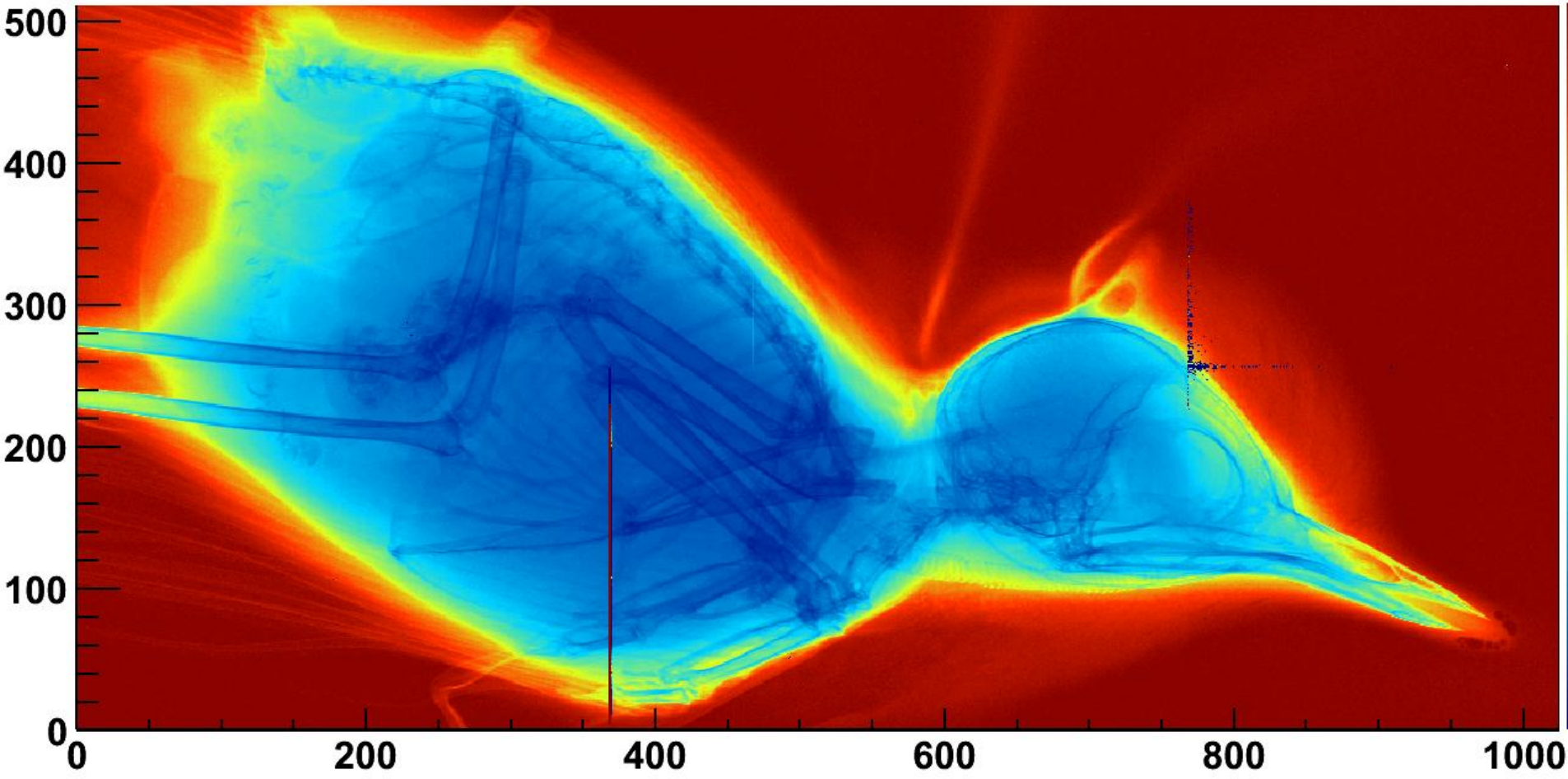
Shrew



X-ray Images, full module

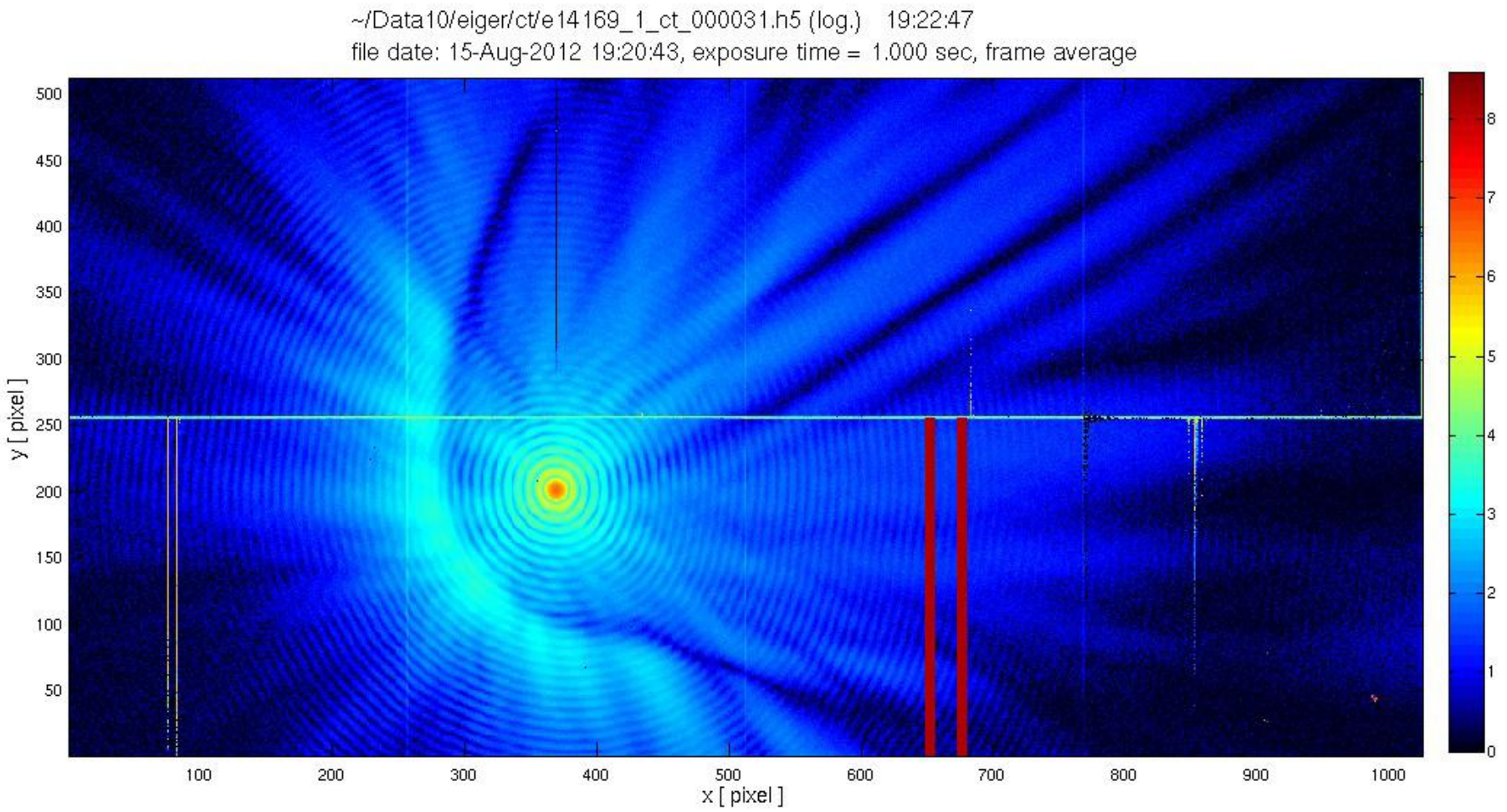
First working module after recovery from bump-bonding disaster.
No stitching, no trimming, no setup optimization, with background correction. New module.

Robin



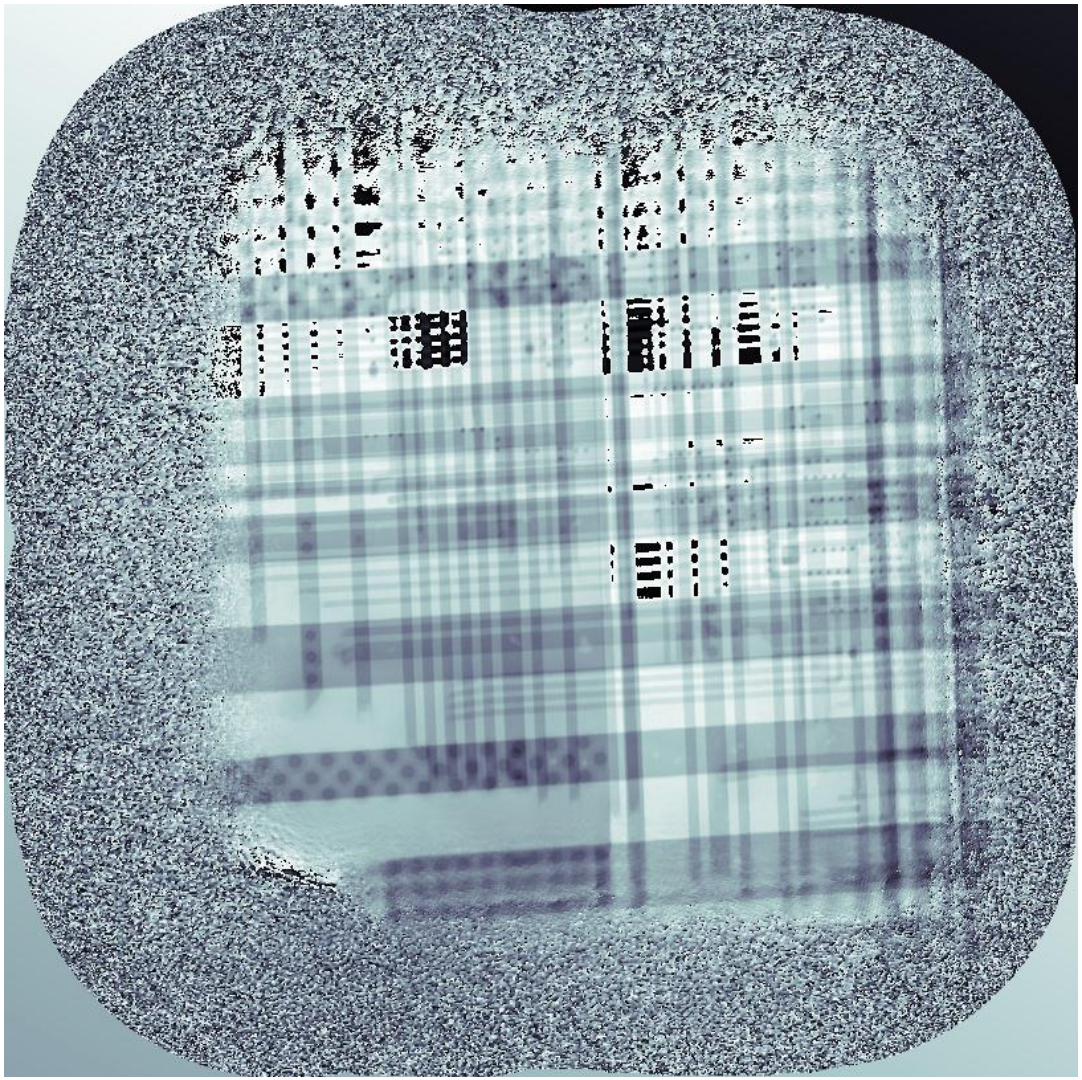
Full module: first CSAXS experiment

RAW DATA



Full module: first CSAXS experiment

Phase contrast image of a small area of a Pentium IV



Full module: first CSAXS experiment

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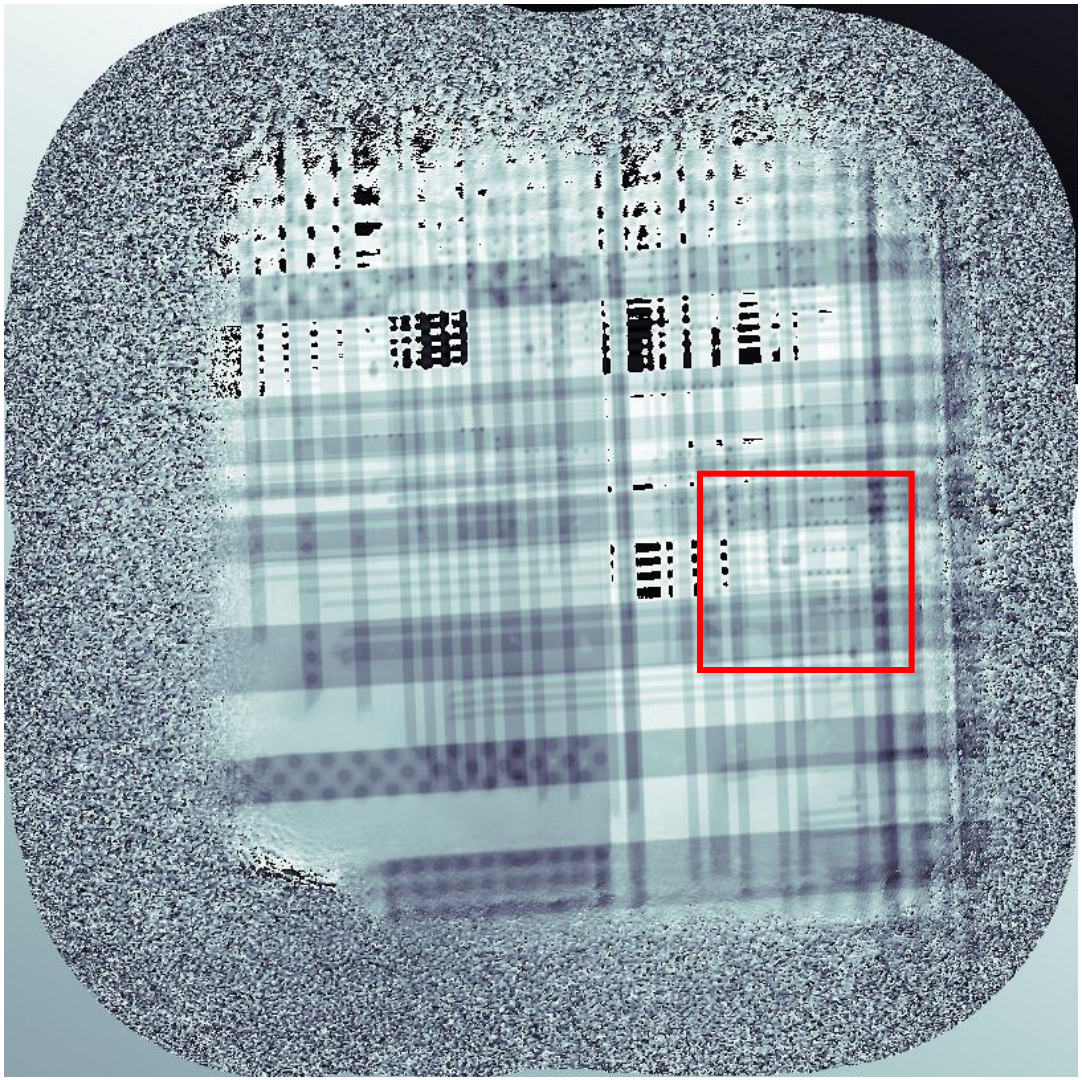
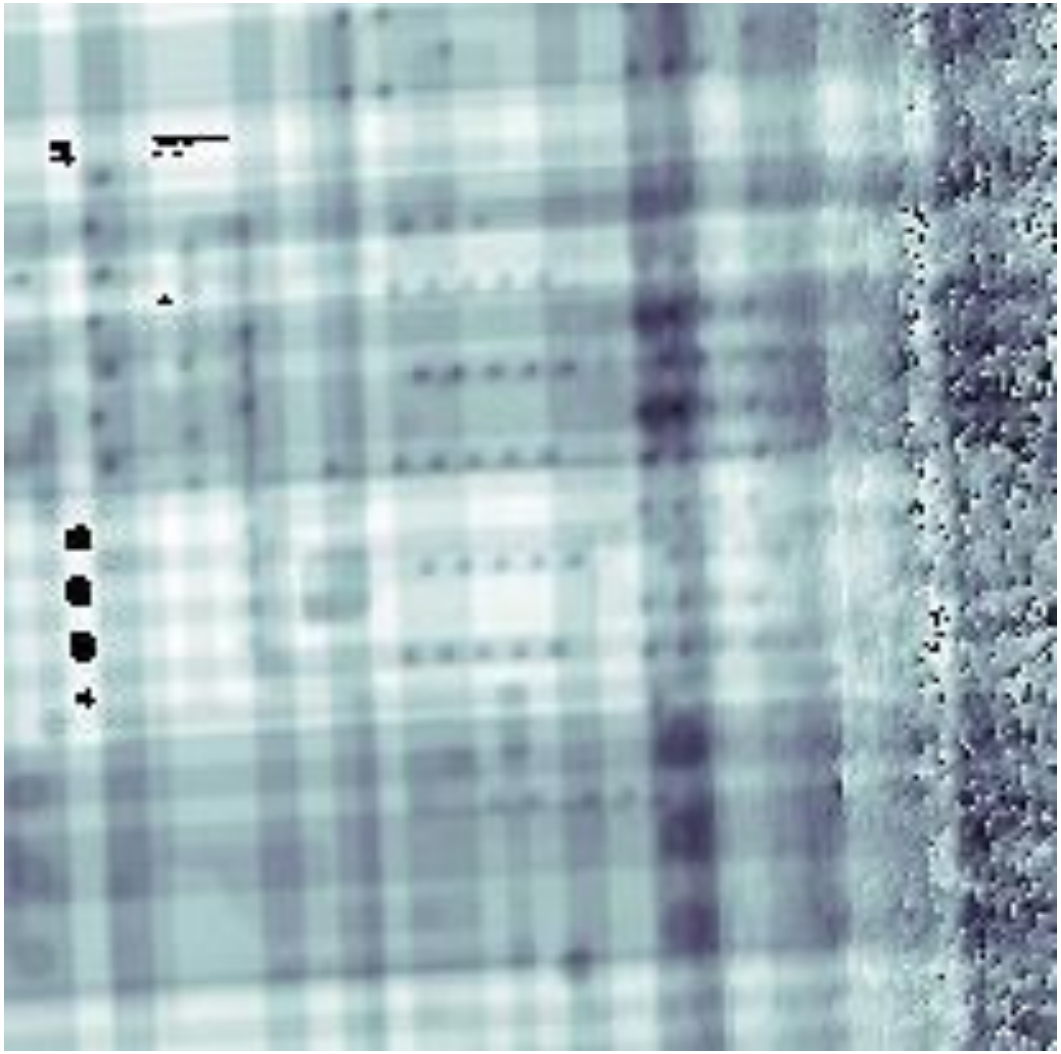
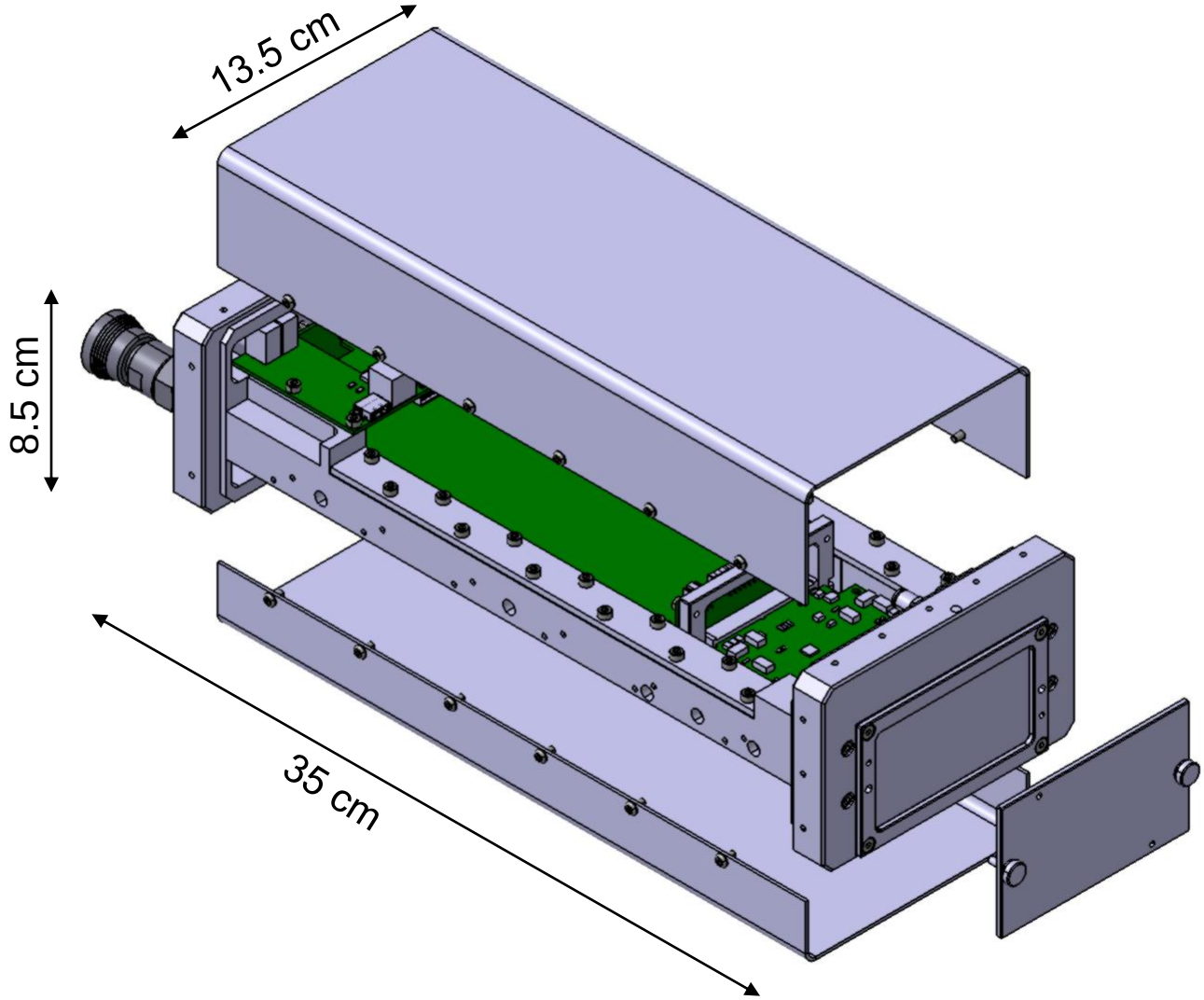


Full module: first CSAXS experiment

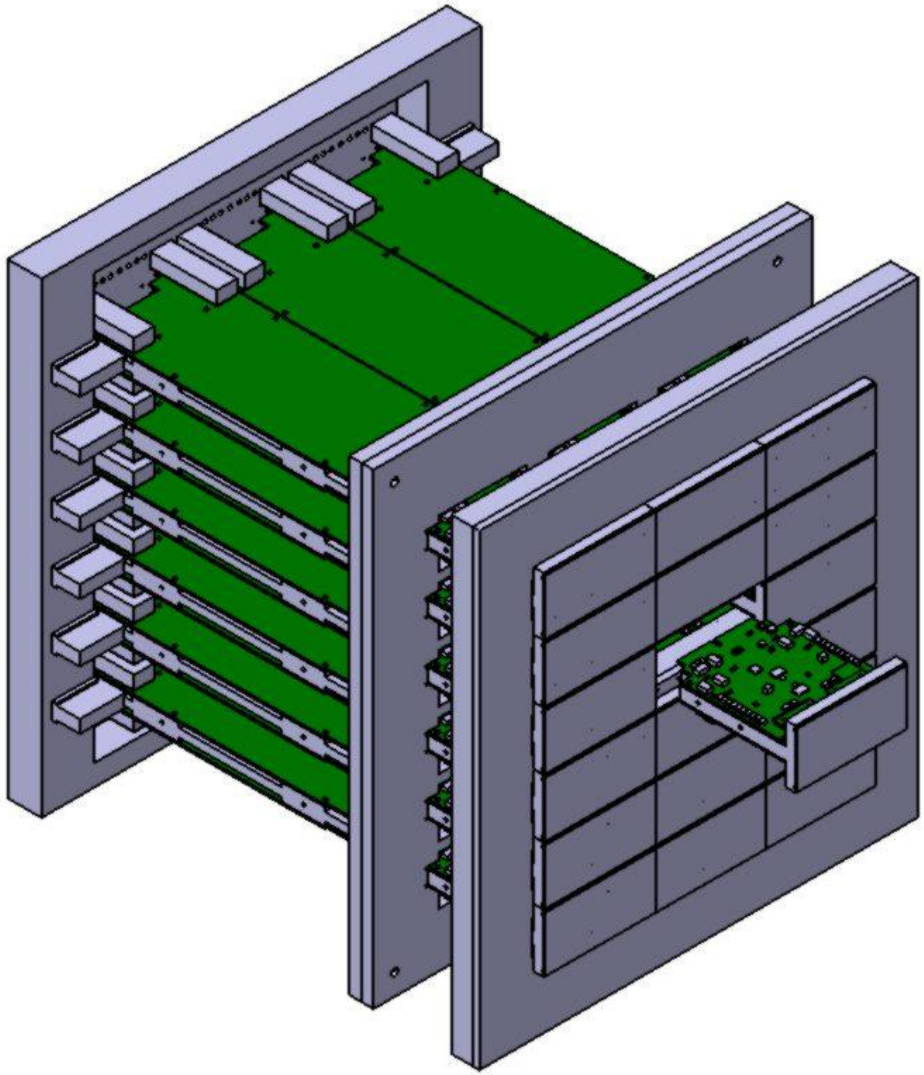
Phase contrast image of a small area of a Pentium IV



EIGER 500k



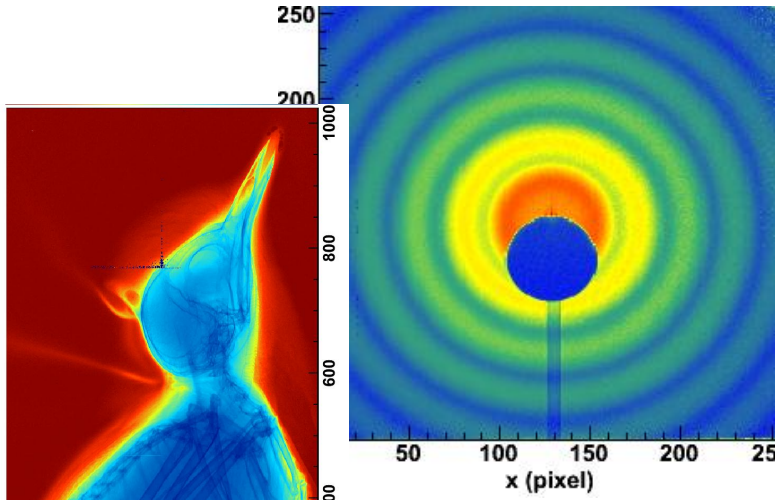
EIGER 9M, nine million pixel detector

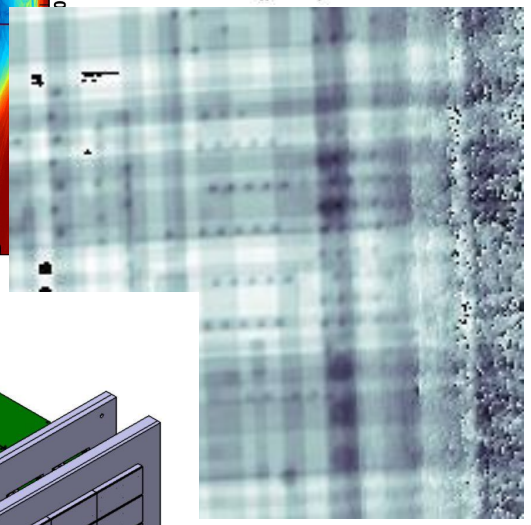


- Area: 23x23cm^2
- Number of pixels: 9 million
- Frame rate: up to 23 kHz
- Developed for SLS cSAXS beamline
- Total (raw) data rate: 900Gb/s

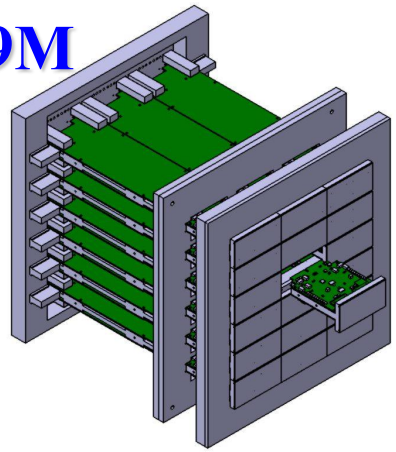
Conclusions

- We have a few Single chip test systems
  - High bump bond yield
  - The Eiger chip is operational
    - First x-ray images
    - Achieved a 22 kHz frame rate
  - First experiments
    - Time resolved
    - X-ray Photon Correlation Spectroscopy
- We are working towards modules
  - Front and Backend Boards
    - Boards have been produced and tested
    - Firmware and software almost ready
  - Half module system
    - Half module system is working
  - Full Module
    - Flex PCB (HDI) produced and working
    - First images taken with a prototype
    - First CSAXS experiment done
    - Bump bonding problems being addressed
- EIGER 9M prototype in early production phase





EIGER 9M



ACKNOWLEDGMENTS

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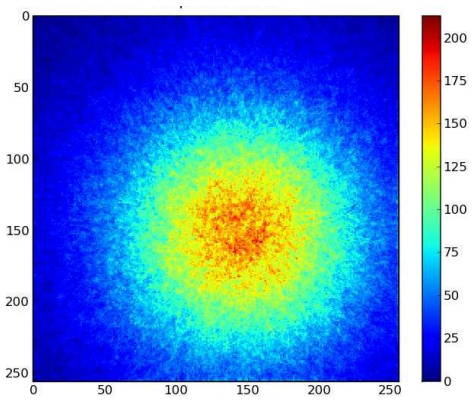
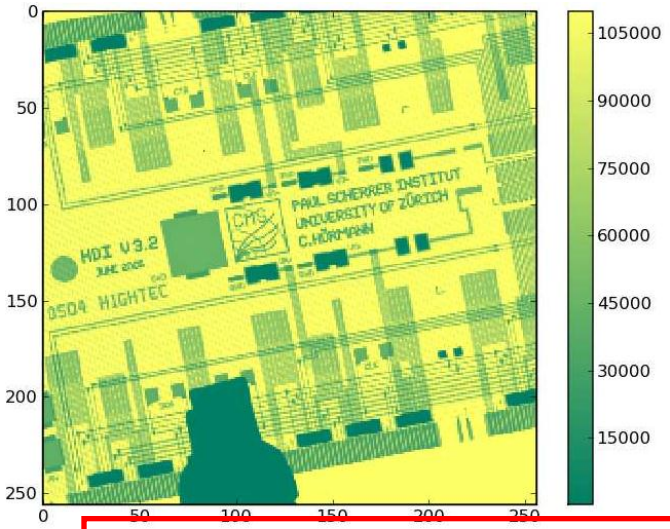
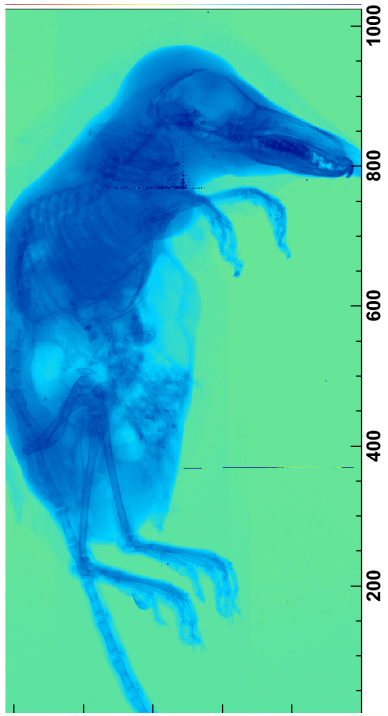
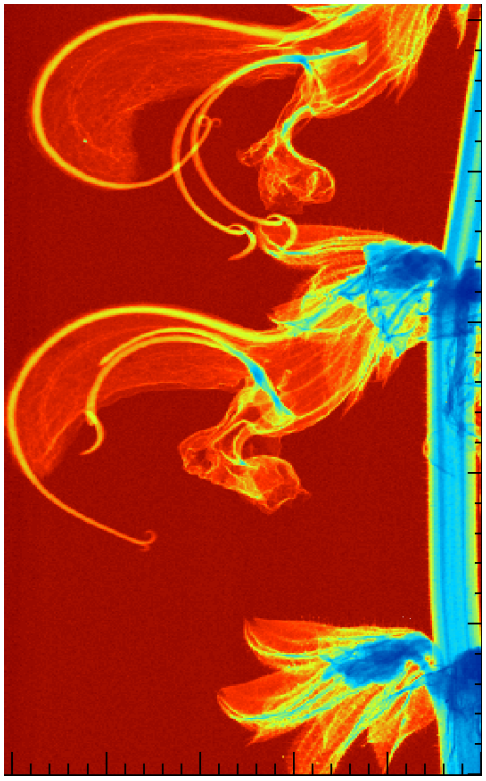
SLS Detector Group

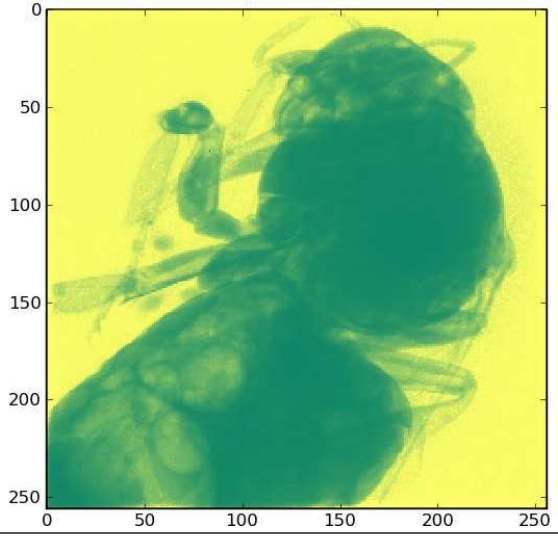


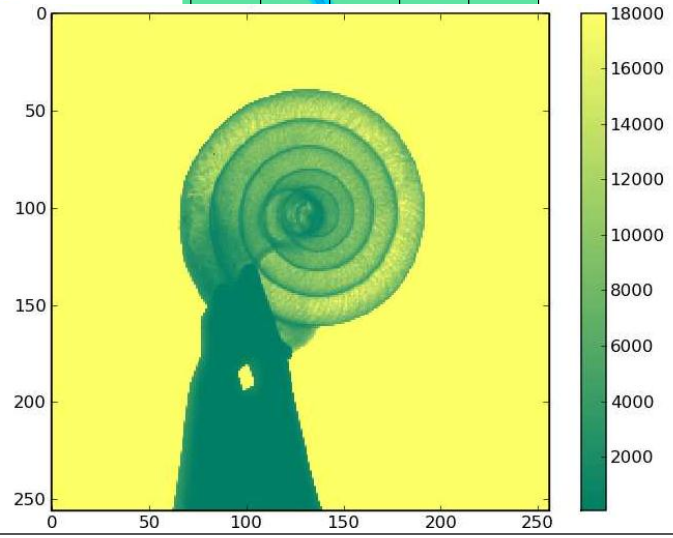

HDI V3.2
0504 HIGHTEC
PAUL SCHERRER INSTITUT
UNIVERSITY OF ZÜRICH
C.HÖRMANN



THANKS!







BACKUP SLIDES

EIGER main features (III)

- **Count rate: 1MHz/pixel (1.8 x 10^8 x-rays/mm^2/s)**

  Max. frame exposure time before overflow:

  - **T_{max} @ 4 bit mode = 16 µs**
  - **T_{max} @ 8 bit mode = 256 µs**
  - **T_{max} @ 12 bit mode = 4 ms**

- **100 MHz DDR readout (PII:100 MHz)**
  - **T_{ro} @ 4 bit mode = 40.96 µs**
  - **T_{ro} @ 8 bit mode = 81.92 µs**
  - **T_{ro} @ 12 bit mode = 122.9 µs**
  - **In continuous readout mode, max. frame rate=1/readout time;**
    12.5 KHz @ 8 bit mode

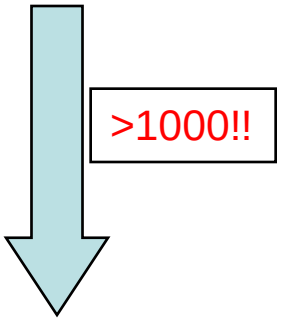
Pilatus II:

- **Same count rate**
- **T_{max} is about a second**

(but no continuous readout!)

Pilatus II:

- **100 MHz LVDS readout**
- **T_{ro} =1.2 ms**
- **BUT: Detector frame rate 5-10 Hz**



Requirements for an ideal detector

Both SAXS mapping & high resolution Coherent Scanning Microscopy need large (> 2 Mpixels), very fast and noise-less 2D detectors with a large dynamic range

- Single photon counting detector
- Modular detector system
- Parallel data transfer architecture

Smaller pixels will allow larger aperture and better statistical sampling
of coherent diffraction patterns (172 micron pixel are 'at the edge')

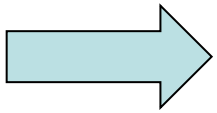
- Small pixel size
- No spatial distortion and uniform response

Scanning now usually done with a dead time of 50%

- Fast Frame Rate
- Simultaneous exposure and readout
- Negligible dead time

There is enough flux to go 10 to 100 times faster (depending on sample)

- High count rate of incoming photons

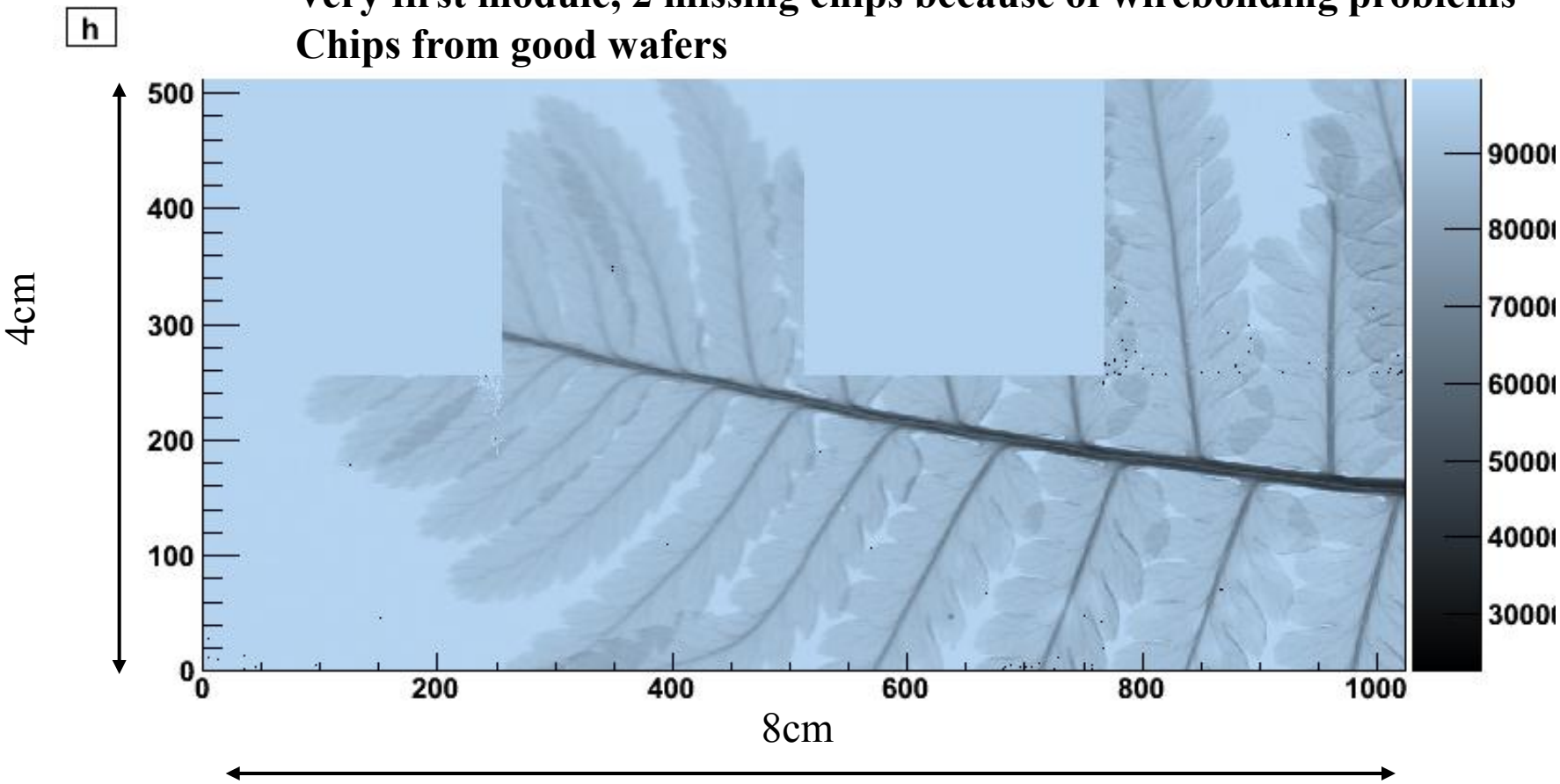


E I G E R

X-ray Images, full module

Fern leaf

No stitching, no trimming, no setup optimization, with background correction.
Very first module, 2 missing chips because of wirebonding problems
Chips from good wafers



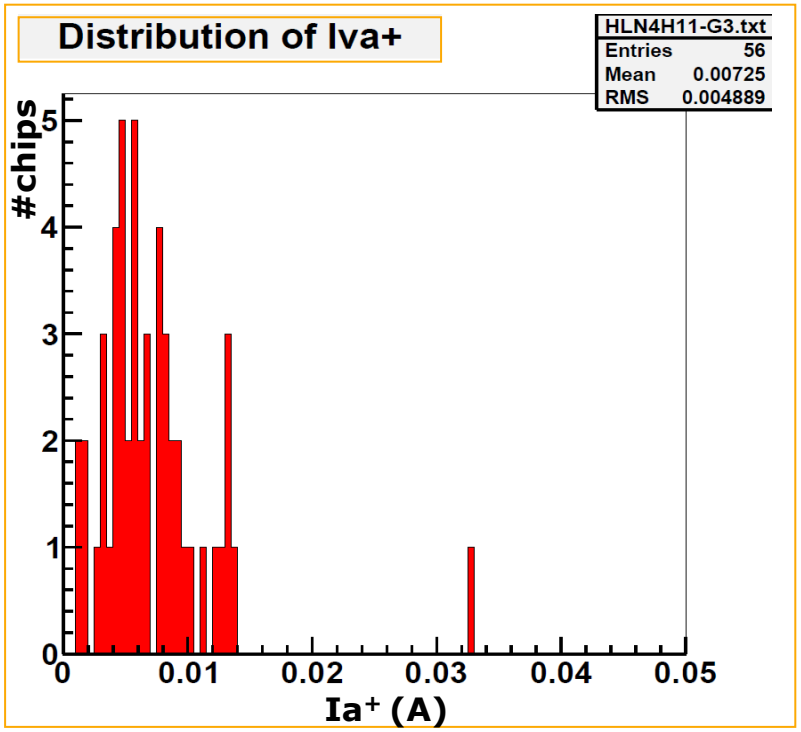
Further Considerations

- Distribution of Ia^+ for a nominal Va^+ settings (1.14V) measured on the chips in one wafer *(Wafer test setup)*

- For the chip under test:
  Ia^+~8mA; $Iash^+$~91mA
  Ia+/pixel ~122nA; Iash+/pixel~1.40µA

- Ia+ and $Iash^+$ are lower then expected →
  - from sim. nom. ~ 182m
    /pixel ~ 2.78µA

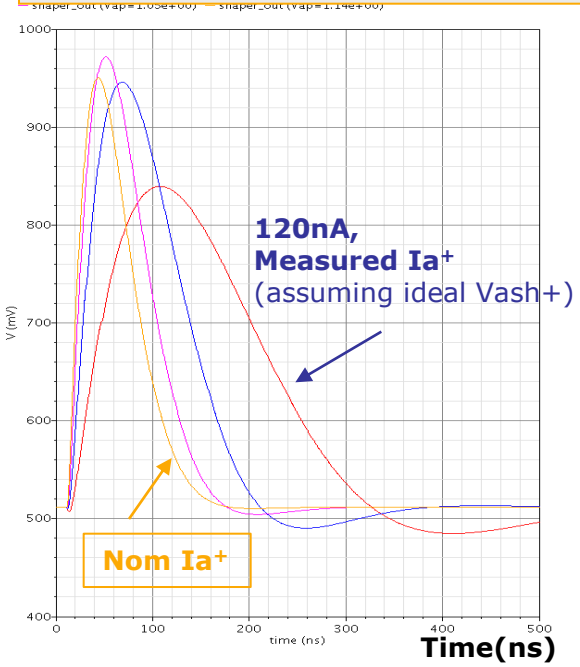
- Simulation: Lower analogue currents:
  - LOW power chip
  - BUT higher noise
  - Slower preamp.!

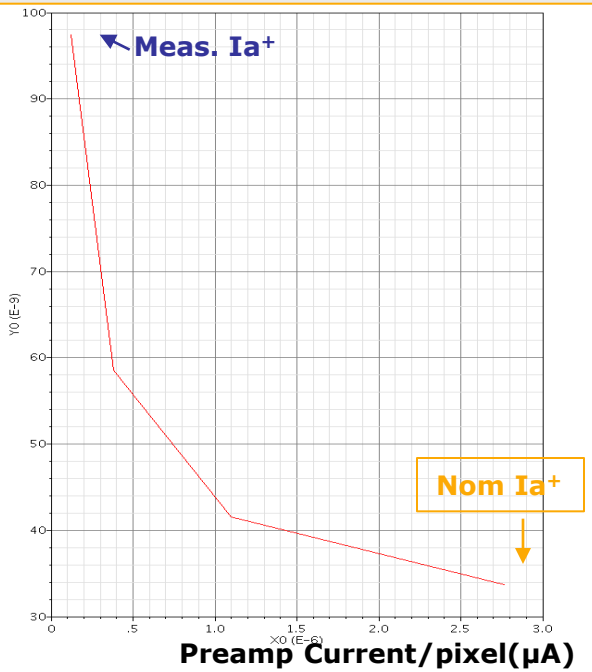


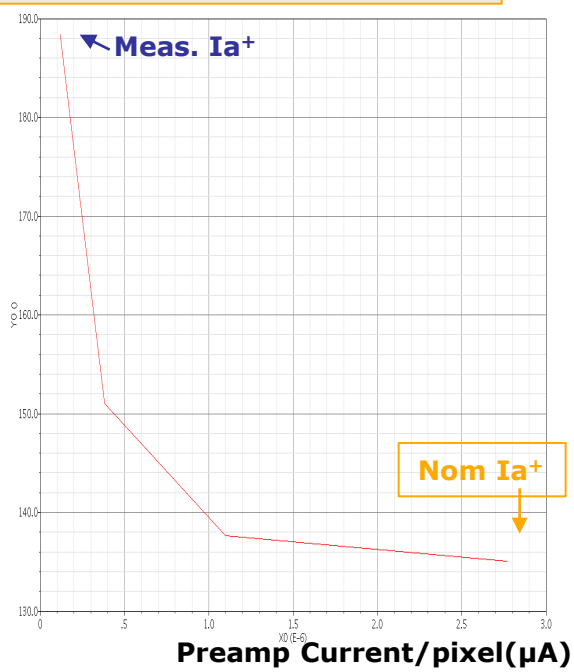
The present configuration can be defined as **"LOW POWER"** chip!

Low Ia current effect:

- **Shaper Oputput (mV)** **Peaking time (ns)** **Shaper output Noise (e-)**







Plan:

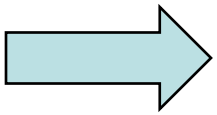
- ❑ studying the analog signal and optimize the preamp. and shaper working point
- ❑ redefine the 3 mode of op. with improved the chip performances

Pixel matrix static power consumption

EIGER: 2.8+1.4+1.4 uA *256*256 = 5.6 uA * 65536 = 0.367 A (=1.43 mA/col)
2.8*1.14+(1.4+1.4)*2 *256*256 = 8.8 uW *65536 = 0.576 W (=0.156 W/cm^2)

PII: 4.6+4.6+3.6 uA *60*97 = 12.8 uA * 5820 = 75.5 mA (=1.26 mA/col)
(4.6+4.6)*1.2 +3.6*2.5 *60*97= 20 uW * 5820 = 0.117 W (=0.068 W/cm^2)

Transistor count:
170 nGAA
196 pLIN
68 pGAA
=434 transistors/pixel
=28.44M transistors in the matrix.

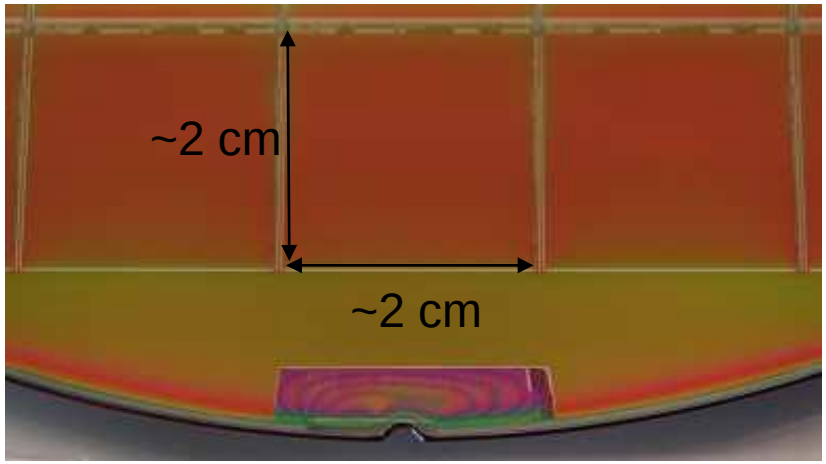


Transistor density:
~13um^2/transistor (with TWELL)
(~12um^2 in the digital section)

PII: 517 transistors/pixel
3M transistors in the matrix

PII: 57.2 um^2/transistor (without TWELL)
Actual transistor density improvement:
4.4x+TWELL

Short EIGER history



Design started: 02.2005
→Design supervision: almost none
→Software and system management support: almost none

Tape-out to EUROPRACTICE: 26.02.09

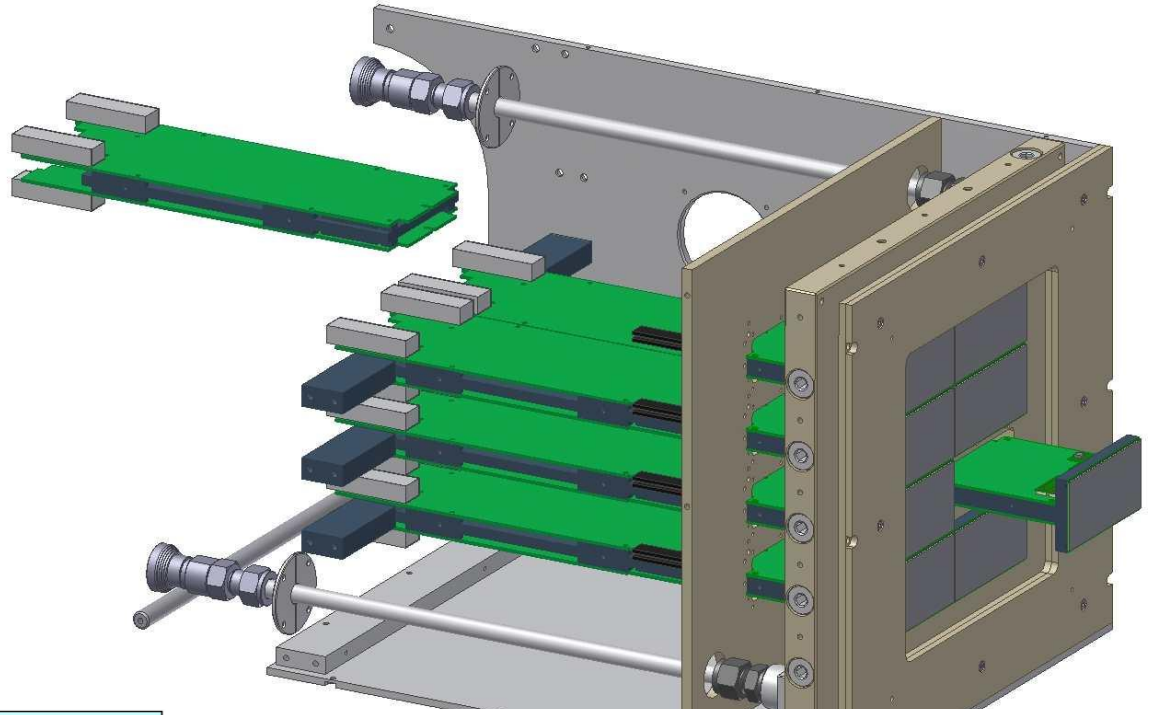
->>Almost all chip blocks are on silicon for the first time

- First wafer (with some parameters off-specs) received back from foundry: 03.06.09
- Testing started: 10.06.09, the chip is not "smoking"
- First image with a Strontium source: 24.08.09
- First "high quality" image: 02.09.09
- First time at a beamline: 11.09.09
- First maximum speed x-ray movie: 28.09.09
- First wafer map: 23.08.10
- First real experiment at a beamline: xx.xx.11
- First 2 chip image:17.05.11
- First half module image
- First full module image: 21.10.11
- First experiment at a beamline with a module: 15.08.12

First conference proceeding paper (ELBA '09):

"A new family of pixel detectors for high frame rate X-ray applications"
Nuclear Inst. and Methods in Physics Research, A
DOI information: 10.1016/j.nima.2009.10.043

EIGER 4M, four million pixel detector



Chip Specification		
Columns	256	per Chip
Rows	256	per Chip
Bits	8	per Pixel
Framerate	12 000	Hz

[1] 1 Gbit / s = 10^9 bit / s

[2] 1 MByte / s = 1024 * 1024 * 8 bit / s

	Detector Specification			Data Size		Data Rate	
	Modules	Chips	Pixel	Bit	Byte	Gbit / s [1]	MByte / s [2]
Chip		1	65 536	524 288	65 536	6.3	750
Half-Module	0.5	4	262 144	2 097 152	262 144	25.2	3 000
Module	1	8	524 288	4 194 304	524 288	50.3	6 000
4M Detector	8	64	4 194 304	33 554 432	4 194 304	402.7	48 000
9M Detector	18	144	9 437 184	75 497 472	9 437 184	906.0	108 000