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3D integration of Geiger-mode avalanche photodiodes for future linear colliders

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Geiger-mode avalanche photodiodes (GAPDs) offer excellent qualitites to meet the challenging requirements of the next generation of particle colliders. High sensitivity, fast timing response, virtually infinite gain and compatibility with standard CMOS technologies are some of the properties that make these devices so attractive. In fact, owing to to their extraordinary sensitivity and picosecond rise times, GAPDs enable single hit detection at each bunch crossing. In spite of all these advantages, GAPD detectors suffer from two main problems. First, they generate noise pulses that cannot be distinguished from radiation triggered events. As a consequence, the noise counts may lead to erroneous results and limit the range of detectable signals. Second, they present a low fill factor, which has a typical value around 40-50% and results in a low detection efficiency. Fortunately, the noise can be coped with advanced techniques, such as the gated operation or particle sampling at various layers. Nevertheless, it is difficult to increase the fill factor with standard technologies. In this contribution, the 3D vertical integration of a multilayer detector is proposed to overcome the fill factor limitation of standard GAPDs.

The reduced fill factor is basically due to two aspects related with the design of the pixel. On the one hand, to the readout electronics, which is monolithically integrated with the sensor to improve the dynamic response. The readout electronics usually consists of a simple inverter and a memory element. However, additional transistors are needed to perform the gated operation and also to control the outward data flow. In our case, the readout electronics is composed of a maximum of 10 transistors, which are still too many compared with a sensor area of 20μmx20μm. On the other hand, in a conventional CMOS process the photodiodes are implemented by means of a p+/n-well junction and surrounded by a p-well with a lower doping profile to prevent premature edge breakdown. In particular, for those technologies below the 0.25μm node where the shallow trench isolation (STI) is used to prevent the punchthrough and latch-up, it is necessary to increase this non-active ring to avoid a dramatic increase of the noise (up to 1MHz). As a result, the non-active area is quite large compared with the sensitive area.

This paper presents an analysis of the achievable fill factor by an array of GAPDs with the 130nm CMOS process by Tezzaron, which allows the vertical stacking of two tiers. Fill factors between 75% and 96% have been obtained considering different structures with and without interconnection between tiers. Moreover, different sensor areas have been used to maximize the overlap between the non-active area from one tier and the sensor area of the other one. A chip containing several arrays of GAPDs with different alternatives has been designed with the 130nm Tezzaron process.

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