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Development of Monolithic Active Pixel Sensors in 65 nm CMOS Technology

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This work presents the design and characterization of a CMOS monolithic active pixel sensor manufactured in a commercial 65 nm process. The sensor is our first prototype in this technology for next generation, ultra-high resolution and radiation-hard direct detectors for electron and X-ray imaging, and follows previous developments in 0.35 μm and 0.18 μm CMOS processes. The chip features square pixels of 2.5 μm pitch arrayed on a 400x400 pixel matrix, and subdivided in four sections implementing different pixel designs, all based on the same 3-transistor (3T) architecture but varying in diode and transistor layout. The sensor has been extensively characterized in the laboratory in order to determine its charge-to-voltage conversion gain, noise and leakage current performance. Electron detection tests have been performed on an FEI TITAN electron microscope at the LBNL National Center for Electron Microscopy (NCEM), including irradiation with 300 keV electrons to doses up to 200 Mrad. The presentation will review the results from this characterization and discuss their interpretation as a function of the various pixel design features. The impact of effects such as gate leakage, encountered in this technology but not observed in previous sensors manufactured in coarser feature size processes, will also be discussed.

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