A study on the dynamic range of integrating SOI chips

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ABSTRACT

A SOI chip has been designed and tested to study the feasibility of using I/O transistors so as to improve the dynamic range of integrating circuit. The design is based on a successful chip named INTPIX4, and test results show that an improvement of 50% can be achieved this way. This gives people one more option about how to improve the dynamic range of integrating pixel. However, systematic study has not been finished yet, which is foreseen in the near future.

Motivation and Methods

In the design of INTPIX4, two stages of source follower were used in each pixel, integrating, sampling and reading out the signal charge (as shown in Fig. 1, the pixel circuit). Obviously, the dynamic range of signal charge that can be handled by this circuit is primarily dominated by the power supply. Subtracting the power supply by the transistor threshold, the dynamic range is basically determined, while the load current has certain influence on it as well.

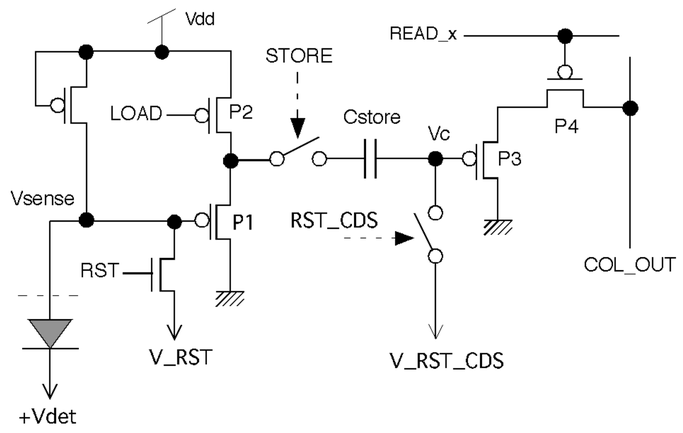

Figure 1. The Pixel Circuit of INTPIX4

In the 0.2 μm SOI detector process developed by KEK and LAPIS Corp., 1.8V core transistors and 2.5V I/O transistors are provided. In previous versions of INTPIX chips, 2.5V transistors were used in I/O buffer only. With a source follower powered by 1.8V, one can get about 1.2V dynamic range due to a threshold of 0.6V.

Despite a slightly higher threshold of 0.7V, I/O transistors are still an appealing choice in terms of dynamic range.

In order to verify the preceding idea, a small chip was designed and submitted to SOI MPW run in 2011. **This chip took the successful INTPIX4 as a starting point, and made modifications as follow.**

. In each pixel, 2.5V transistors simply take the place of 1.8V transistors;
. Column buffer is replaced by a 2.5V source follower;
. An existing I/O buffer is used as the final buffer, but the power supply is decreased from 3.3V to 2.5V;
. A bunch of 1.8V-to-2.5V converters are used as interface between digital and analog, because all digital circuits remain in 1.8V domain.

As a result, power rails are set to 2.5V/ground and 1.8V/ground.

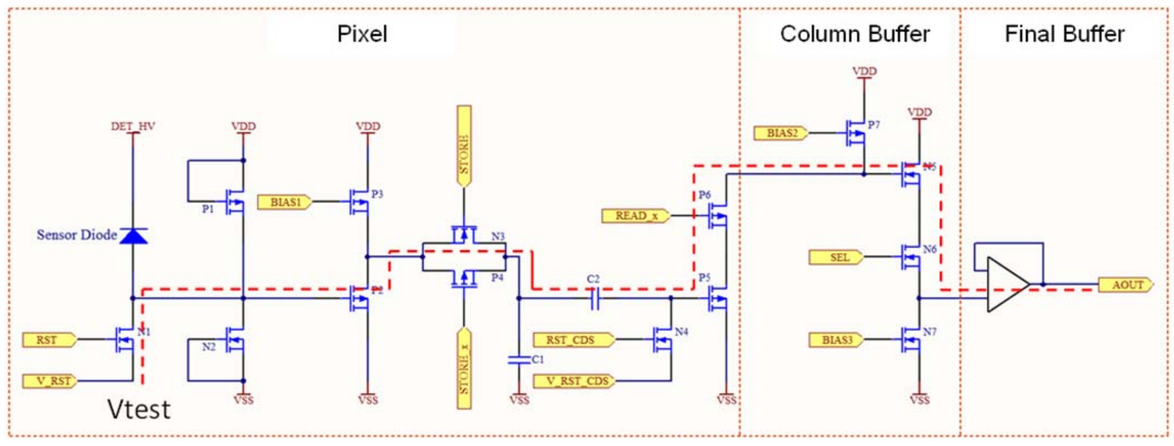

Figure 2. Signal path of the chip

Trade off between dynamic range, layout area, speed, and power consumption:

. Decreased load current in pixel, to squeeze all transistors into the same area; (speed VS layout area)
. Decreased load current in column buffer(SF), to guarantee enough dynamic range; (Dynamic range VS speed)
. Increased load current in final buffer, to improve speed. (Speed VS power)

Measurements

The waveform of analog output was measured using an oscilloscope (as shown in Fig. 3):

. Rinsing edge about 30 ns;
. Falling edge about 40 ns.
. Consistent with the simulation results.

The voltage steps close to 0.8V were produced by a row of edge pixels, which are not enclosed by the guardring as tight as other pixels do. These pixels collects the leakage current from a larger area.

120 ns/pixel was used in the following measurement, but surely 80 ns/pixel is also quite safe.

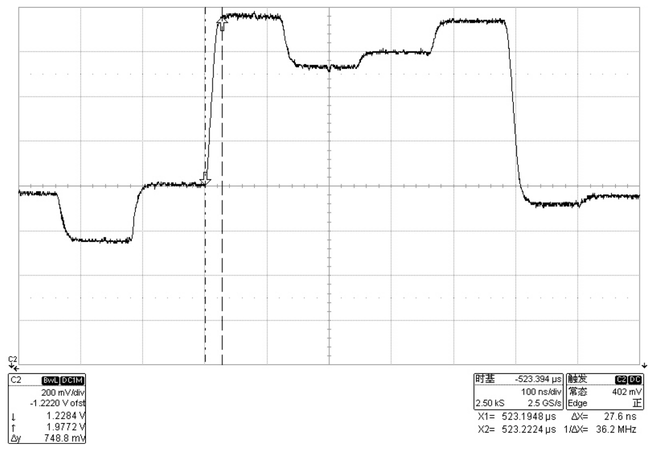

Figure 3. Waveform of the analog output

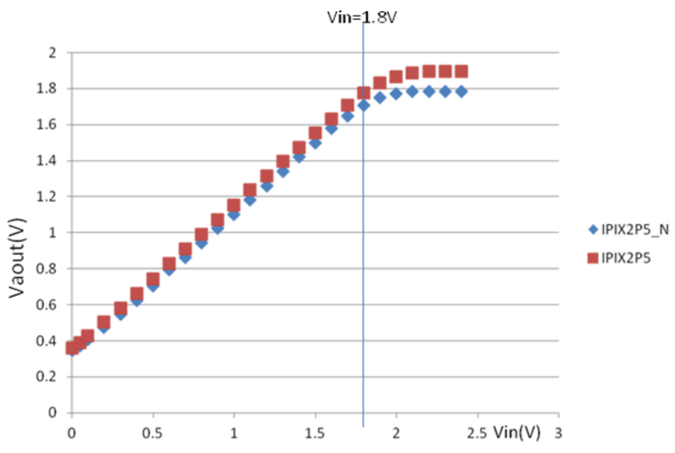

Figure 4. Circuit Test on Two Chips

A series of test voltage steps were injected into all the pixels through the external port V_rst . The signal path is indicated by the red line in Fig. 2.

Two chips measured (Fig. 4):

. One chip with slightly thinner gate oxide. (IPIX2P5)
. One normal chip. (IPIX2P5_N)

Dynamic range:

. **0-1.8V for IPIX2P5_N;**
. **0-1.9V for IPIX2P5.**

Gain:

. 0.777 for IPIX2P5_N;
. 0.801 for IPIX2P5.

In fig. 5, the same chip IPIX2P5_N was measured with 2.5V and 2.3V powering.

Decreasing of the power voltage has a significant influence on the chip in terms of the dynamic range. This can be understood as PMOS source follower turns to saturation when its input gets close to the power supply.

Special attention should be paid to the distribution network of power supply.

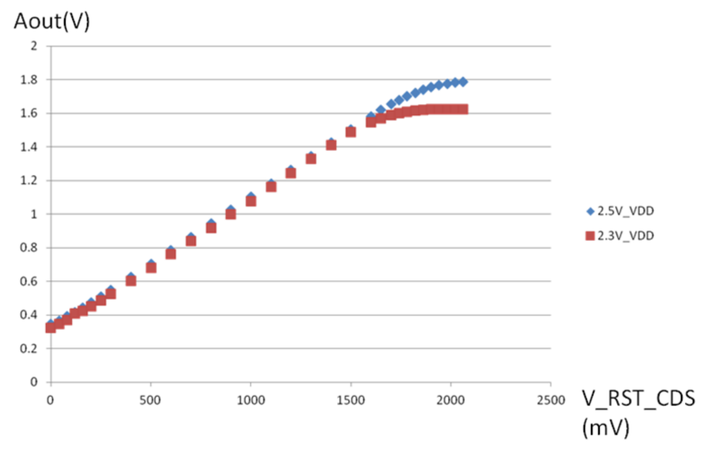

Figure 5. Circuit Test with different power conditions

Discussion

Conclusions:

. A larger dynamic range can be achieved by using 2.5V I/O transistors;
. The readout speed is able to reach 100 ns/pixel;
. The power variation affects dynamic range obviously.

The possible costs:

. Larger layout size;
. More complicated power scheme and/or additional voltage converters;
. Redesign of existing cells.

More to look at in the future:

. Uniformity over a whole chip;
. The chip performance under different temperature;
. Statistical test on a batch of chips.

The chip was designed as a monolithic detector chip. Fig. 6 shows a red laser image taken by the chip. The dynamic range as a detector involves more factors, such as noise, leakage current, diode capacitance etc.. Those need further study also.

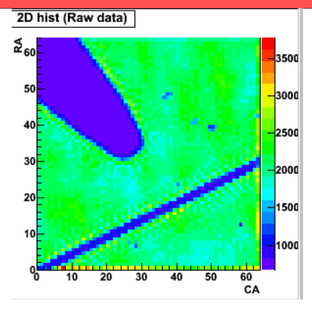

Figure 6. Red laser image of a pin head and a 30 μm wire