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A study on the dynamic range of integrating SOI chips

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In the SOI process developed by KEK and LAPIS, transistors can be divided into two groups by their nominal power supply, 1.8V and 2.5V respectively. All the past integrating SOI chips use 1.8V transistors in core circuit and 2.5V in IO buffers. To verify the idea of increasing dynamic range of integrating charge, a chip using 2.5V transistors in core circuit was submitted to MPW run in 2011. The test results show that an increasement of 50% of dynamic range can be achieved by this way.

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