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New fabrication and packaging technologies for CMOS pixel sensors: closing gap between hybrid and monolithic approach

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Monolithic CMOS Pixels (MAPS) integrate on the same silicon substrate the radiation sensor element with the processing electronics. Their fabrication is possible through an easy access to commercial high-volume foundries, resulting in low costs and high yield. However in the standard implementation these devices suffer from two major limitations. First, only NMOS transistors are allowed on top of the active area. Second, even high-resistivity substrate cannot be fully depleted because of voltage limitation of CMOS transistors.
In order to overcome both limitations, we propose new CMOS fabrication procedures recently available for low-volume users. The first one (TowerJazz CIS) is a 180 nm process with high-resistivity epitaxial layer and quadruple well option. Two additional deep wells (implants) isolate electrically the substrate from standard shallow wells and allow for both types of transistors to be implemented. The second process (ESPROS Photonics Corporation) is a 150 nm CMOS on bulk high resistivity (detector quality) substrate, insulated from transistor level by deep implant (junction). Following front-end processing, wafers are back-thinned to 50 microns; back-contact is implemented and activated at low temperature. This is part of standard ESPROS foundry procedure, no post-processing is required. Resulting structure allows not only for both types of transistors on top of the sensing area but also for full depletion (or even over depletion) of entire detector thickness. Results of charge collection efficiency and irradiation study of sensors from both manufacturers are presented.
Total thickness of monolithic CMOS sensors can be very small: typically 15 μm for active silicon and 5 μm for interconnections (several metal-insulator layers). Therefor MAPS can be thinned down to less than 30 μm, without loosing their tracking performance. This allows very small material budget and construction of non-planar (cylindrical) detector layers: thin silicon is quite flexible. In order to demonstrate feasibility of large area, ultra-light (< 0.1% radiation length) sensor ladders we develop novel packaging method. Thinned sensors (<50 microns) are embedded in polymer (kapton) film, electrical connection to pads are implemented by metal deposition and metal lithography (no wire bonding). The process is based on slightly modified process (existing at CERN) for flexible multi-layer PCB fabrication, in which aluminum is used for all metal interconnections. We present details of ladder design adapted for large area, followed by minimum ionizing particle tracking tests results.
Microelectronics industry is evolving rapidly: several other foundries propose deep submicron advanced CMOS process on high resistivity bulk material. Wafer back thinning and back-contact implementation as post-processing start to be also easily available on a cost-effective way. We believe that in near future this approach will reduce hybrid pixel technology approach to the cases where the use of non-silicon detector material (like diamond or cadmium telluride) is really mandatory.

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