Experience with 3D integration technologies in the framework of the ATLAS pixel upgrade for the HL-LHC

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Introduction

- 3D integration technologies can be used in HEP to build hybrid pixel detectors for application in high luminosity experiments featuring low mass, increased functionality, high density

- For the upgrade of the ATLAS pixel detector at the HL-LHC, R&D is ongoing on different 3D projects

- IC design in 3D, i.e. 3D electronics
  - Exploit full potential of 3D integration for innermost pixel layers
  - Tezzaron/Chartered 3D process (Bonn/CPPM/LBNL)

- Post processing 3D technologies: bonding, thinning, Through Silicon Via (TSV)
  - Develop compact module concepts for outermost pixel layers
  - Fine pitch bump bonding with thin chips (Bonn, IZM), post processing TSV (Bonn, IZM), Solid Liquid Inter-Diffusion (SLID) bonding (MPI/HLL Munich, EMFT)

A. Macchiolo, Thin n-in-p pixel sensors and the SLID-ICV vertical integration technology for the ATLAS upgrade at HL-LHC, Friday, 9:50 AM – 10:10

universitätbonn

3D electronics

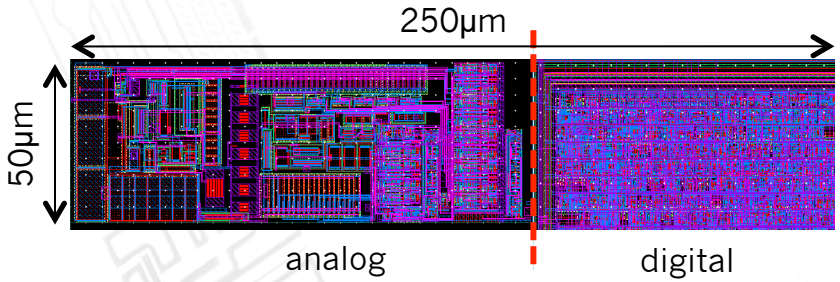
SI LAB Silizium Labor Bonn

3D electronics for inner pixel layers

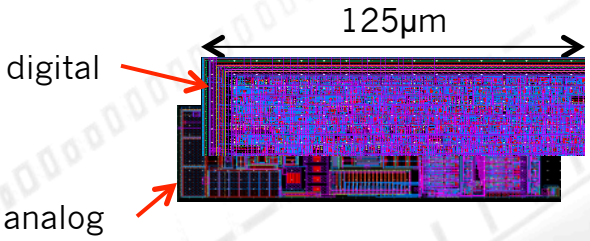
- 3D IC design uses via first/middle technology, i.e. TSV are formed before/after FEOL, at pixel level
  - Very small feature size, high via density → via pitch <10µm
  - Wafer thickness <50µm

- 3D ICs feature
  - small, fast pixels with high functionality
  - low power consumption
  - optimized technology for each layer

FE-I4, 130nm

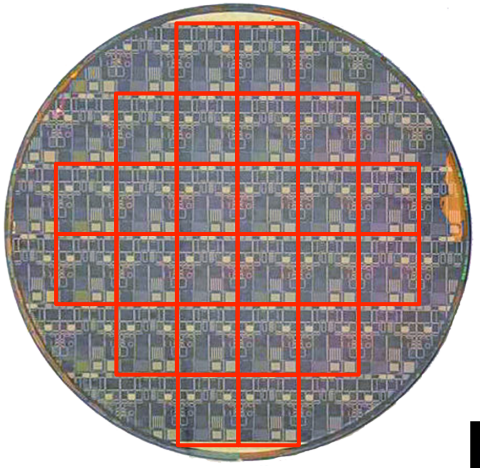


3D stack
Analog 130nm, digital 90/65nm

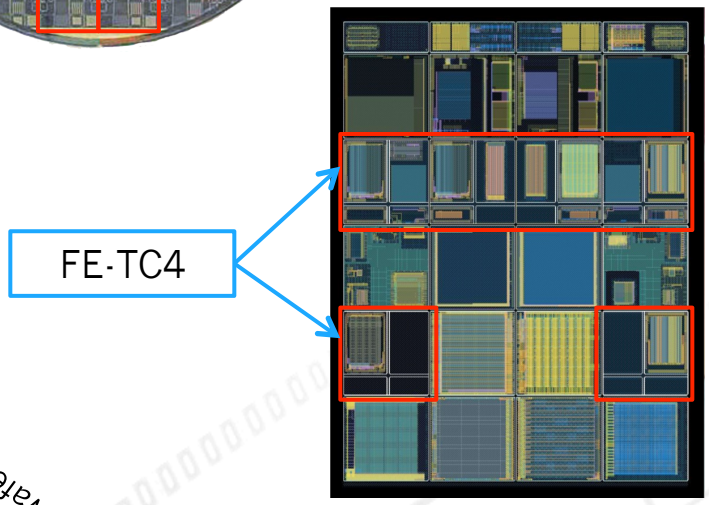


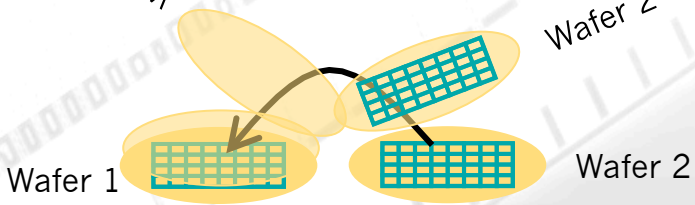
1st HEP 3D MPW run

- HEP consortium for 3D circuit design formed in late 2008
  - 17 groups from 6 countries (Italy, France, Germany, Poland, Canada, USA), led by FNAL
- Chosen technology: Tezzaron/Chartered
  - 130nm CMOS process (5 metal layers) from Chartered
  - 3D integration process from Tezzaron
- Two tier design
- Single set of masks for both tiers (cheaper) → identical top and bottom tiers, special mirroring in the design
- 24 reticules (26×31mm^2) hosting more than 25 two tier designs



Top		Bottom	
TX1	TY1	TY2	TX2
A1	B1	B2	A2
C1	D1	D2	C2
E1	F1	F2	F2
G1	H1	H2	G2
J1	K1	K2	J2





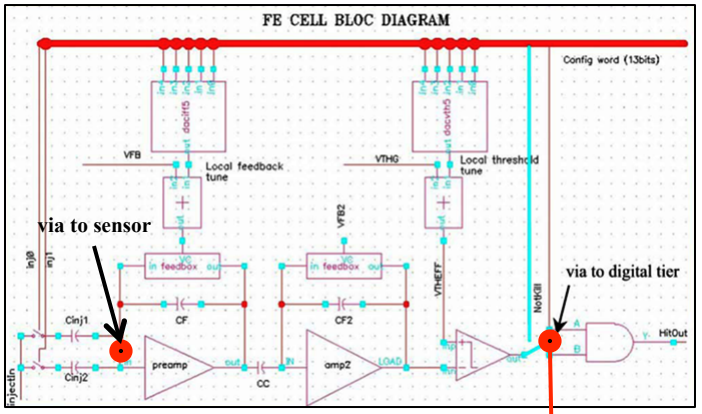
FE-TC4

- Institutes: Bonn, CPPM, LBNL

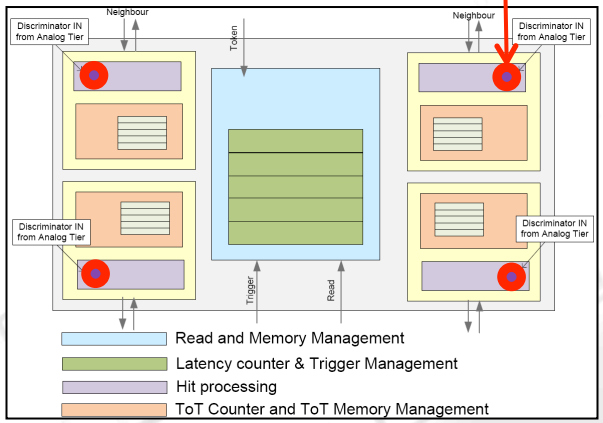
- 3D chip = analog tier + digital tier
  - Analog tier design based on FE-I4 prototype
  - Digital tier complex: digital 4-pixel region FE-I4 like
  - Digital tier simple: “drum” cells to test coupling between tiers
  - Both tiers can be configured and tested independently via shift registers
- Pixel size: 50×166μm²
- Pixel matrix: 14×62

- Analog 2D prototypes have been submitted as technology test bench (2009 – 2011)
  - Independent MPW run with Chartered
  - Good performance and radiation tolerance

Analog tier



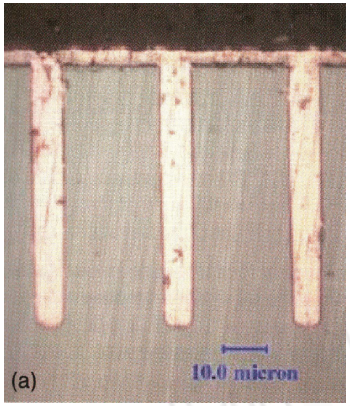
Digital complex tier

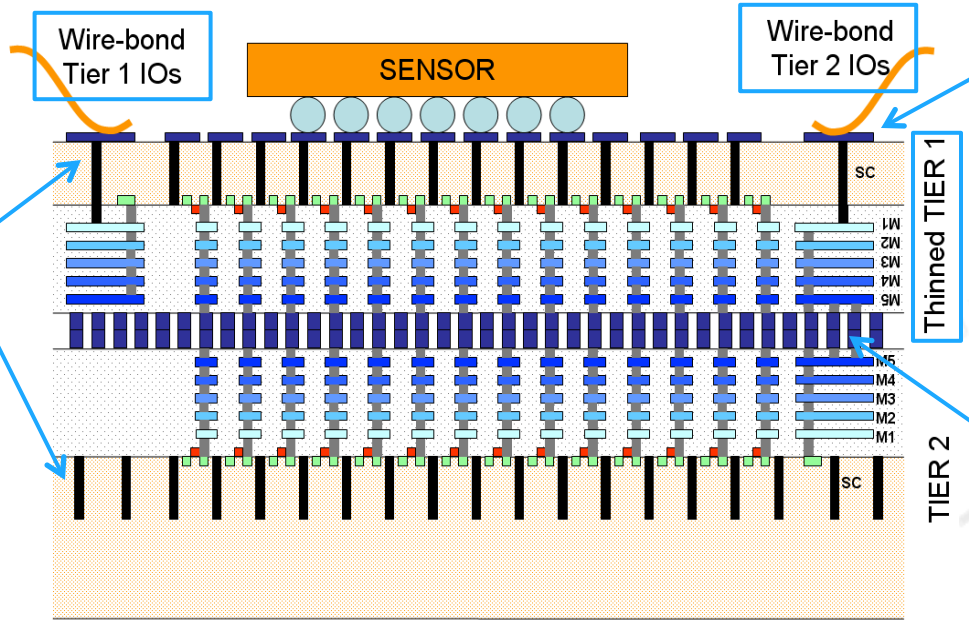


3D process at Tezzaron/Chartered

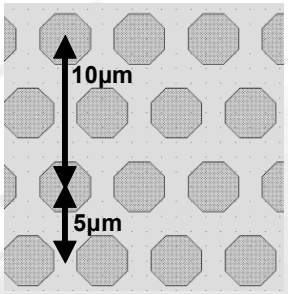
- Via Middle technology: Super-Contacts (TSV) are formed after FEOL of Chartered technology. Depth = 12µm, Ø = 2.5µm, R < 1 Ω
- 2 wafers (tier 1 and tier 2) are stacked face to face with Cu-Cu thermo-compression (electrical and mechanical connection)
- Top wafer is thinned to 12µm to access Super-Contacts
- Back-side metal for bonding (after thinning)
- IOs of each tier accessible, independent testing possible

Super-Contact





Bonding interface: Fine pitch & high density

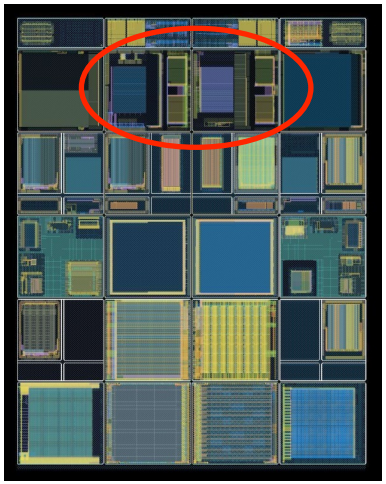


Submission issues and timeline

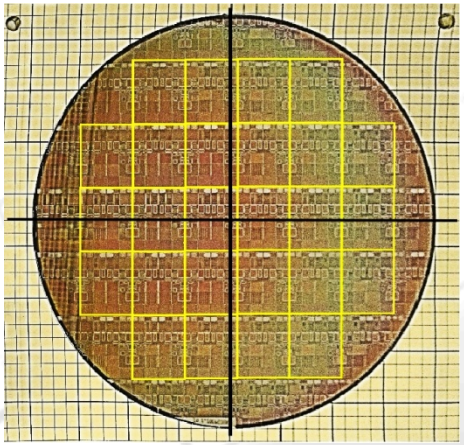
- This submission encountered issues at all stages of the process (wafer ordering, design, submission, processing)

- Timeline
  - May 2009 · All 3D designs initially completed
  - January 2010 – Global Foundries takes over Chartered Semiconductor (Personnel/equipment changes)
  - March 2010 · All rework done and designs finally accepted by foundry
  - October 2010 · Misaligned wafer lot completed
  - November 2010 – One misaligned wafer received for 2D testing
  - December 27, 2010 – Newly fabricated wafer lot received
  - March 9-10, 2011 · 3D Wafer bonding
  - April 2011 · Expected 3D wafer delivery
  - November 2011 – 1st 3D wafer delivery
  - June 2012 – Reworked 3D wafers received (some bonded at Ziptronik)

Layout incorrectly mirrored

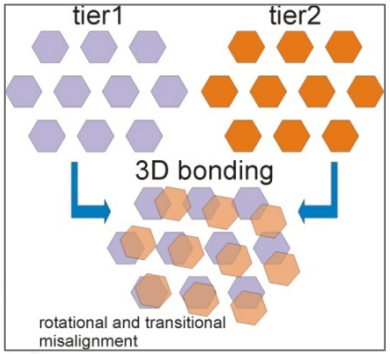


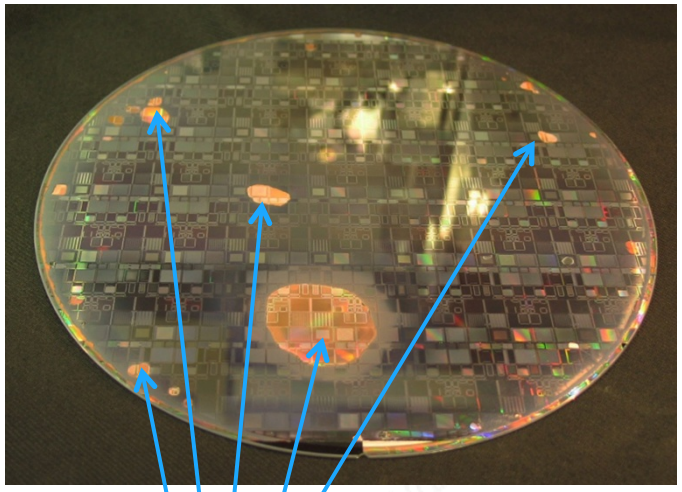
1.2mm misalignment between frames and wafer center lines



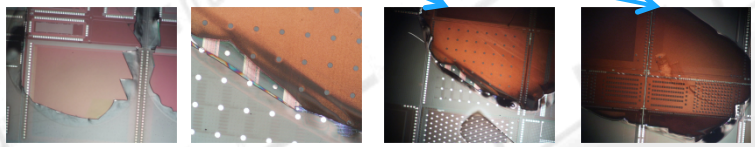
3D wafer delivery

- From the 1st 3D wafer delivery, only 3D bonded wafer pairs received for testing showing extensive damages on the surface
  - Bad electrical & mechanical connection due to misalignment of the tiers lead to top tier removal during thinning process → communication between tiers cannot be tested





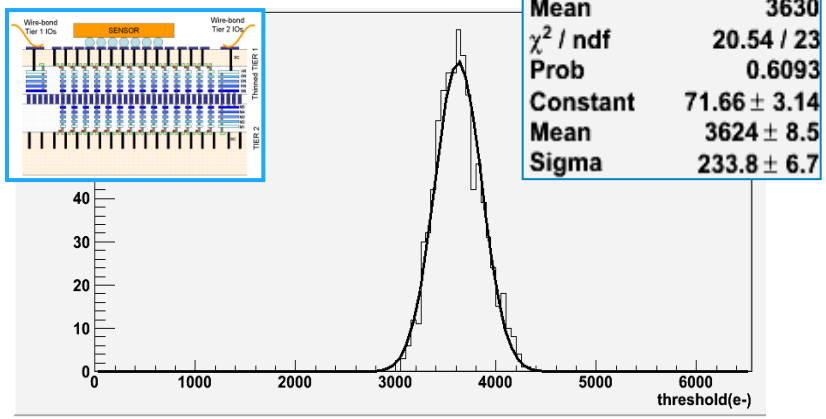
Damages on the wafer
Close up photographs

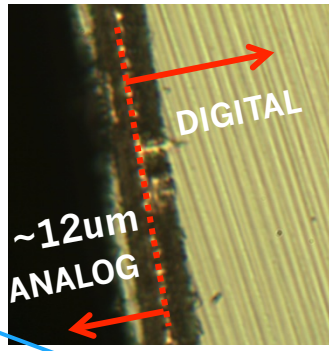


- Bonding on reworked 3D chips from the 2nd delivery was more successful
- 3 out of 4 FE-TC4 tested show communication between analog and digital tier (very preliminary results)!!!

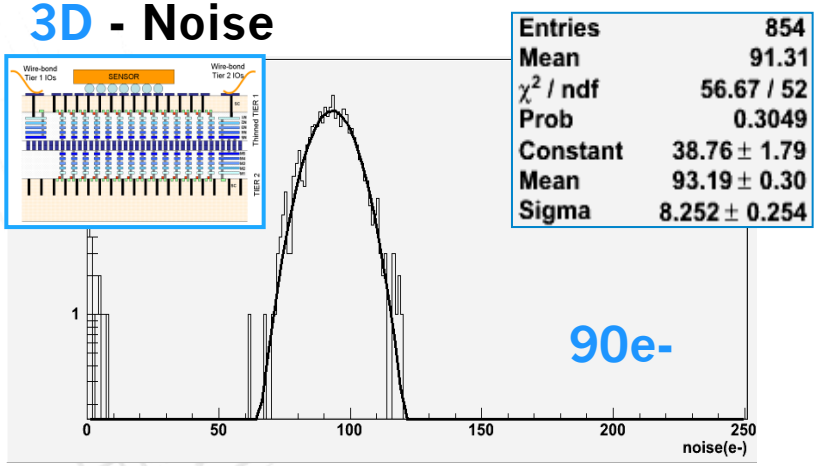
FE-TC4 test results: 12µm analog tier

3D - Threshold

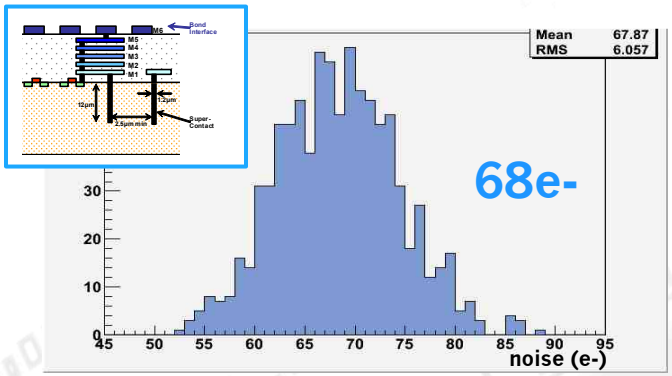




3D - Noise



2D - Noise



Analog tier with TSV, 12µm thin works with slight noise increase

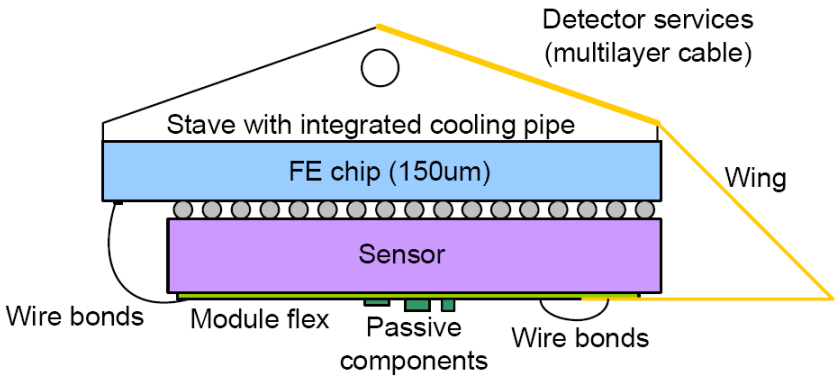
Post processing TSV

Post processing TSV for outer pixel layers

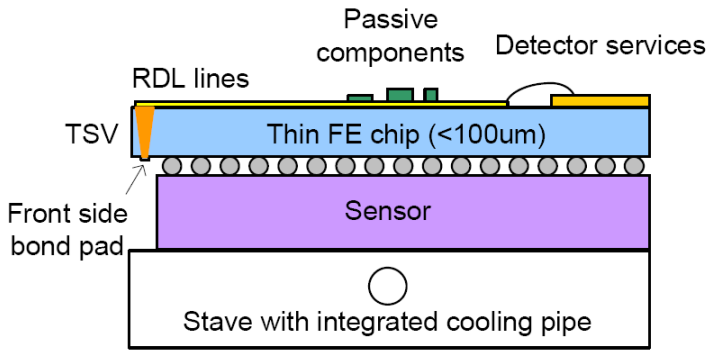
- Post processing TSV is a via last technology, i.e. TSV are formed after BEOL, in the peripheral bond pad
  - Large via feature (Ø up to bond pad size), low via density → via pitch ~100-150µm
  - Wafer thickness <200µm

- Hybrid pixel modules with via last TSV feature
  - Compact design → 4-side abuttable
  - Standard CMOS technologies with minimal modification to the traditional FE-layout

IBL module



Hybrid pixel module with TSV



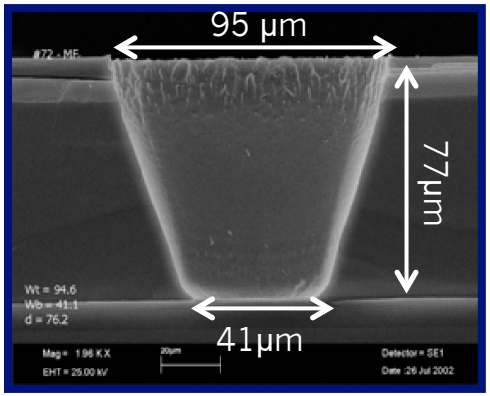
Via last TSV at IZM

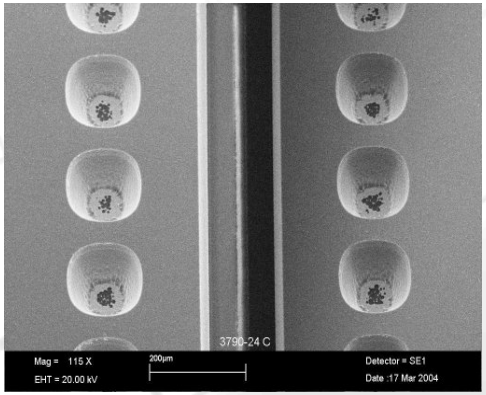
- IZM offers two via last TSV technologies: tapered & straight side wall TSV
- Both processes have been demonstrated on monitor wafers → TSV process works
- Tapered TSV process selected to build modules with ATLAS FE-I2/3 electronics

- TSV are etched in one step and oxide is deposited after etching
- Wrt Bosch process
  - Faster etching process
  - Simpler deposition process of isolation layer

- Via features
  - Side angle ~60°-70°
  - Bond pad pitch 150µm → Max wafer thickness 80-150µm
  - Current development at IZM aim at 300µm depth with Øtop = 150-200µm

Tapered Side Wall TSV on monitor wafer





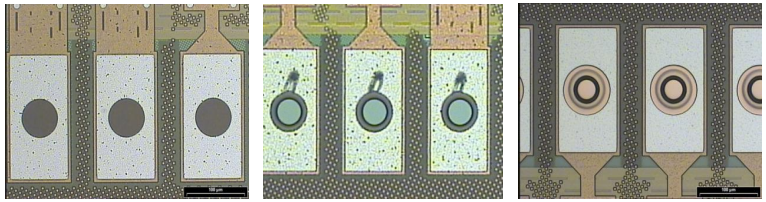
Tapered TSV processing on ATLAS FE-I2

1. Front side processing

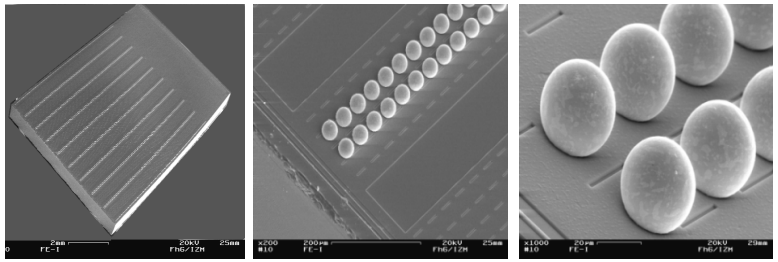
Al pad opening by wet etching

BEOL SiO_2 stac etching

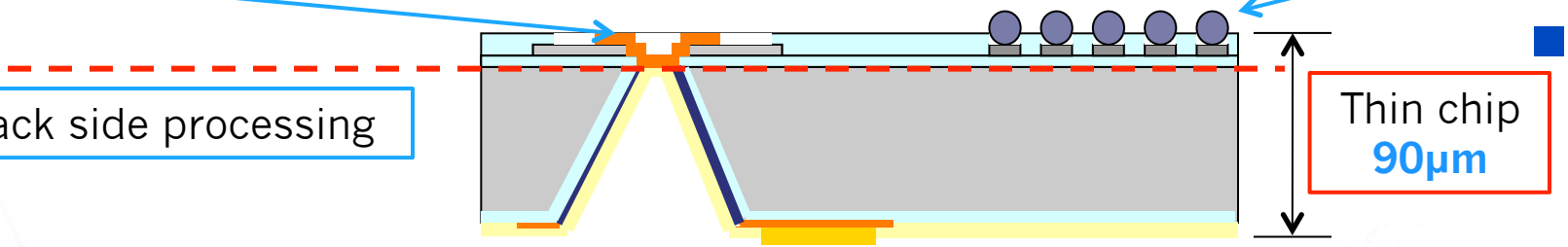
Cu electroplating – interconnection plug to Al pad



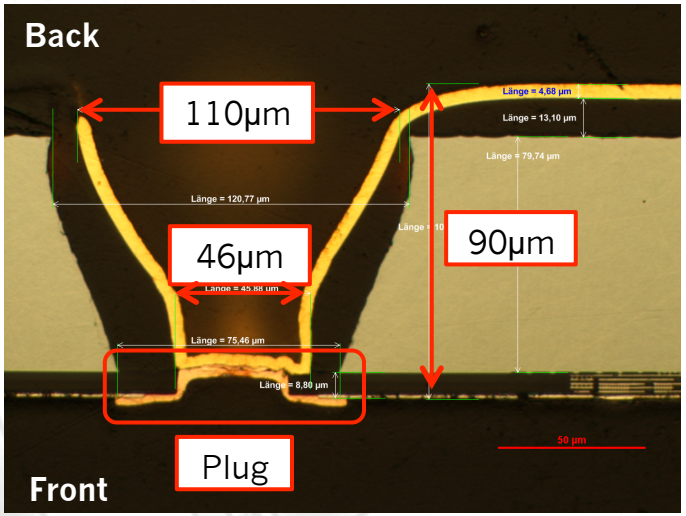
3. Bump deposition and dicing



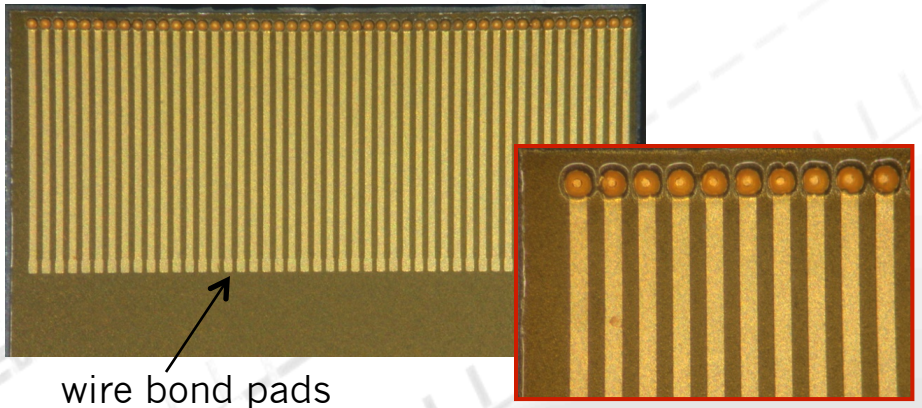
2. Back side processing



Thin chip
90µm



Re-Distribution Layer (RDL)

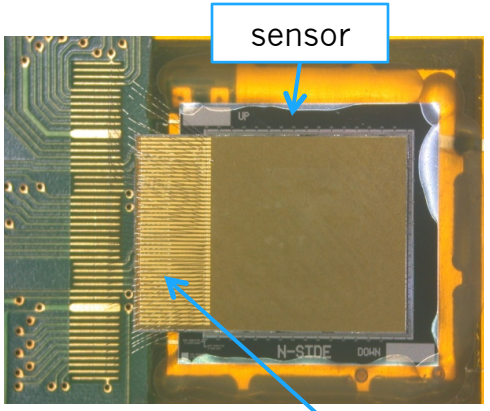


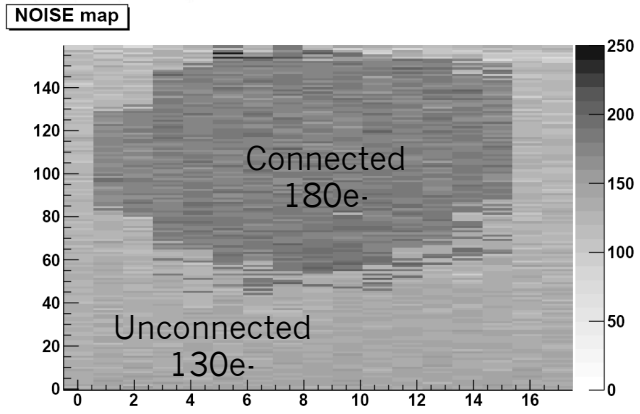
wire bond pads

TSV modules test results

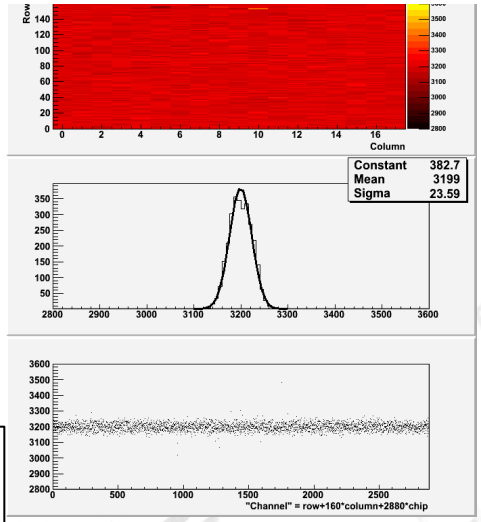
- IZM bump bonding method for thin FE not used → unconnected pixels expected along the FE perimeter
- No noise increase wrt FE-I3 bare chips and modules
- Module with TSV can be tuned without problems

→ No loss in performance wrt modules without TSV

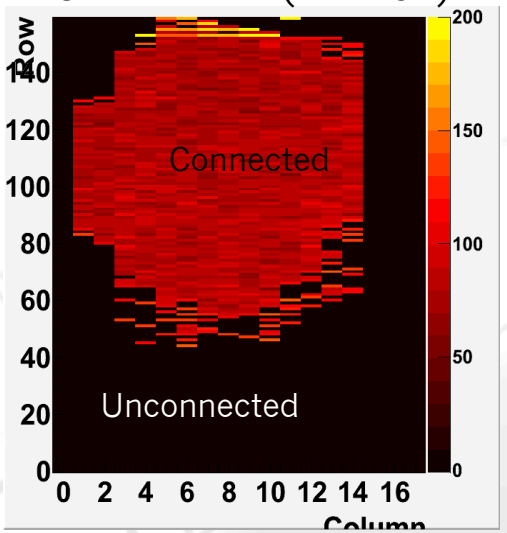




Threshold tuning to 3200e-



Source scan (Am-231)

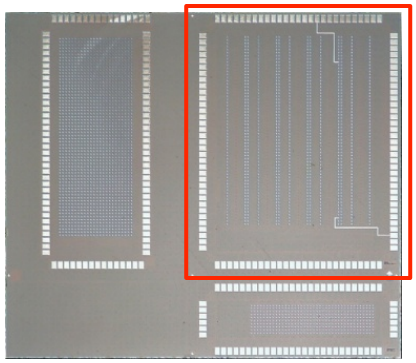


Work published at:
http://iopscience.iop.org/1748-0221/7/08/P08008/

Conclusion

- 3D technologies are investigated for the upgrade of the ATLAS pixel detector at the HL-LHC

FE-TC4
Analog on top



- IC design in 3D (via middle) allows to reach small pixel sizes with high functionality, low power consumption, and very low material. However, the technology presents still technical challenges for the industrial partners
- Working 3D chips just received (~3yrs)

- Post processing TSV (via last), despite the lower via density, can be used to design compact hybrid pixel detectors, using standard CMOS processes. They have proved to be technically feasible
- Next step: process FE-I4 wafers with the tapered TSV process from IZM