3D Electronics Development for Pixel Detectors

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Outline

- Motivation 3D
- Overview – MIT-LL (VIP chip) and oxide bonding
- Present Tezzaron 3D Run
  - VICTR & VIPIC chip results
- Towards large arrays (Active Edge, Tiling)

Future Challenges for Pixel Detectors

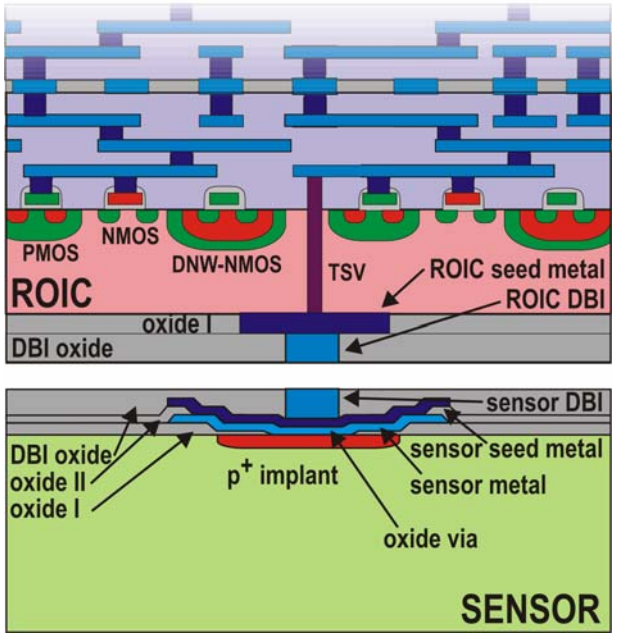
We believe that technologies related to 3D integration can address many of these issues and enable a new generation of uniquely capable sensor systems

- **Lepton Collider Vertex Detector – precision**
  - Superb impact parameter resolution (5μm ⊕ 10μm/(p $\sin^{3/2}\theta$))
  - Transparency (~0.1% X0 per layer)
- **Muon Collider – processing to deal with harsh background environments**
  - 1-3 TeV muon collider on FNAL site
  - ~~Substantial~~ Huge detector and radiation backgrounds
  - Fast timing and high precision for background rejection
- **CLIC – speed and precision**
  - ILC + ~ns time resolution
- **SLHC – large scale, high speed, harsh environment**
  - 100-200 int/25 ns crossing, track trigger required
  - On-detector background rejection
- **X-Ray Imaging – speed and density**
  - Variety of challenges – timing
- **Intensity frontier**
  - Thin, fast electronics

- **<25 micron pixels**
  - bump bonding density
  - density of electronics
- **50-100 micron thick sensors**
  - thinning processed
  - handling
- **large area ~ 100 m²**
  - yield and cost (tile-able)
- **ns time resolution**
  - power
- **radiation hard**
  - cooling, mass, materials

Fusion vs. Bump Bonding - Cost and Yield

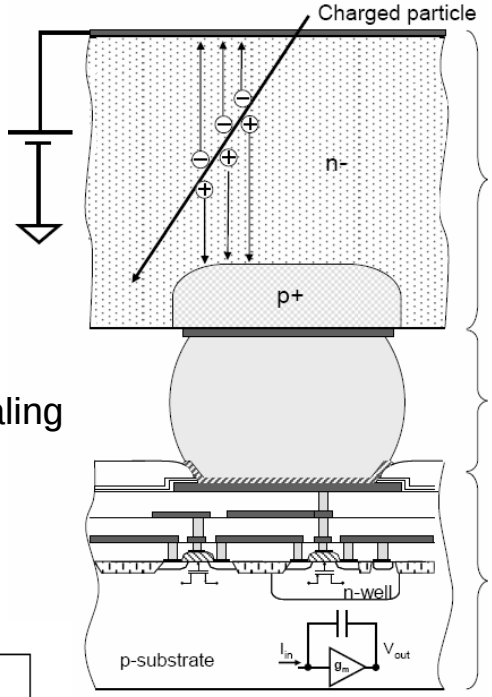
fusion bonding



In our studies the most promising fine pitch bonding technology is the direct bond interconnect (DBI) process from Ziptronix:

- very fine pitch:
  4 microns used for 3D Tezzaron wafers
- mechanical strength enables aggressive post-bond procedures:
  thinning, back implantation, laser annealing
- uses standard IC processes
  CMP and metallization
- can withstand high temperatures
- in principal: low cost

classical bump bond



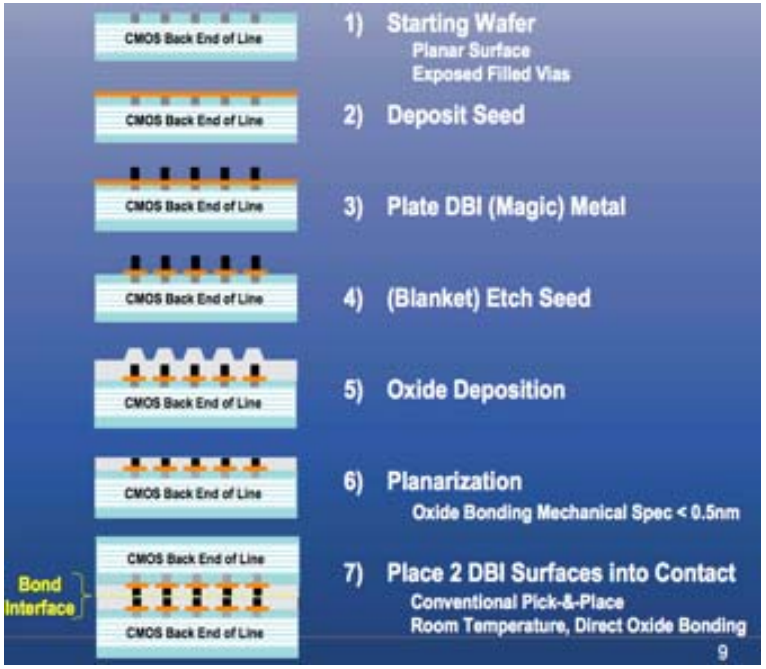
[R.Ballabriga, CERN]

Component	Current or projected cost	Yield	Comment
Readout IC	\$8/cm^2 [6]	65-70% [7]	Current 3D wafers and FEI4 prototype yield
Active Edge Sensors	\$53/cm^2	-	Current cost for prototype 150 mm wafers
Silicon Strip Sensors	\$10/cm^2	100%	CMS tracker costs
Bump bonding	\$213/cm^2	98%[8]	CMS forward pixel costs (2007) Yield ≡<20 bad bumps/chip
DBI bonding	\$0.04/cm^2	90%	Projected by Yole Development [9] for high volume production
Target Costs (2020s)	\$10/cm^2	90%	Assuming 200 mm sensor wafers and batch active edge process

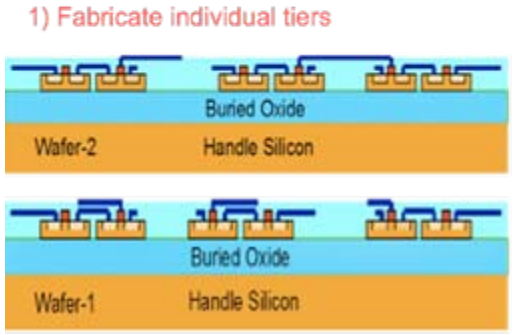
Current and projected costs and yields for sensor/readout integration technologies [1]

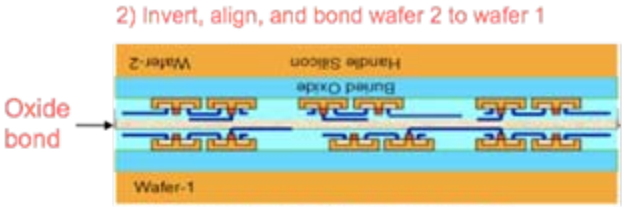
Processes Explored

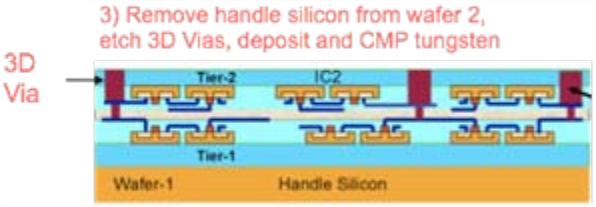
Ziptronix Oxide Bonding

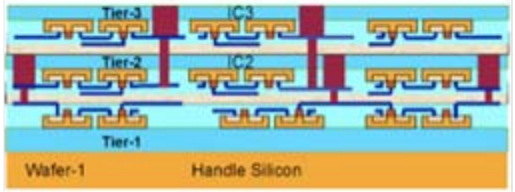


MIT-LL oxide wafer bonding

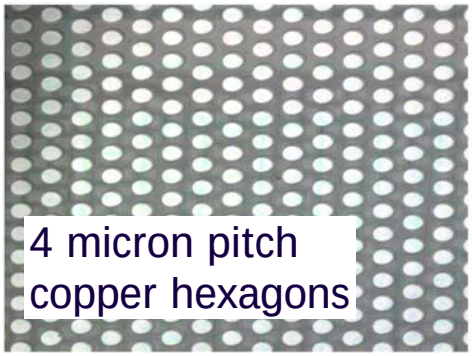


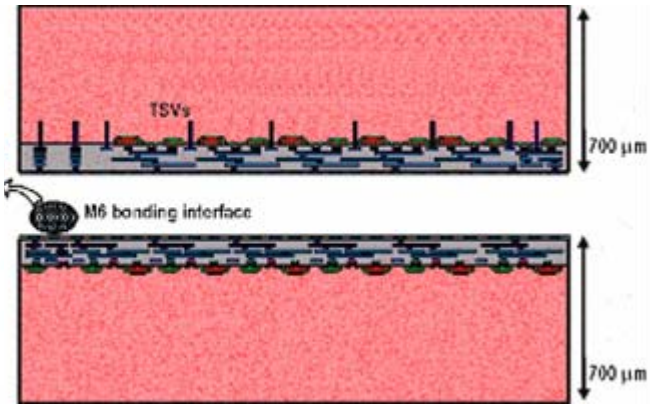


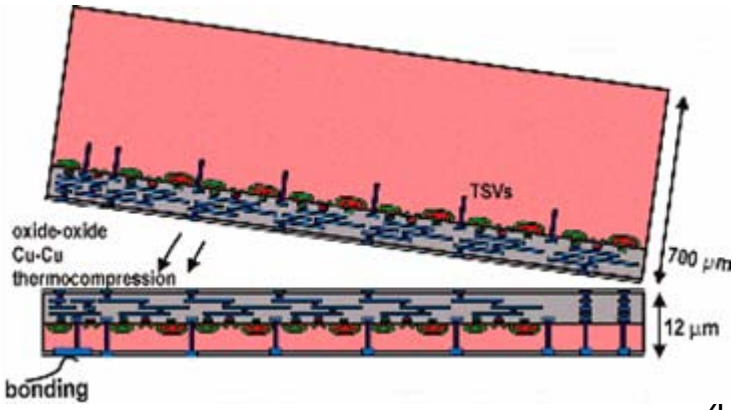




Tezzaron cu-cu bonding

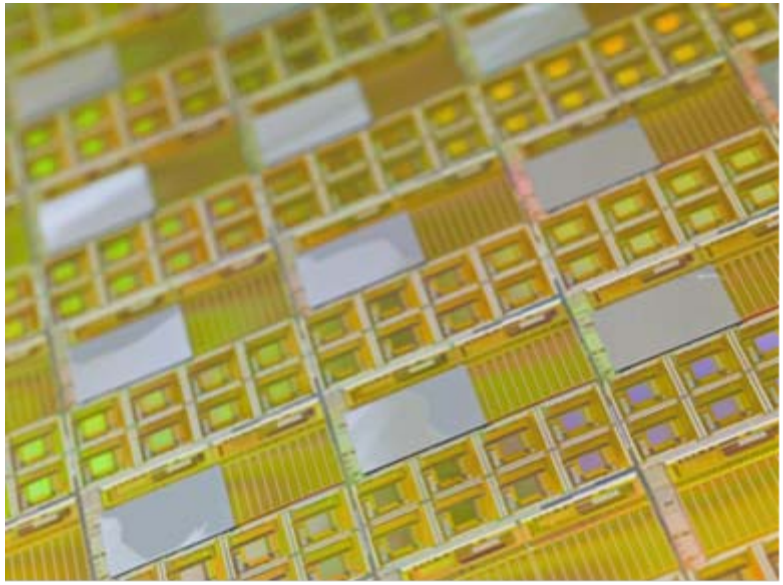


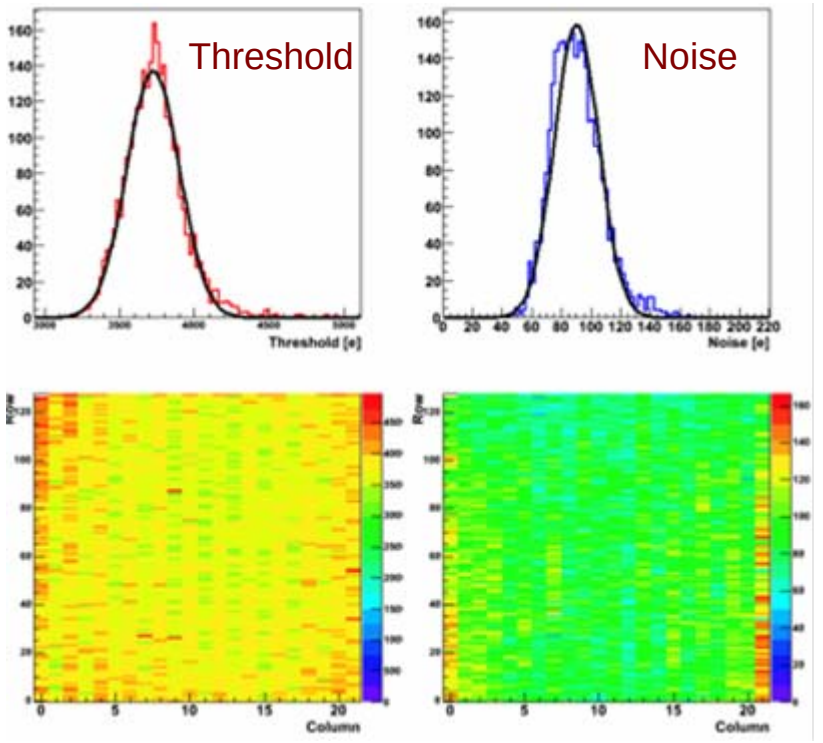




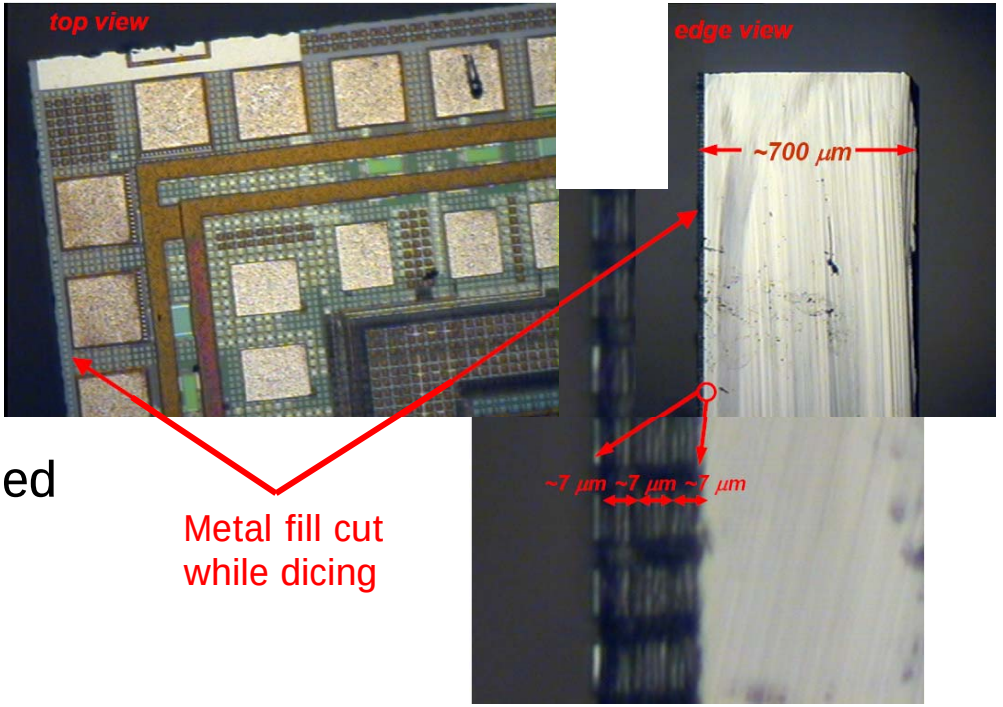
Oxide Bond Demonstration

- Initial work was based on existing ROIC wafers from BTeV and sensor wafers from MIT-LL
  - chip (sensor) to wafer (FPIX) bond
  - Sensors thinned to 100 microns -> 8 V depletion
  - 100% connectivity on sensors without obvious bond voids
  - No degradation in S/N
  - Radiation hard to >10 MRad
- Process used with 3D wafers (iphone camera), planned for track trigger, active edge and x-ray imaging projects



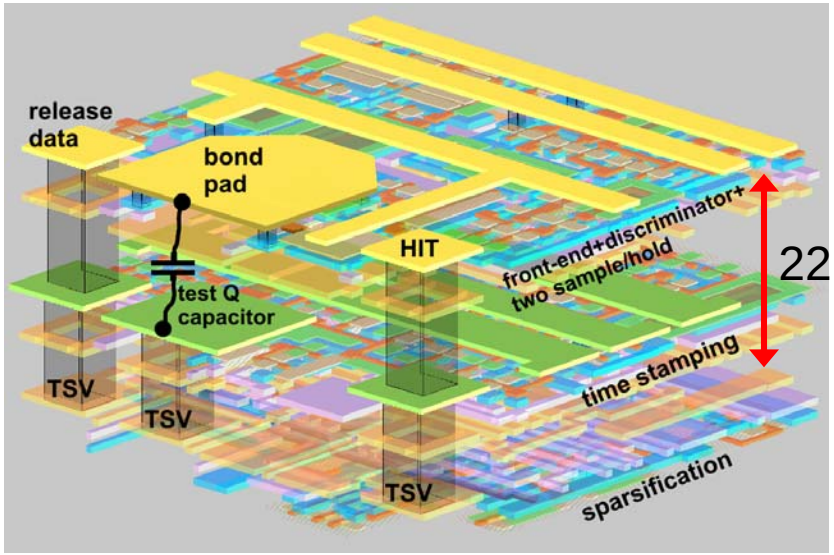


MIT-LL 3D Technology



- MIT-LL had developed a 3D technology which seemed an excellent match to ILC needs
  - Demonstrated 50 micron thick bonded sensor/readout (~0.1% radiation length/layer)
  - 3 Tiers of 0.18 micron SOI CMOS
  - Bonding, thinning and detector laser anneal technology
- We participated in 2 DARPA-sponsored 3D runs (2006/2009)
- Submitted the VIP ILC- vtxd chips (participated in improving the design kit)

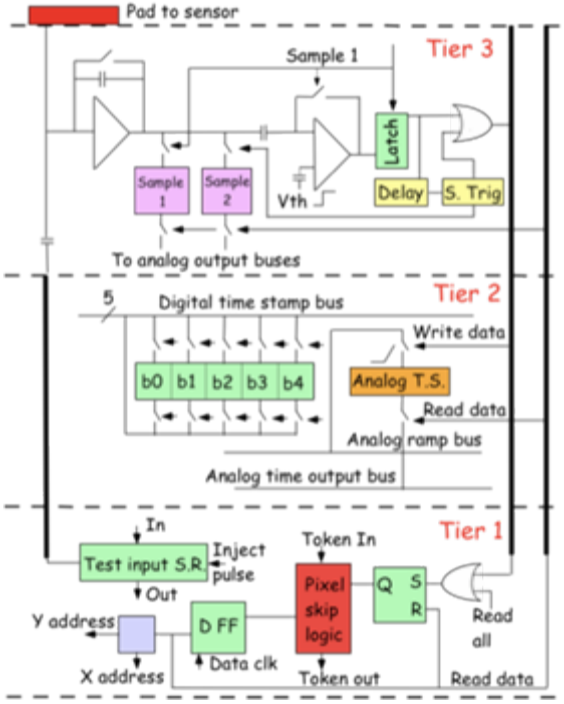
Micro Magic Pixel Layout



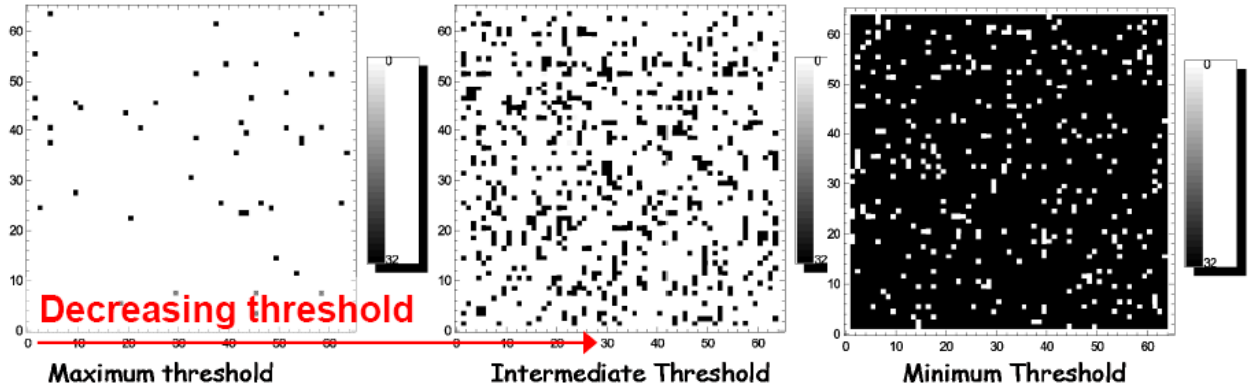
VIP Chip (MIT-LL & Tezzaron)

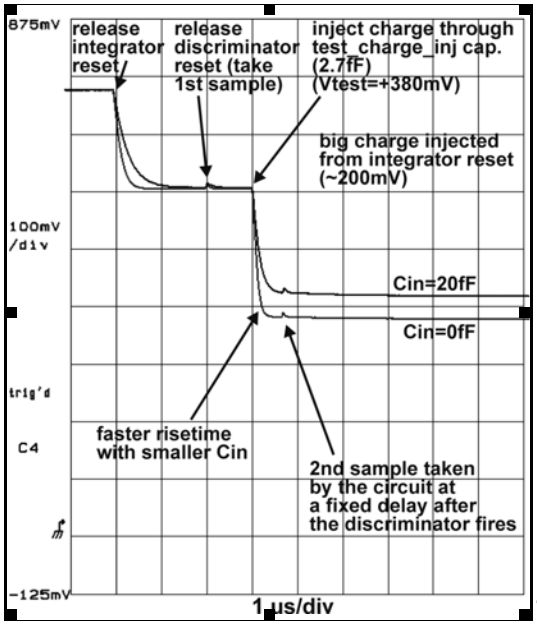
- <25 micron pixels
- 50-100 micron sensors
- Large area ~ 100 m^2
- ns time resolution
- Radiation hard

- Chip designed for ILC Vertex
  - Low power front end
  - Digital and and analog time stamp (~3-200 BX resolution)
  - Sparsified readout
  - 20(VIP1), 24(VIP2a) micron pitch
- Initial submission had low yield and marginal functionality due to MIT-LL process issues.
- Second submission (SOI->CMOS) with a more conservative design worked well. Converted to 0.18 micron CMOS for 3D Tezzaron run VIP2b. Analog performance of the 2D VIP was tested and reported last year.
- Full 3D VIP2b is received at Fermilab – expect begin testing in October



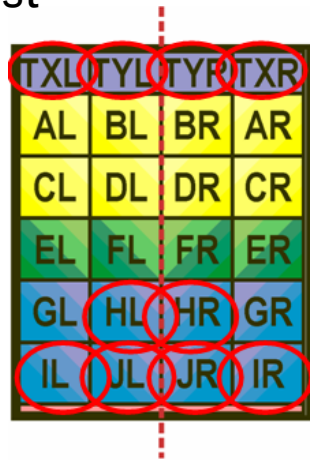
Data readout out using data sparsification scheme.

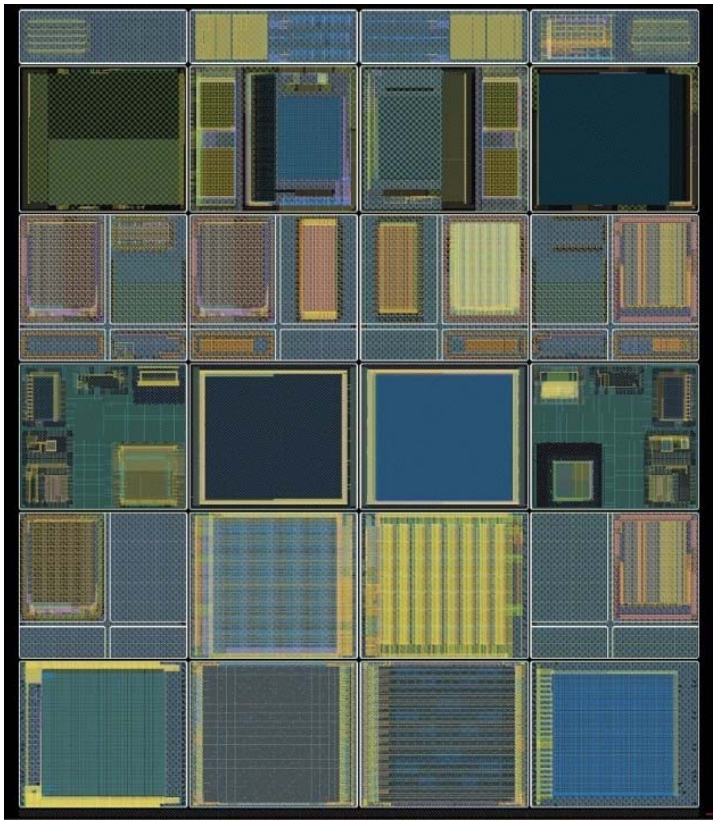


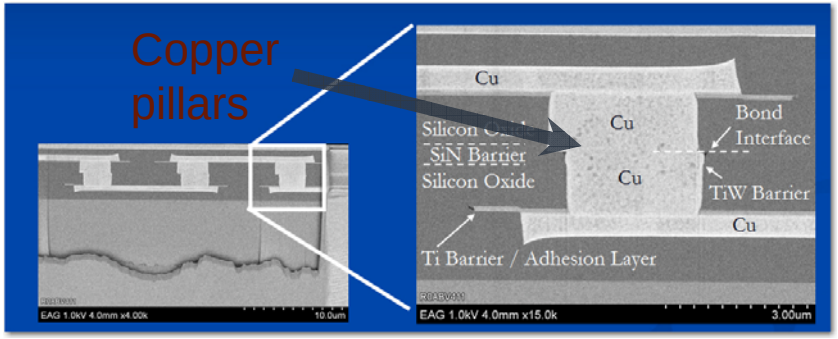


Tezzaron 3D Run

- 3D consortium formed in late 2008
  - 17 member groups from 6 countries (France, Italy, Germany, Poland, Canada, USA)
- Tezzaron Process
  - Two tiers, 0.13 micron CMOS, TSVs
  - Single set of masks to reduce cost
  - Cu/Cu thermo compression
  - face to face bonding
  - wafers thinned to 12 um
- More than 25 two tier designs
  - ATLAS pixels
  - CMS strip ROIC for track trigger
  - X-ray imaging
  - B-factory and Linear Collider pixels
  - Test circuits
- Frame divided into 24 subreticules
  - 12 for top tier
  - 12 for bottom tier



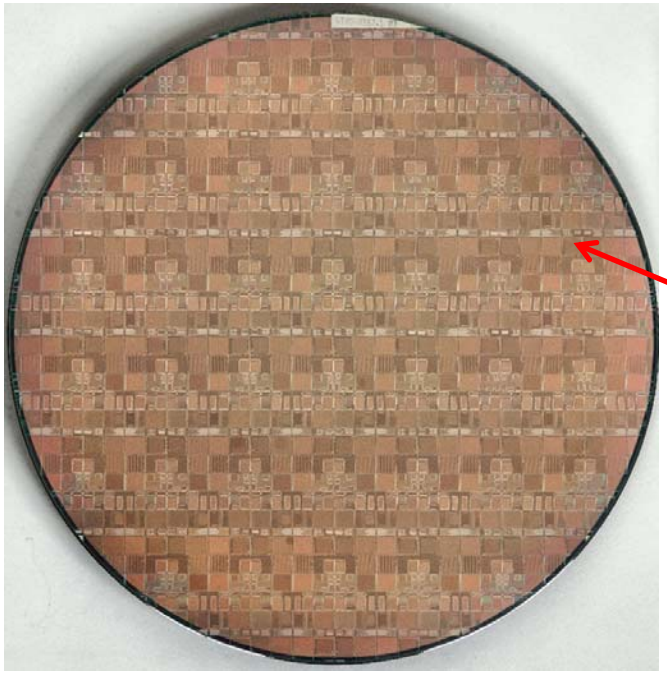




3D Run History

- **Design Issues (2008/2009)**
  - Designers did not use the same design kit (Top Metal, MIM Caps, SRAM)
  - Some design rules were interpreted incorrectly
  - Conversion issues Cadence -> Micro Magic (off grid rounding)
- **Submission Issues (2009)**
  - wrong frame size (street size, labels, 3 revisions)
  - incorrect mirroring by the mask house
- **Fabrication Issues (2010)**
  - Global/Chartered did not properly place frames on wafers, symmetry violated (rerun 31 wafers, no cost to users)
- **Bonding issues (2011)**
  - equipment being relocated / staff changed
  - Improper removal of 400nm of protective nitride (-> unbonded areas, insufficient bonding strength for grinding)
  - Misalignment in bonding (1.2mm)
- **Wafer Recovery (2012)**
  - Wafer resurface and bonding using Tezzaron Cu-Cu as well as Ziptronix DBI

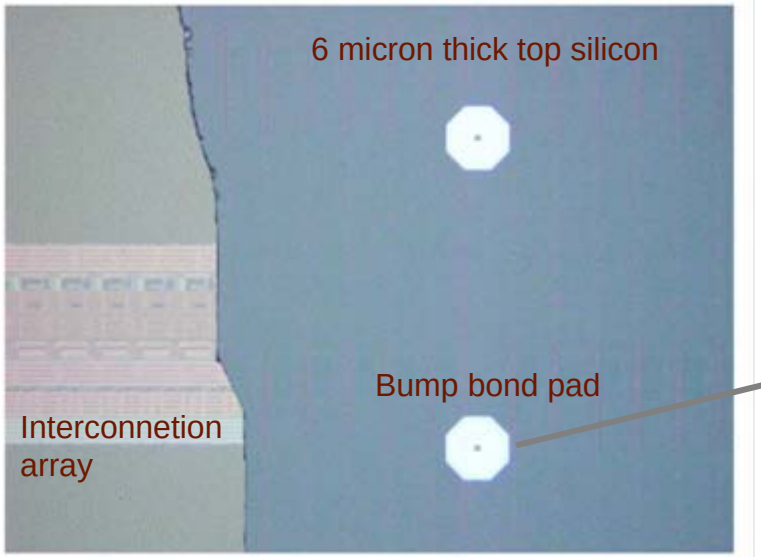
Status of Tezzaron/GF 3D run



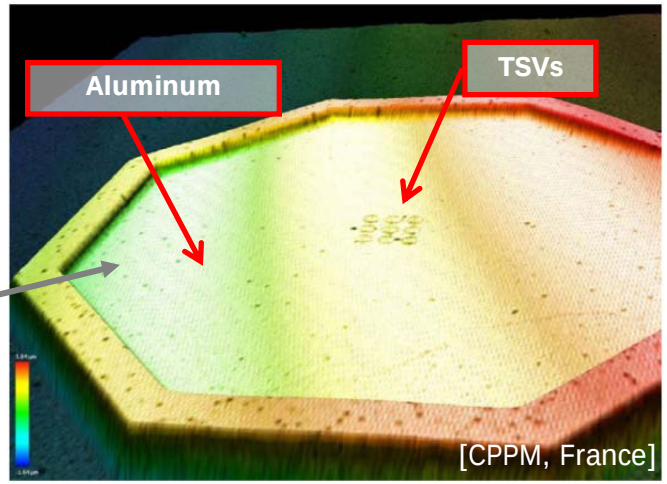
Wafer were back-thinned, back Al pads were deposited, chips diced and distributed

2 Wafers with some well bonded chips received in June

18 backup wafers **just completed** and awaiting 3D bonding, we continue exploring two paths for bonding:
- Tezzaron (removal of oxide to raise Cu bond pads)
- Ziptronix (smaller pads to increase oxide bond area)



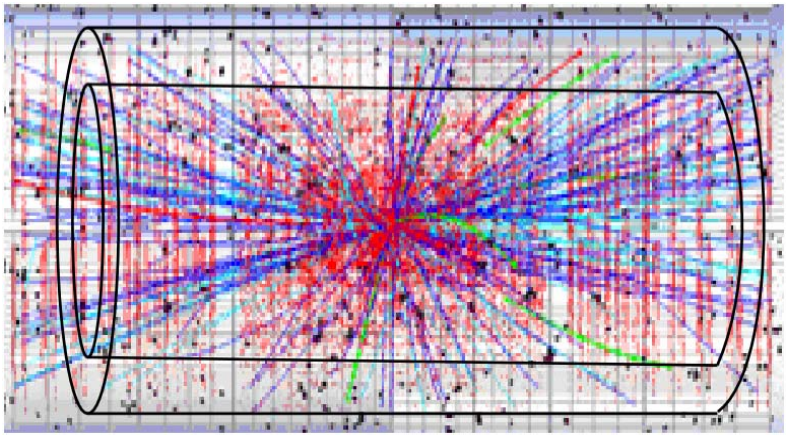
Exposure of TSV tips at AL pad

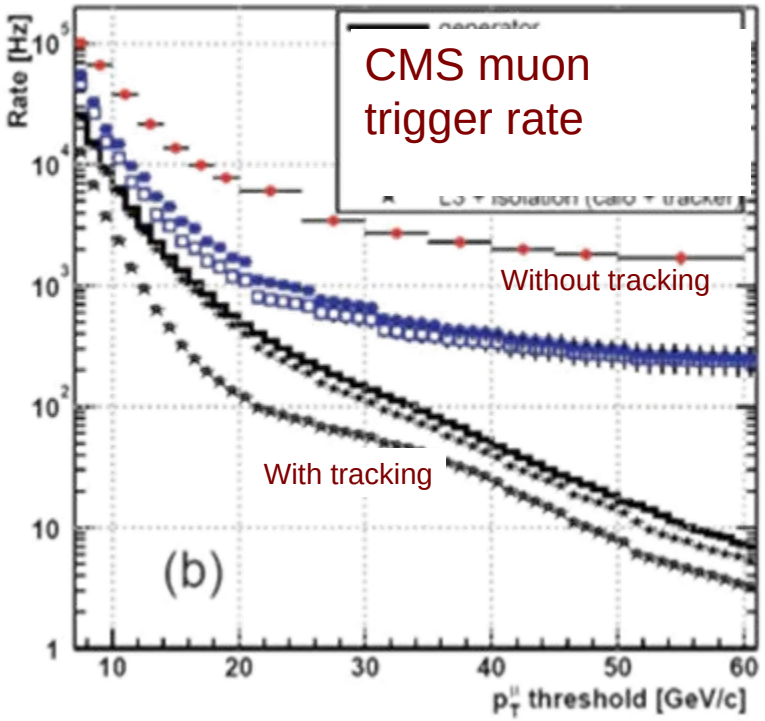


Key 3D steps:
- Backside processing,
- TSV formation and
- TSV exposure,
- Metallization

Track Trigger for CMS (~2020ies)

- <25 micron pixels
- 50-100 micron sensors
- Large area ~ 100 m^2
- ns time resolution
- Radiation hard

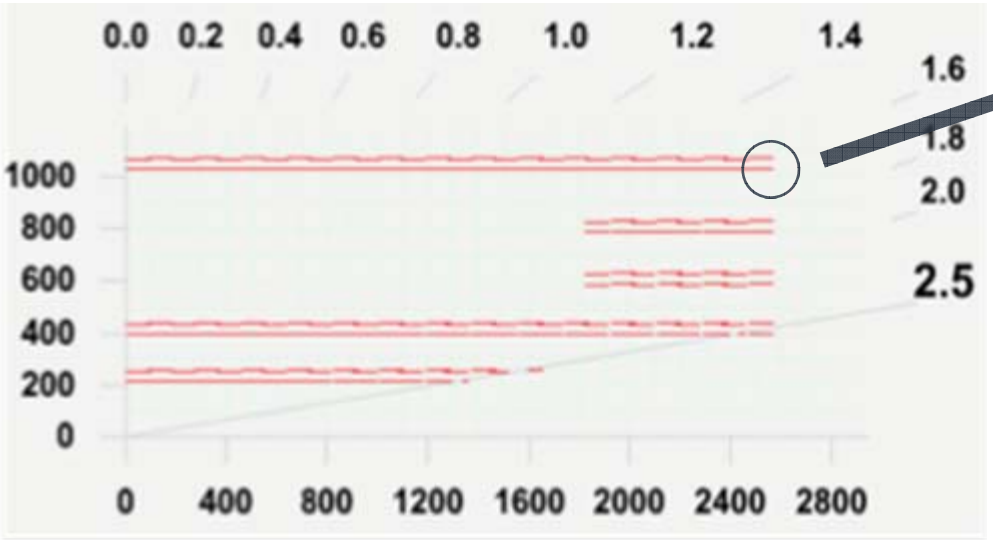


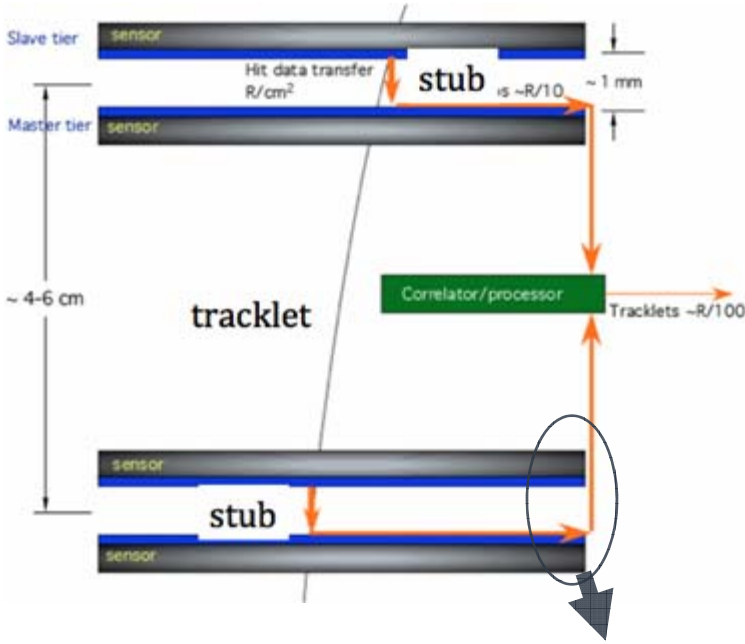


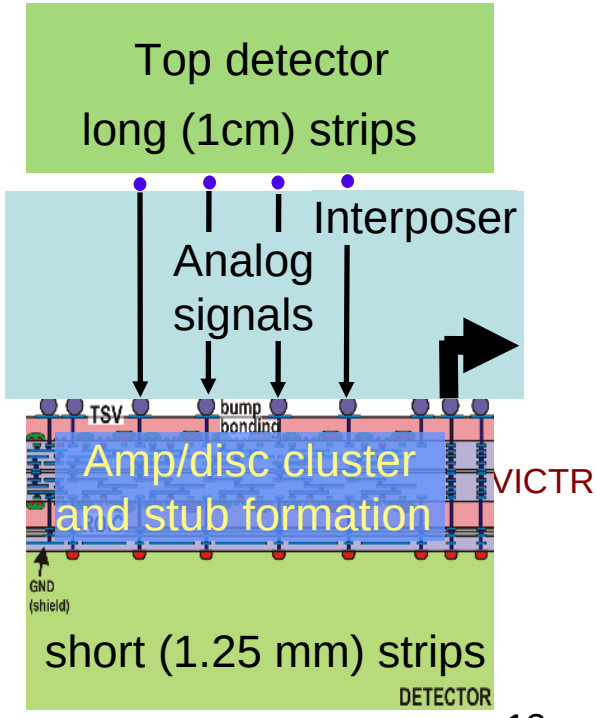
- It has become increasingly clear (since 2009) that CMS will need a L1 trigger for HL-LHC:
  - Must be (40MHz/100kHz) = 400 times faster than a L2 trigger like FTK or SVT
  - Good Z resolution to reduce background event candidates. Minimize the tracks used for isolation.
  - Limit rate at the front end by using correlated layers (x200 rate reduction)
- 3D is a key enabling technology for a “local” design (minimizing data transmission)

Tracker Design / VICTR chip

(with Cornell, Brown)







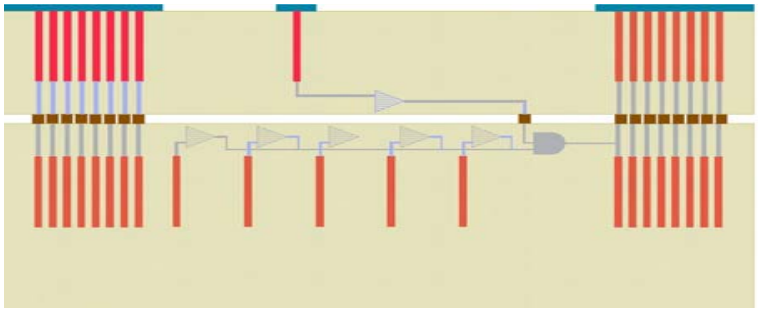
- Stubs found in sensor pairs
  pt > 2.5 GeV threshold
  - 3D chip (VICTR) used to correlate top and bottom sensors

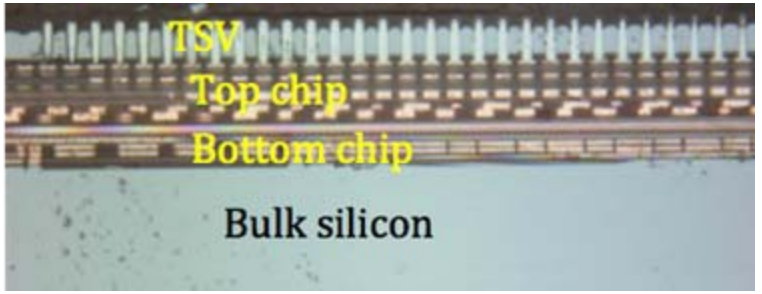
Tracklets found in module pairs in a rod

Tracks found using precise extrapolation of tracklets to other layers (tracklets have good Pt, position resolution)

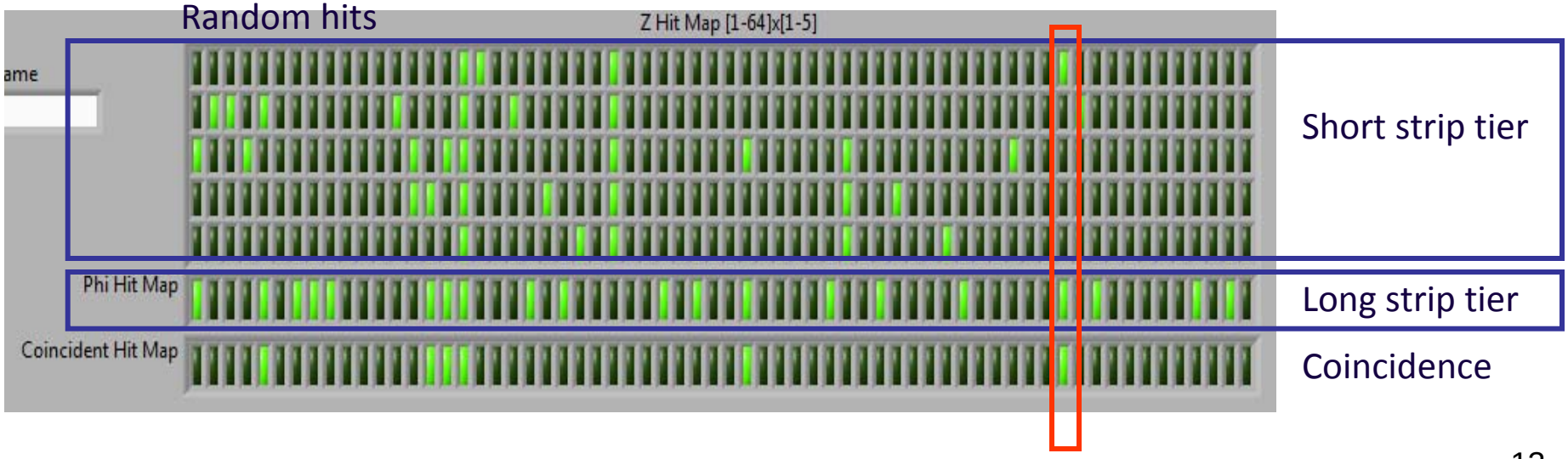
Our current design provides full sets of tracks to L1 in ~1.5 microsec

VICTR Test results

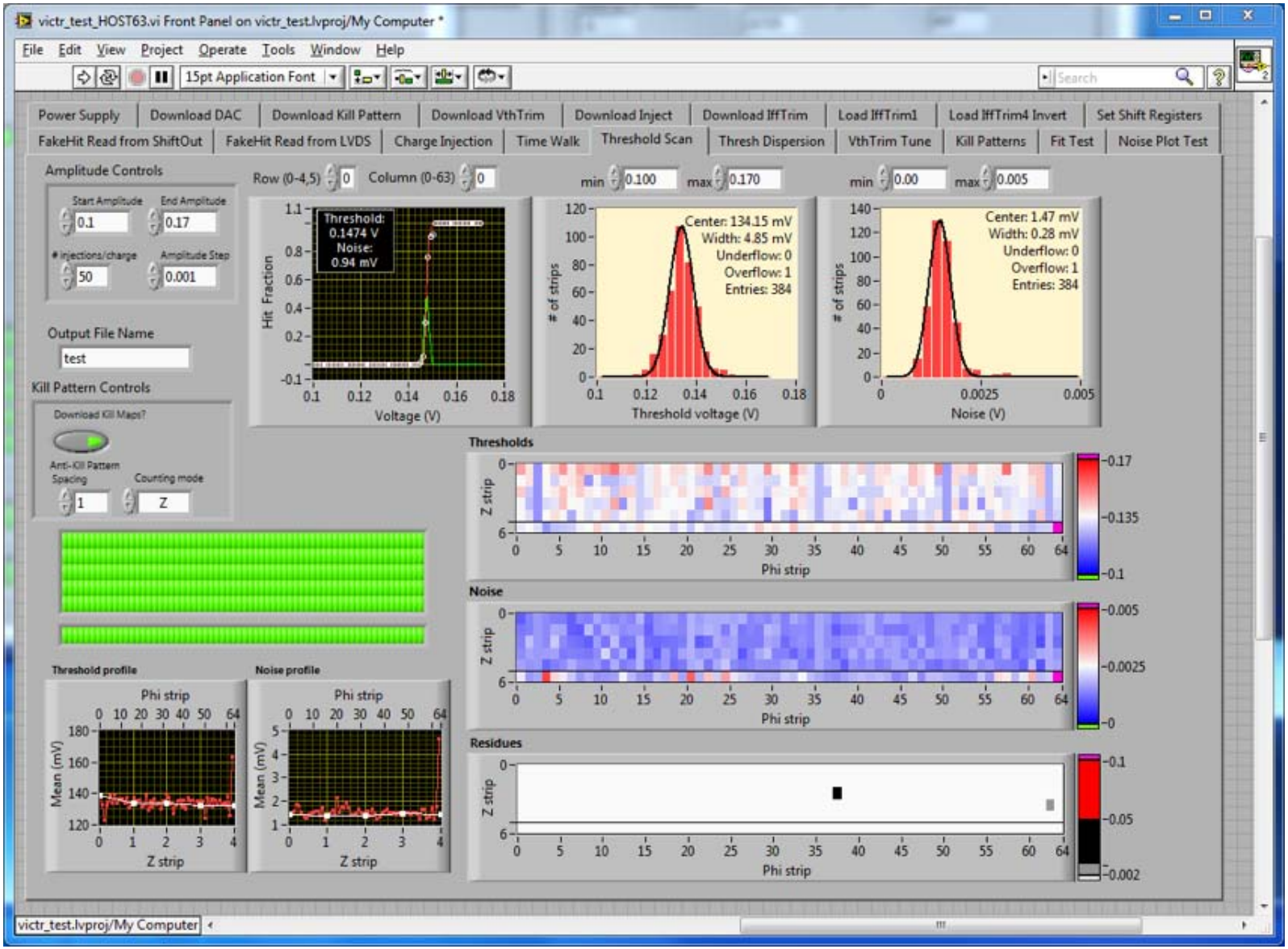




Observing top and bottom tier fast and slow outputs **as well as coincidences between tiers** –> indicates successful 3D bonding



VICTR DAQ (Threshold scans)



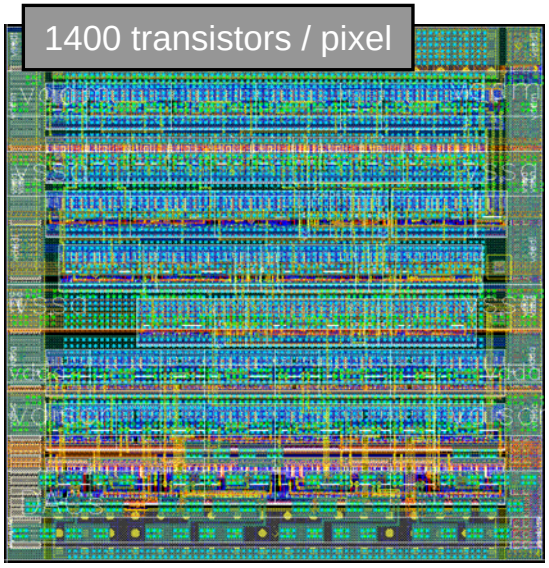
Analog Portion (modified version of LBNL's ATLAS FEI-4) of the chip tested and correspond to expected performance (noise, threshold dispersion)

VIPIC – Xray Imaging (Tezzaron 3D)

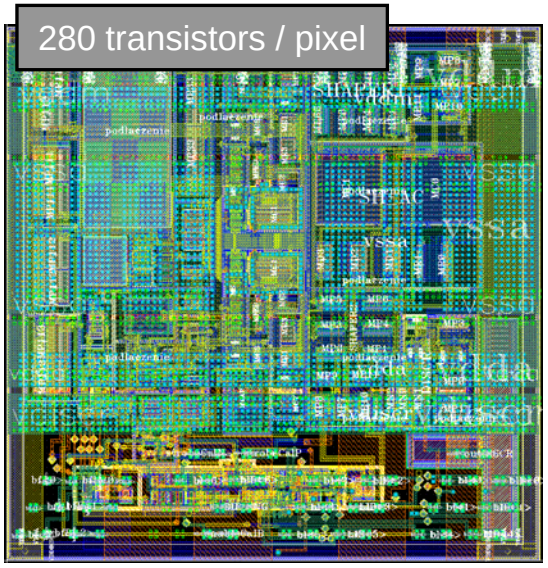
(with AGH Krakow, BNL)

- <25 micron pixels
- 50-100 micron sensors
- Large area ~ 100 m^2
- ns time resolution
- Radiation hard

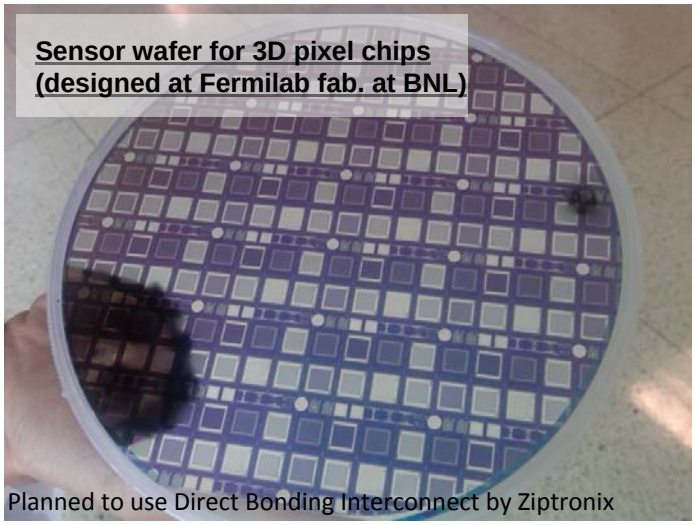
- XPCS light source applications (2D autocorrelation)
- 64 × 64 array of 80 um^2 pixel, shaping time t_p=250 ns, power ~25 mW, analog pixel noise <150 e- ENC
- dead-time-less operation
- Data sparsified readout with priority encoder circuit
- Imaging: counting of events (2x 5bit counter) at frame rates ~10ms
- Present Development: featuring TOA mode (10ns timing) and cluster reconstruction to compensating charge sharing (2D prototype fabricated)



Digital part of pixel



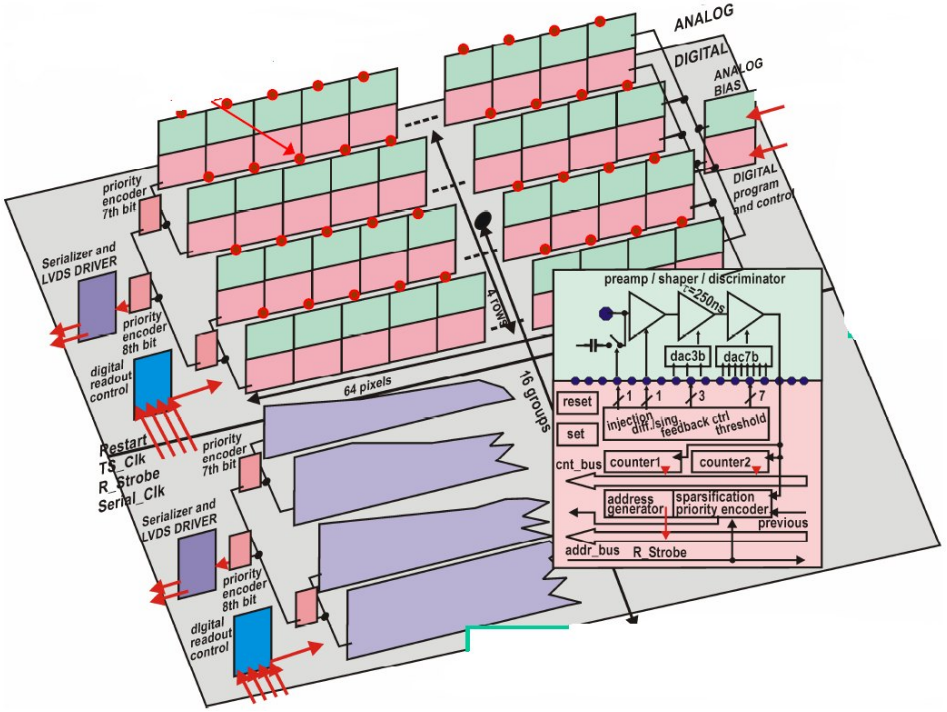
Analog part of pixel

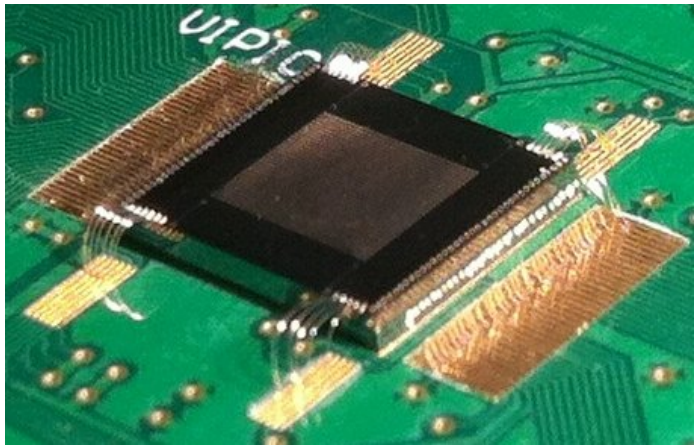


VIPIC – First Results

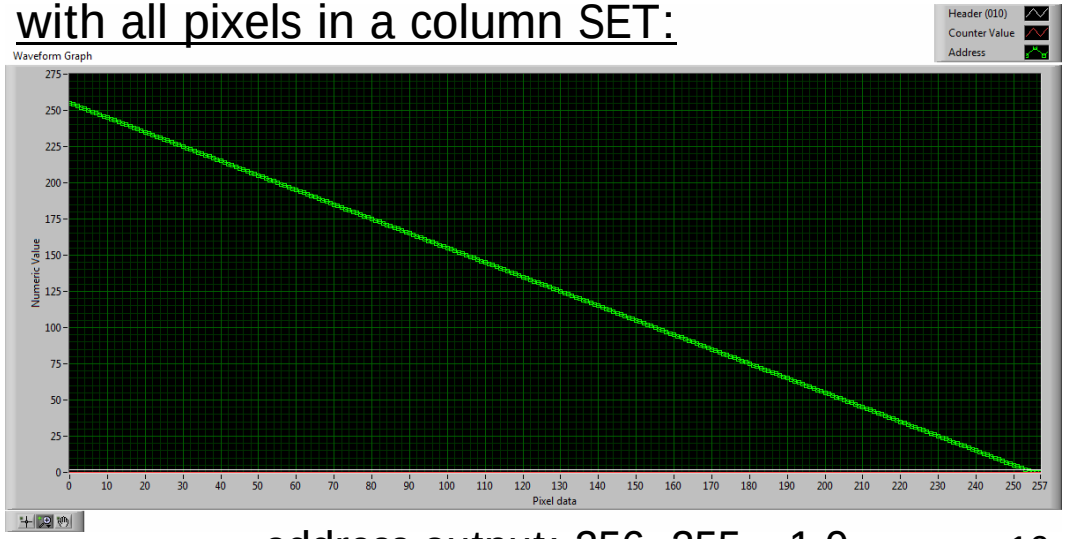
Initial tests results:

- program all pixels to be set
- read out all 16 column blocks with each 4 x 64 addresses through the sparsification system
- observing noise hits – counters respond proportional to threshold settings
- **DACs work -> 25 connections between analog and digital tiers of each pixel are working!!**
- More detailed tests soon!





Output of full sparsified readout chain with all pixels in a column SET:

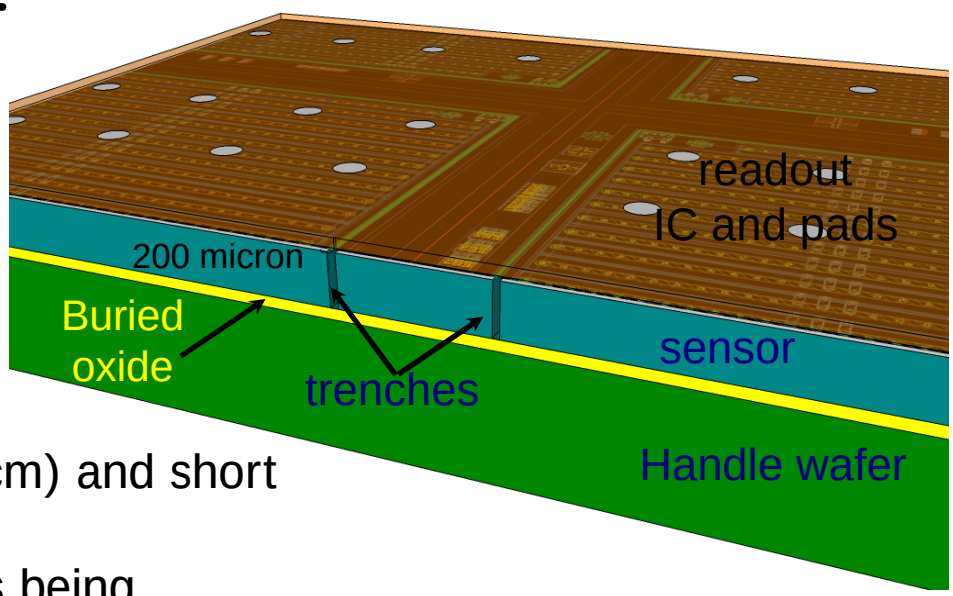


address output: 256, 255....1,0

3D Outlook:
Towards large scale / 'edgeless' detector systems

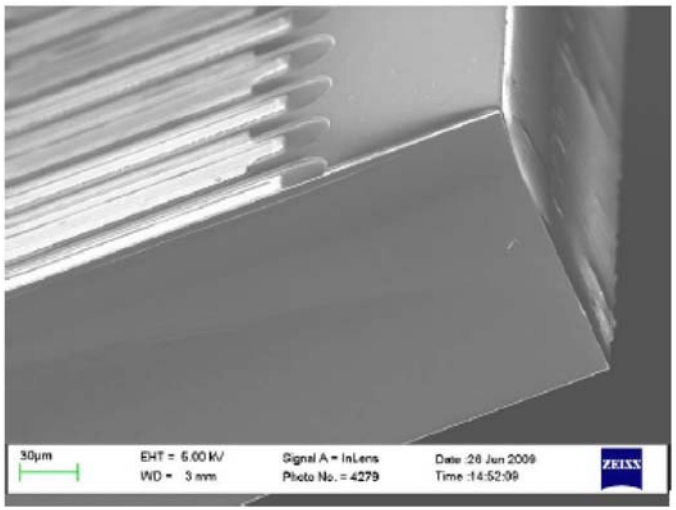
Active Edge Project

(with Cornell, SLAC, Hawaii, Brown, UCSC, NRL)



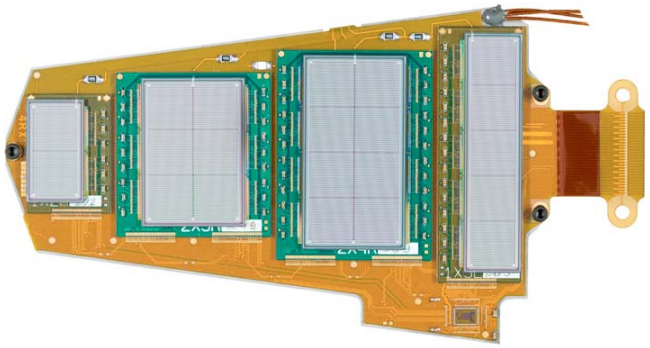
- We are building a demonstration array including active edge sensors, oxide bonded wafers, and “damascene” dummy readout wafers:
  - Sensors (fabricated at VTT) match the geometry for CMS track trigger long (1 cm) and short (1.25 mm) strip sensors.
  - Top tungsten plug “damascene” wafer is being fabricated at Cornell - designed to readout either long or short strips with single reticule.
  - Wafer bonding top thinning, etch and interconnect at Ziptronix
  - Singulation and handle wafer removal will be done at Stanford in collaboration with SLAC
  - There are no trenches on the edge reticules to allow test of the UCSC/NRL “slim edge” process
- Processing of the VTT and Cornell wafers is underway Ziptronix interface design is complete - should get results next year.
- Next step - move to 8” sensor wafers

VTT Active Edge sensor



Towards large scale detectors (hep and imaging)

CMS forward pixel plaquette



The Problem: Build large area arrays of highly pixelated detectors with minimal dead area and reasonable cost

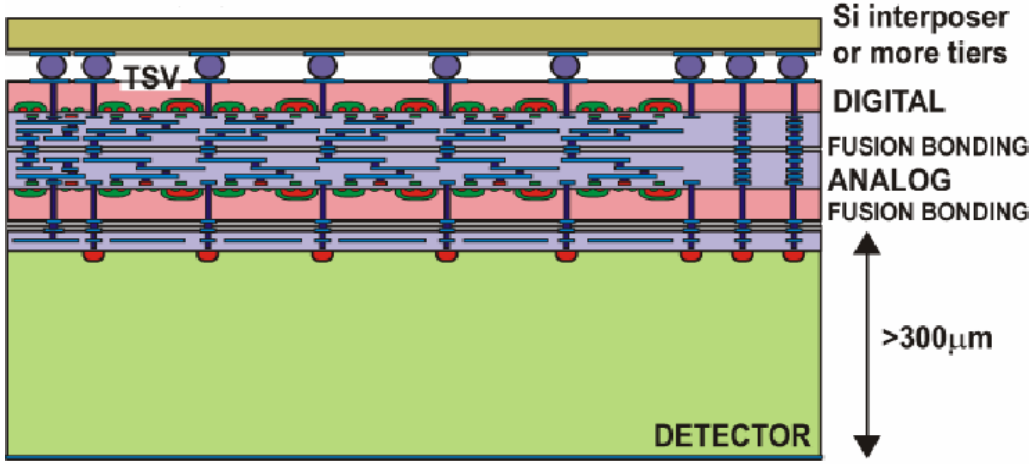
Current pixel detectors have dead areas arising from

Sensor Edges Wirebond connections for

Readout Integrated Circuits (ROICs)

A solution:

- 3D or vertically integrated electronics provides path for extraction of signals,
- Active edge sensors remove dead area at the edges



Combine:

- active edge technology with
- 3D electronics and
- oxide bonding with Through-Silicon-Vias to produce fully active tiles

Tiles can be used to build large area pixelated arrays with good yield and reasonable cost (e.g. SiD forward disks)

Summary

- 3D technology offers unique opportunities for pixel detectors
- For many future hep/imaging challenges 3D integration is appropriate solution
- Tezzaron run finally provided useful chips; final batch of wafers still to be delivered
- First test of ‘recovery lot’ shows successful 3D bonding (VICTR tested, VIPIC tested, VIP tests scheduled)

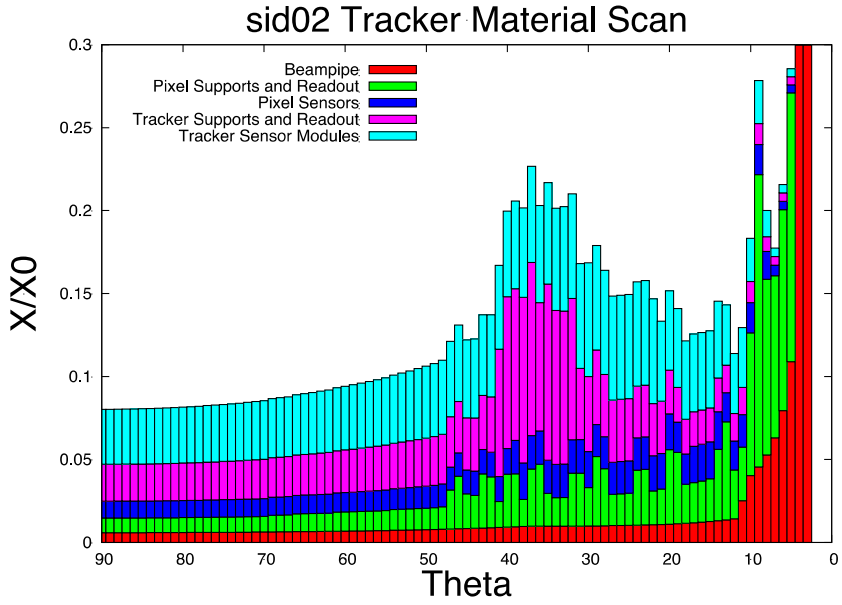
- **Exploring new paths (like 3D) is challenging and requires time**
- FNAL continues/starts new projects facilitating 3D (VICTR, VIPRAM: tracking using Associative Memory, VIPIC2: 10ns time of arrival, charge sharing compensation)

Footnotes / references

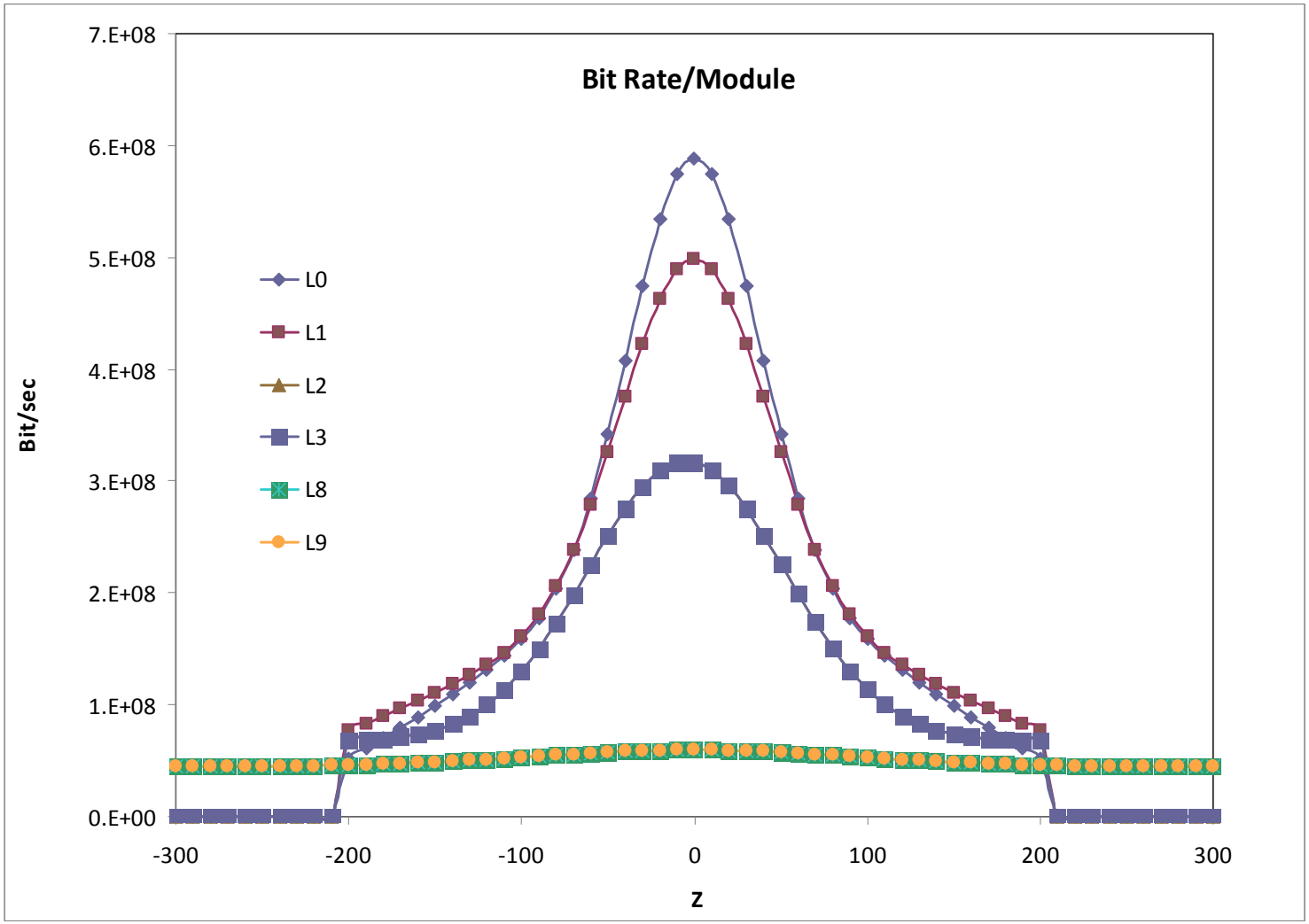
- [1] R.Lipton, ‘Combining the Two 3Ds’, WIT2012 proceedings
- [6] Current cost for 0.18 micron CMOS wafers with through-silicon vias, Yole Development Study
- [7] M. Barbero, Vertex 2011 Workshop, Rust - Austria, June 19th - 24th 2011
- [8] P. Merkel et. al. NIM A 582 771 (2007)

Backup Slides

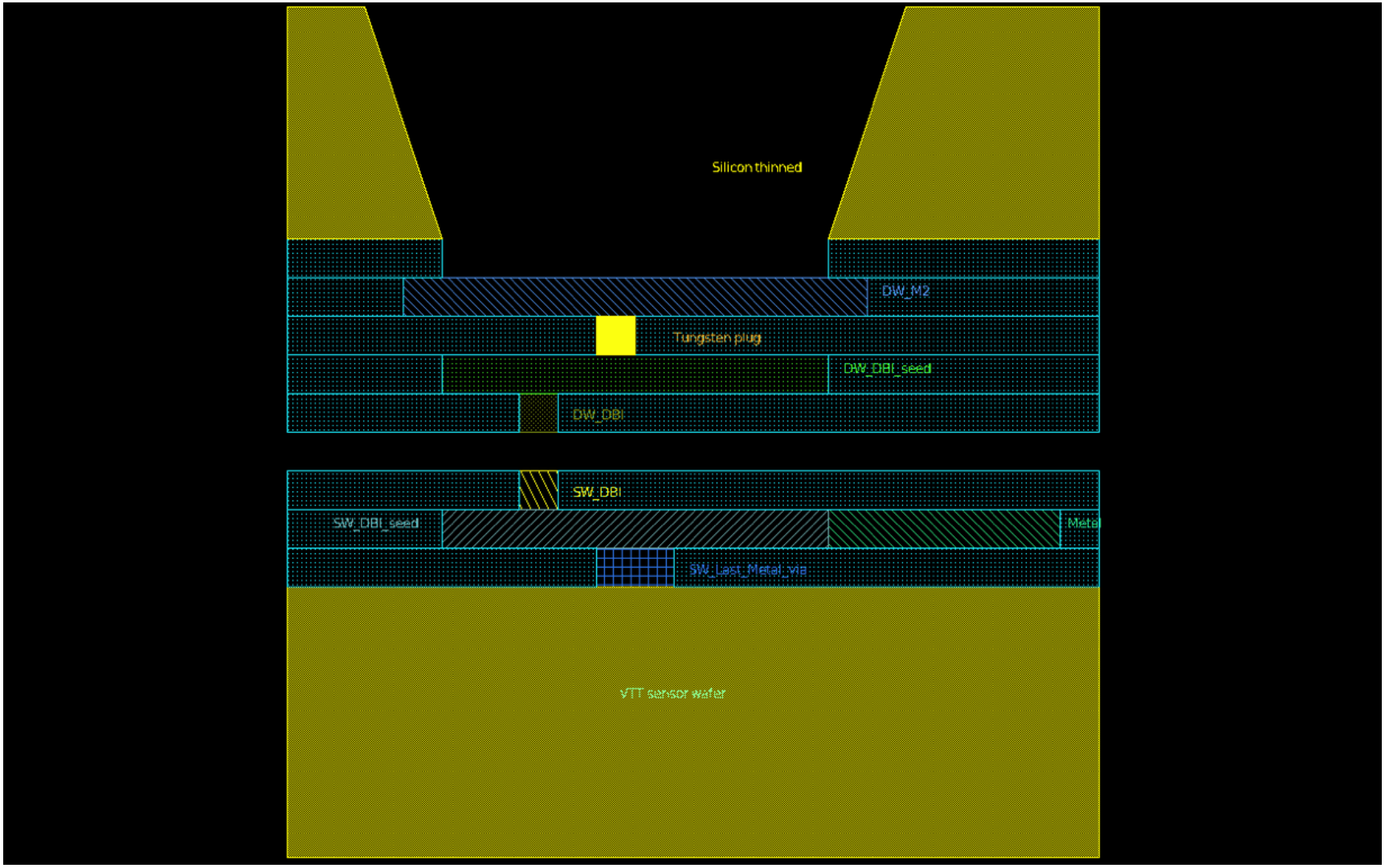
ILC Vertex Sensor Development



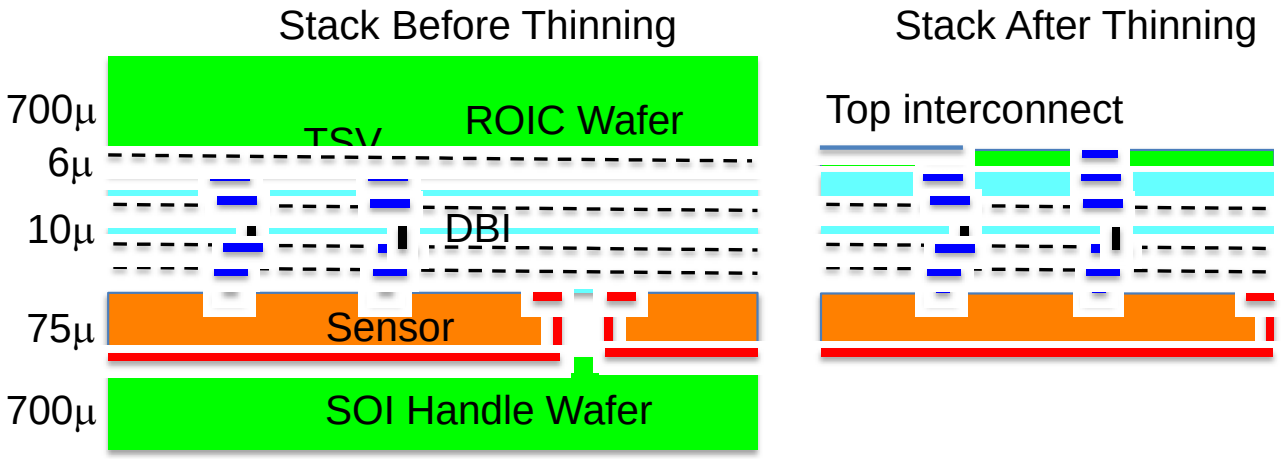
- Our initial work on 3D electronics was motivated by the extraordinary requirements for ILC vertex detectors
  - ~0.1% radiation length/layer
  - time stamping
  - 5 micron resolution
- We realized that emerging IC technologies which offer a high density of electronics, fine pitch interconnects, and wafer thinning could offer a solution to the ILC vertex problem.
- This led to work with:
  - MIT-LL on SOI based 3D ICs
  - Tezzaron on bulk CMOS based 3D ICs
  - Ziptronix on detector/sensor integration with oxide bonding
  - Cornell on thinning and laser annealing

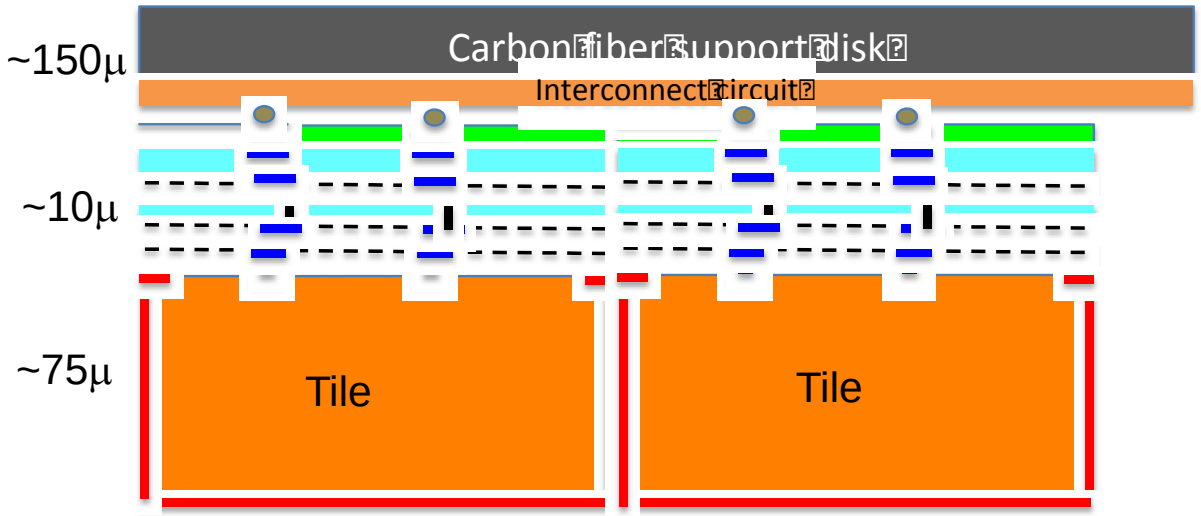

Bit Rate/Module
Bit/sec
7.E+08
6.E+08
5.E+08
4.E+08
3.E+08
2.E+08
1.E+08
0.E+00
L0
L1
L2
L3
L8
L9
-300
-200
-100
0
100
200
300
z

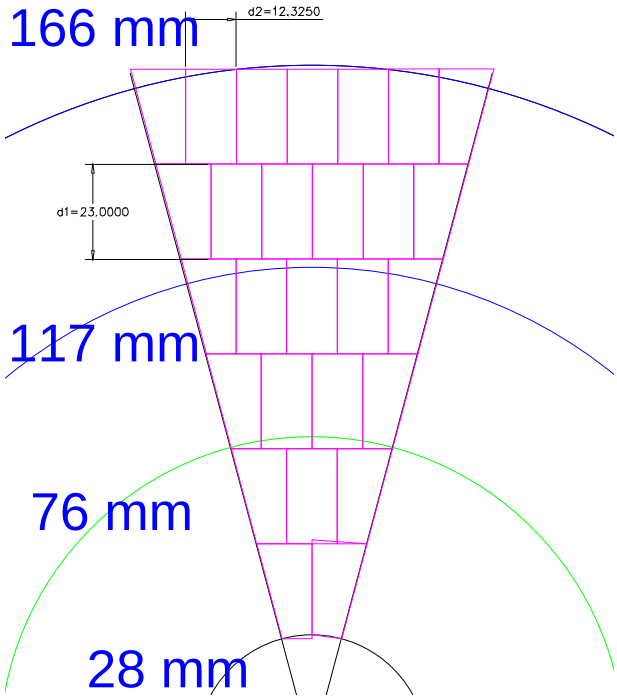
Layer Stack (active edge)



Tiling sensors - ILC forward disk example



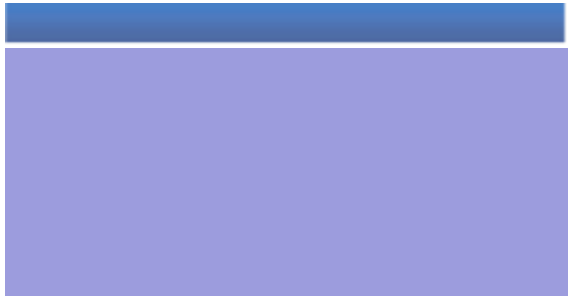




SiD Outer pixel disk rad

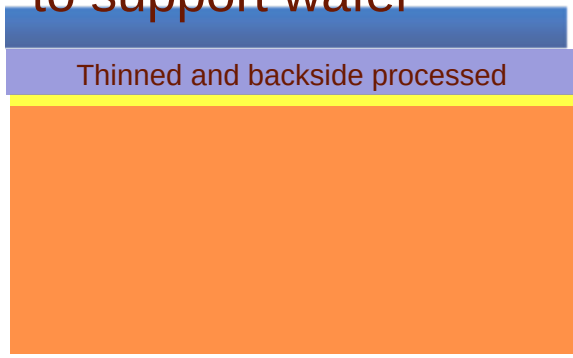
Thinning

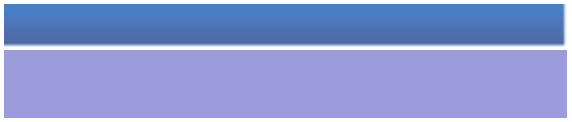
Bulk CMOS/SOI
bonded to sensor



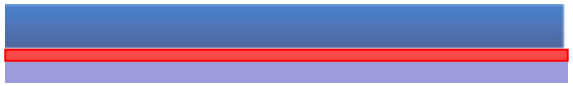
CMOS MAPS
epitaxial layer

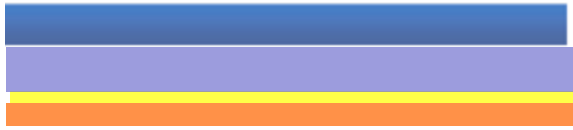
Sensor oxide
bonded
to support wafer



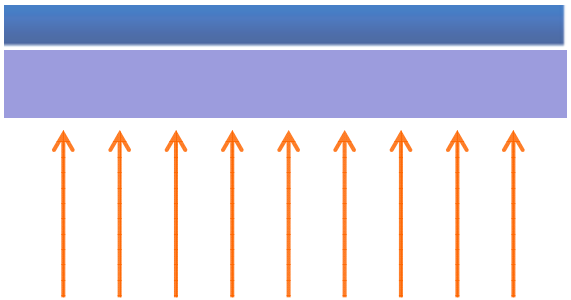


Backgrind



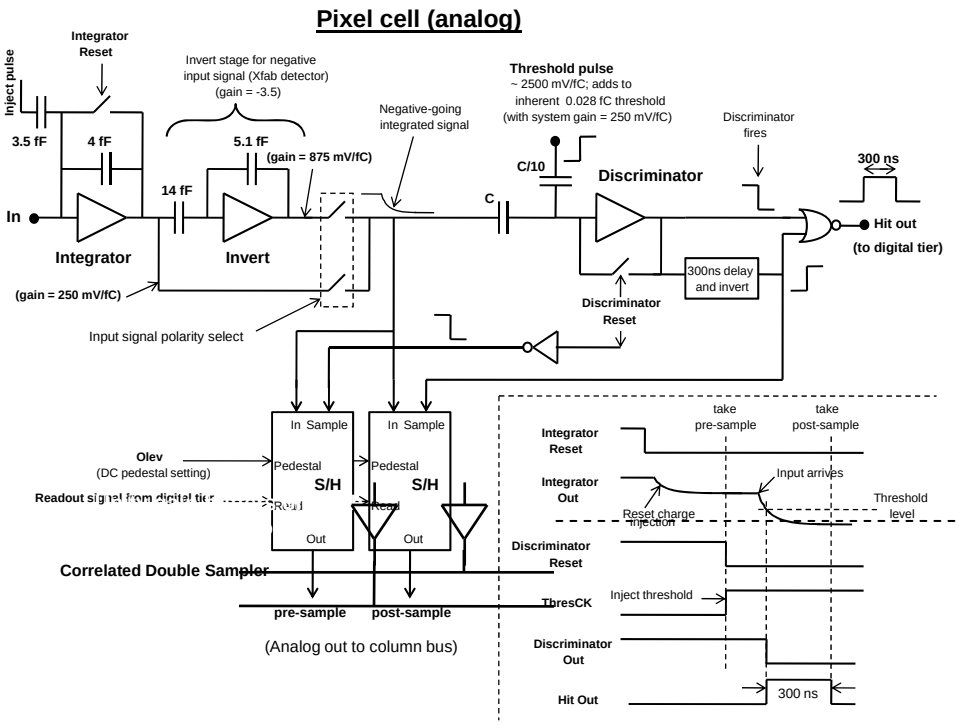


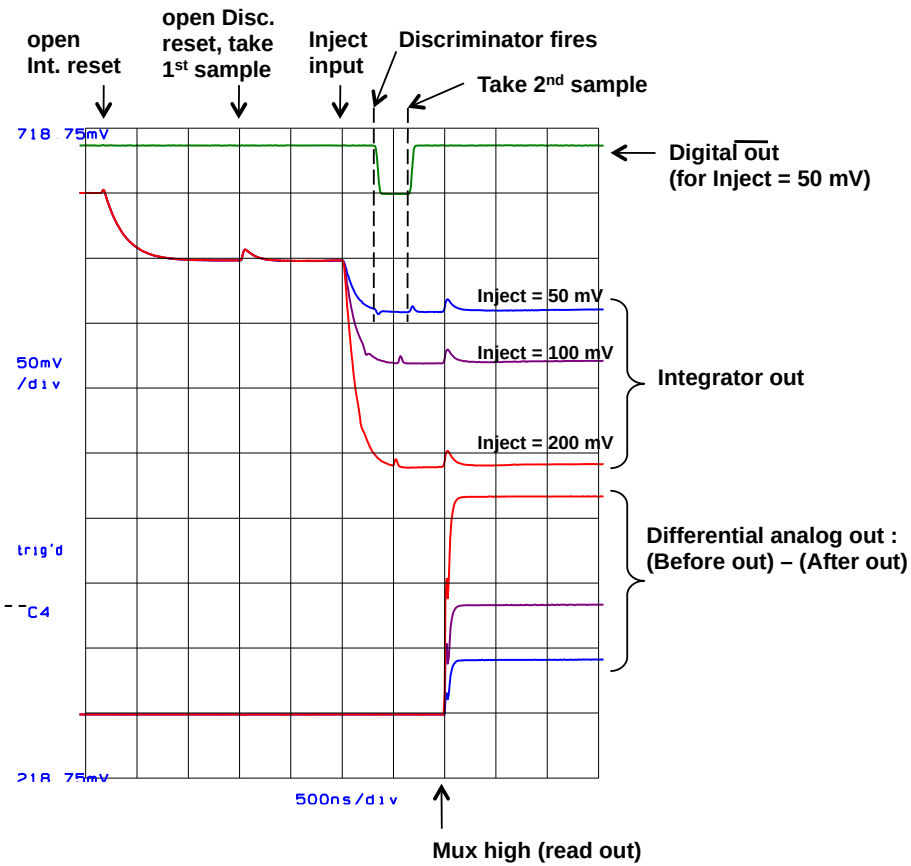
Polish, implant and
Laser anneal



Etch backside silicon

VIP2b (Tezzaron 3D) tests





Measured response with charge injection

Measured noise (DCS)

Csel	Cin added	Cin + Cinstray	Noise at Inv. Out (mV)	Noise at Inv. Out (e)	Noise at Int. Out (mV)	Noise at Int. Out (e)
111	0	12.5 fF	2.26 mV	16 e	0.74 mV	19 e
110	4 fF	17 fF	2.58	18	0.79	20
101	8	21.5	2.84	20	0.82	21
100	12	26	3.11	22	0.87	22
011	16	30.5	3.38	24	0.93	23
000	28	44	4.09	29	1.04	26

Bandwidth not very sensitive to Cin

Bandwidth varies with Cin

8e + 0.5 e/fF

Measured speed

(T = one RC time constant)

Both sample caps on the output

One sample cap on the output

Csel	Cin added	Cin + Cinstray	T_{before} Int. out	T_{after} Int. out	T_{before} Inv. out	T_{after} Inv. out
111	0	12.5 fF	115 ns	73 ns	135 ns	65 ns
000	28 fF	44 fF	215 ns	125 ns	140 ns	80 ns

At integrator out; speed varies due to varying Csample <u>and</u> varying Cin.

At invert stage out; varying Cin has much less effect on bandwidth.

Measured speed is somewhat slower than simulated – probably due to somewhat lower gm and ?