Contribution ID: **70** Type: **ORAL**

Towards third generation pixel readout chips

Wednesday, 5 September 2012 08:30 (30 minutes)

We present concepts and prototyping results towards a third generation pixel readout chip. We consider the 130nm feature size FE-I4 chip, in production for the ATLAS IBL upgrade, to be a second generation chip. A third generation chip would have to go significantly further. A possible direction is to make the IC so generic that different experiments can configure it to meet significantly different requirements, without the need for everybody to develop their own ASIC. In terms of target technology, a demonstrator 500-pixel matrix containing analog front ends only (no complex functionality), was designed and fabricated in 65nm CMOS and irradiated with protons in Dec. 2011 and May 2012. We present the design and measurement results.

Primary author: GARCIA-SCIVERES, Maurice (Lawrence Berkeley National Lab. (US))

Co-authors: Dr MEKKAOUI, Abderrezak (LBNL); GNANI, Dario (LBNL); TBD, TBD (TBD)

Presenter: GARCIA-SCIVERES, Maurice (Lawrence Berkeley National Lab. (US))

Session Classification: Session5

Track Classification: Front end electronics and readout - Readout chip developments