Monolithic Active pixel Matrix with Binary Counters (MAMBO)

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Presentation outline

• Nested well structure
• MAMBO pixel electronics
• Test results
• Conclusions

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- ASIC submission was covered by US-Japan Collaboration funds in collaboration with KEK, Japan
Characteristics of Buried P well (BPW)

Si (n-type) (40keV @ 1e12 cm²)

Capacitance between Interference and Pwell contact (fF/μm)

Capacitance between Interference metal and pwell contact vs. Width of BPW

Charge at Pwell vs Width of BPW

V_dp= .5  V_bias= 0,1,2

Charge density at Pwella1 (fC/μm)

Capacitance between pwell and substrate vs. width of BPW

Charge at Pwell vs Width of BPW

C_B Vdp=.5v  C_B Vdp= 2v  C_B Vdp=10v

Capacitance between pwell and substrate (fF/μm)
Characteristics of Nested Well structure

• $C_N$: Capacitance between interference metal and n well contact increases with increasing BNW dose, but reduces by increasing BNW implantation energy.

• $C_P$: Capacitance between interference metal and p well contact decreases with increasing BNW dose and by increasing BNW implantation energy.

• $C_P$: lower for nested well compared to just BPW

![Graphs showing capacitance variations](image-url)
SOI technology for detectors

- Electric potential under any circuitry may be kept constant or change very little only by voltage from integrated charge.
- Gives increased C-to-V node capacitance.
- Works with charge integrating pixels (3T-like), gain may be nonlinear.
- Charge injections due to electronics activity may be canceled out by sequential readout with exactly repeated patterns for control signals and CDS.
- Full isolation of the electronics and the detector charge collection node.
- Electric potential under any circuitry is kept constant (AC ground).
- Allows designs with amplification stages and virtual ground (CSA).
- Removes parasitics feedbacks and instabilities.
- Unfortunately increases input capacitance of CSA.
**Purpose of the nested well structure**

**Shielding:**
- Tripple role of shielding between the SOI electronics and detector layer:
  - to avoid back-gating in transistors (DC potential underneath the BOX shifts threshold of transistors),
  - to avoid injection of parasitic charges from the SOI electronics to detector,
  - to avoid strong electric field in BOX that results in accelerated radiation damage.

This well separates digital circuits from sensor substrate and prevents back gating effects.

This well collects the charge carriers.

Developed at Fermilab with KEK and OKI/Lapis.

SILVACO process simulation.
MAMBO = Monolithic Active Pixel Matrix with Binary Counters

MAMBO IV & V

Pixel design with window discriminator and per pixel counter

Integrating CSA w/ p-z network, shaping filter CR-RC² with $\tau_p=200\text{ns}$; gain=\~100 $\mu\text{V/e}^-$, ripple counter reconfigurable into shift register, DACs for threshold adjustment, control logic for testability

SOI LAPIS/OKI Semiconductor 0.2μm process
- Single pixel under test
- Selectable modes for analysis & characterization of various blocks
  - Analogue test mode; analyses: noise, linearity and Dynamic Range
  - Counter test mode
  - DAC trimming mode
  - Pixel disable mode
  - Normal Operation mode

MAMBO V 50×52 pixels-testability at pixel level for statistics analyzes
Preamplifier

• Regulated Cascode with extra current boosting to increase $gm$ of input transistor
• Leakage current compensation
• 1.7fF I/P test capacitance

Cfs=14fF, Cc=140fF
Protection diode at Input
Shaper and Baseline Restorer

- CR-RC$^2$ shaper
- Regulated cascode to match preamplifier
- Shaping time = 200ns

Clamping diodes
Feedback capacitance
Feedback resistance

Regulated Cascode
With gain boosting

Baseline restorer
Comparator

• Hysteresis Comparator

• Connected to \textit{in\_Vref} during normal operation

OR

• Connected to baseline for trimming

OR

• Connected to gnd! when disabled
Double Discriminator Logic

- Output of the Lower Threshold comparator behaves as a clock
- Output of the Upper Threshold comparator behaves as a Reset
- When both comparators fire the hit is not counted
Counter /Shift Register

- 12 bit ripple counter
- Count switch disconnects counter from comparator while shifting
- CK_READ is external clock used for shifting data

s2 = Count
s1 = Shift
Nested well conceptual view

Pixel Layout

105 μm
MAMBO: TEST RESULTS
Test Setup
MAMBO V nested BNW/BPW: C-V & $1/C^2 - V$ plots: HR1 substrate 325µm

- Voltage breakdown around 130V
- Leakage current is 3 times larger compared to previous wafer (FZ)
MAMBO V nested BNW/BPW:
C-V & 1/C²-V plots: HR1 substrate < 1kΩ area (5.3 x 5.3 mm²)

- Voltage breakdown occurs before full depletion is achieved
- Doping levels of substrate is not adequate (higher resistivity is desired)
Example of MAMBO IV results:

no shift of PMOS & NMOS transistor $I_{DS}/V_{GS}$ in nested wells at back-gate biases ranging from 0 to 100V

For an NMOS transistor of size 41x(0.64µm/ 0.8µm) and PMOS transistor of size 41x(2µm/0.5µm) the plots indicate that there is no threshold voltage shifts on increasing the voltage on the die pad ($V_{DP}$) from 0-100V

whereas on increasing the voltage of BNW ($V_{BNW}$) from 1-5V threshold voltage shifts of approximately 100mV for PMOS and 150mV for NMOS transistors is observed.
Trimming DAC threshold scans

Detector bias at 2V

Detector bias at 20V

- For DAC current settings of 8nA to 64nA, with average non-linear LSB of 12mV to 27mV, corresponds to a voltage spread of ±90mV to ±200mV respectively
- Digital circuit response independent of detector bias
DAC Scans: Count vs. Threshold (VthL)

Varying Counter voltage

- Baseline set at 400mV
- VthL scanned from 350mV to 475mV

Varying DAC current

- Baseline set at 400mV
- VthL scanned from 350mV to 475mV
IMAGE with Cd$^{109}$ source (22keV)

(1.9mm x 1.9mm) square mask  without mask
BNW resistance simulation

- Shallow and lower concentration of BNW produces higher resistance across the N well contacts.
- The resistance is independent of the Die pad voltage.

R_N vs V_dp; V_bnw=.5

Resistivity between P1,P2 electrodes (kohm um)

Resistivity between N1,N2 electrodes (kohms um)

BNW Energy (keV)

<table>
<thead>
<tr>
<th>BNW dose, energy</th>
<th>BNW Energy (keV)</th>
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</thead>
<tbody>
<tr>
<td>1.00E+12</td>
<td>220keV</td>
</tr>
<tr>
<td>5.00E+12</td>
<td>300keV</td>
</tr>
<tr>
<td>1.00E+13</td>
<td>380keV</td>
</tr>
</tbody>
</table>

BNW Varies

Interference

Substrate

Pwella1 Nwella1 Nwella2 Pwella2 BPW BP1 BP2
IMAGE with Cd\textsuperscript{109} source (22keV) with DiePad at 9V

(1.9mm x 1.9mm) square mask

- Analogue oscillations when Diepad voltage is increased beyond 3V
- Hypothesis: highly resistive BNW, requires more contacts
- Preamplifier gain reduced by operating front-end below 1V
- Image obtained with detector biased at 9V
Conclusions and Future Work

- Extensions made to the process closer to obtain a fully functional detector with all satisfactory parameters

- Good effective collaboration with Lapis semiconductor

- First counting pixel SOI ASIC operated successfully with shielding of sensor from electronics

- Include more BNW contacts in the pixel layout to compensate for BNW resistivity.

- Confirm and stabilize access to HR / FZ Si material

- Optimize nested wells BNW-BPW to decrease input capacitance or implement alternative shielding method

- Provide back processing (implantation and annealing); limit depth of implantation to allow entrance window for autoradiography at low energy of particle (w or w/o back Al)

- Optimize thickness of wafers for actual application 50-100μm for tracking 500 - 700μm or more for X-ray imaging
Questions?