Monolithic **A**ctive pixel **M**atrix with **B**inary c**O**unters (MAMBO)

Farah Khalid, Gregory Deptuch, Alpana Shenai, Scott Holm, Ron Lipton

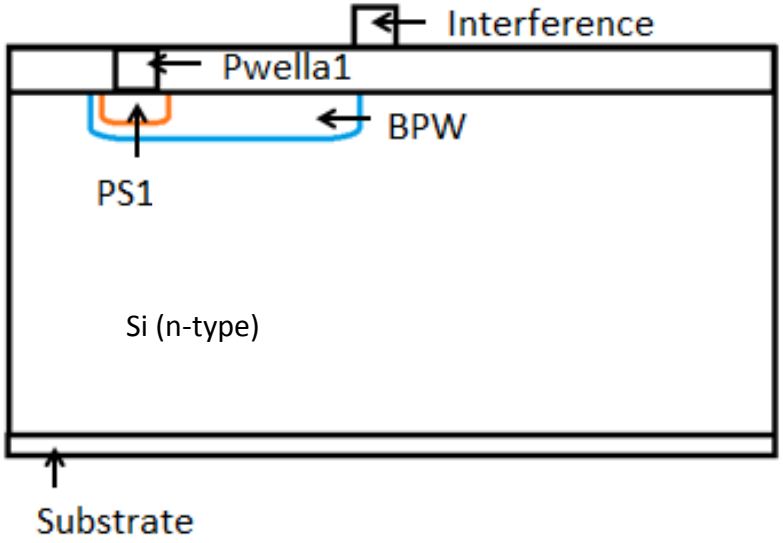
Fermi National Accelerator Laboratory

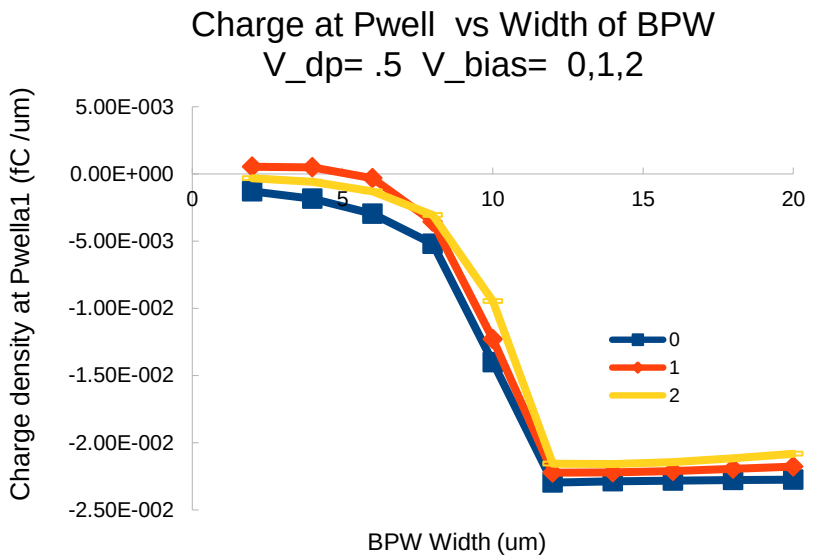
Presentation outline

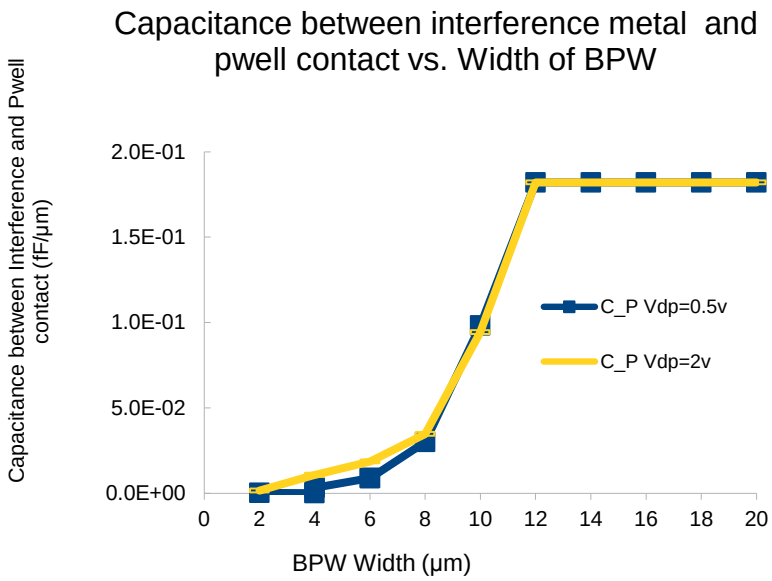
- Nested well structure
- MAMBO pixel electronics
- Test results
- Conclusions

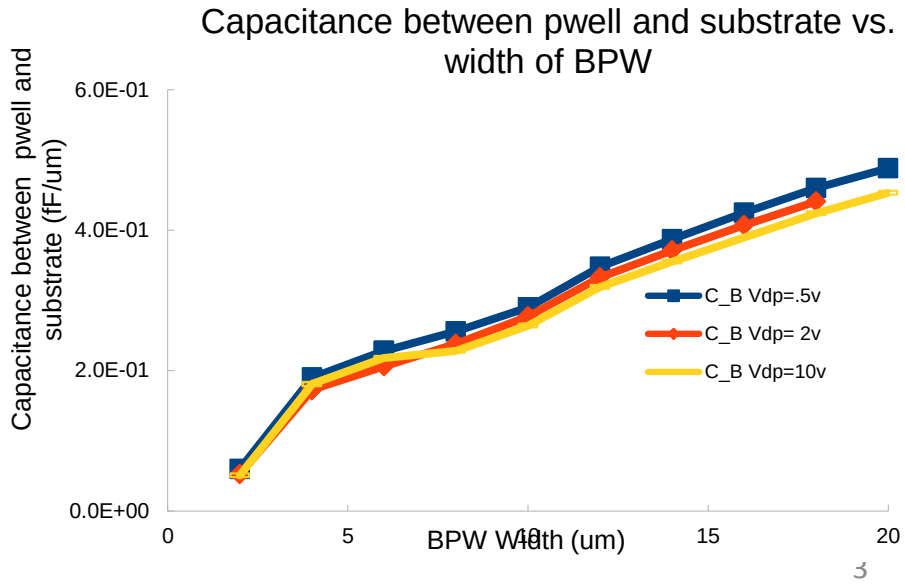
- Fermi National Accelerator Laboratory is operated by Fermi Research Alliance, LLC under Contract DE-AC02-07CH11359 with the U.S. Department of Energy.
- ASIC submission was covered by US-Japan Collaboration funds in collaboration with KEK, Japan

Characteristics of Buried P well (BPW)

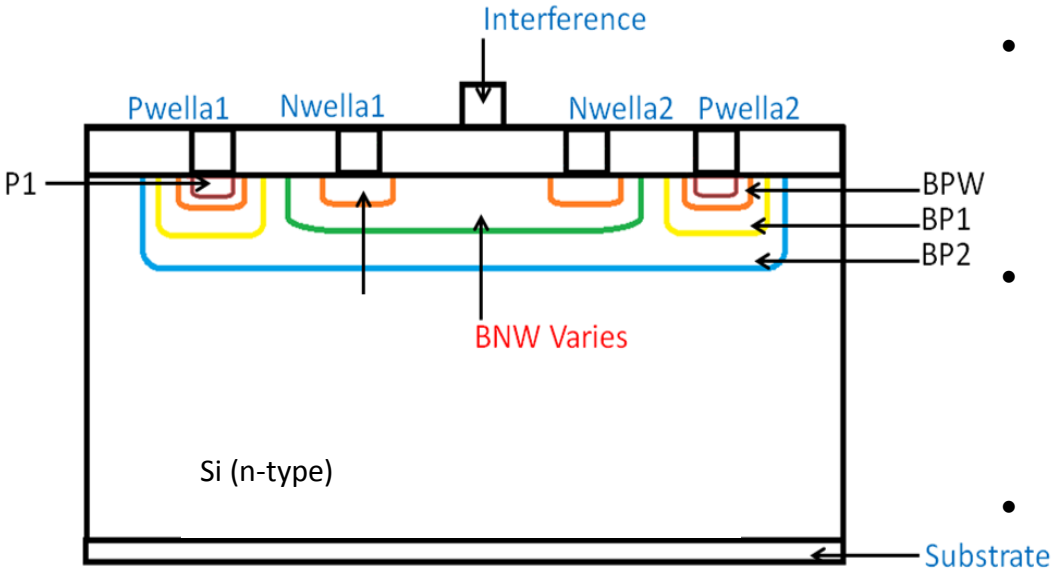




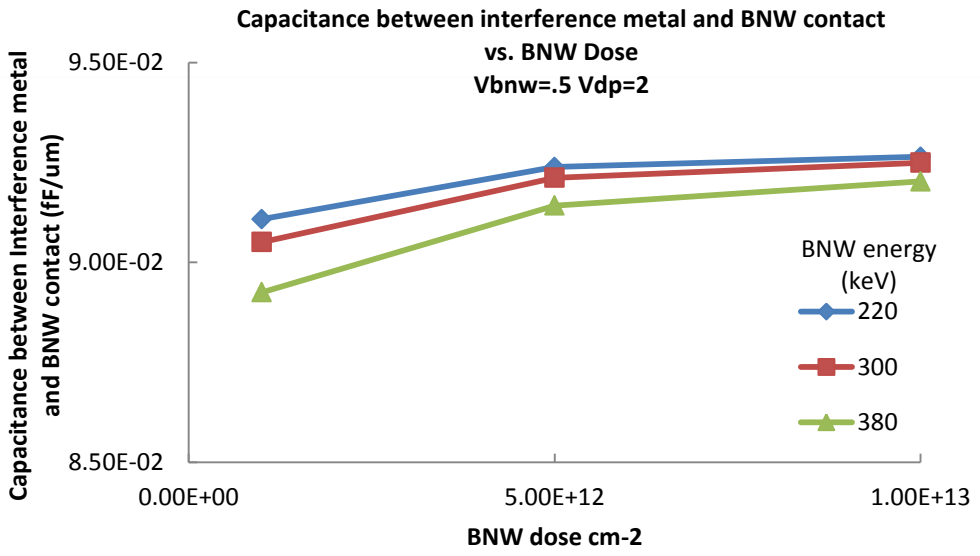


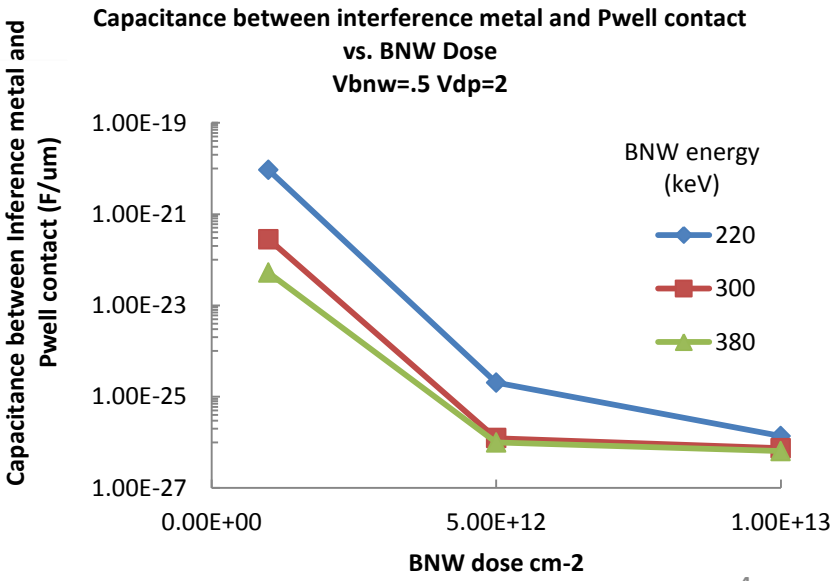


Characteristics of Nested Well structure

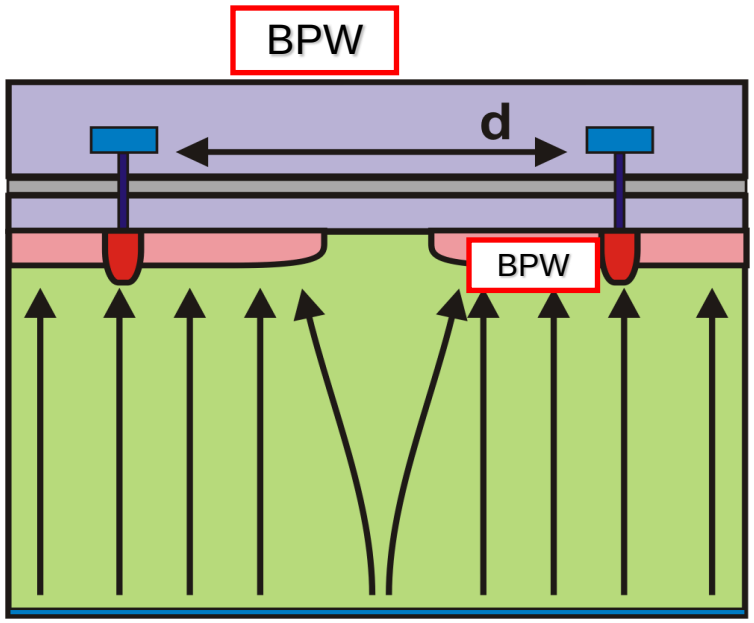


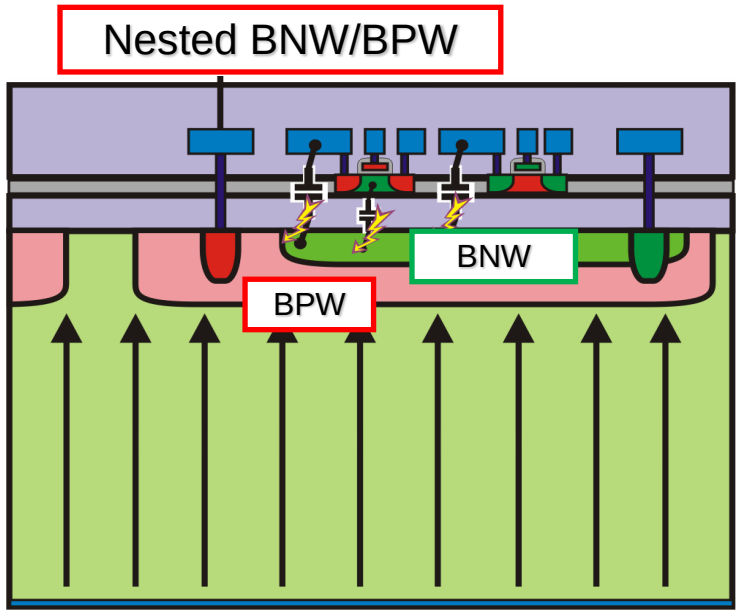
- C_N: Capacitance between interference metal and n well contact increases with increasing BNW dose, but reduces by increasing BNW implantation energy.
- C_P: Capacitance between interference metal and p well contact decreases with increasing BNW dose and by increasing BNW implantation energy.
- C_P: lower for nested well compared to just BPW





SOI technology for detectors





- electric potential under any circuitry may be kept constant or change very little only by voltage from integrated charge
- gives increased C-to-V node capacitance
- works with charge integrating pixels (3T-like), gain may be nonlinear,
- charge injections due to electronics activity may be cancel out by sequential readout with exactly repeated patterns for control signals and CDS

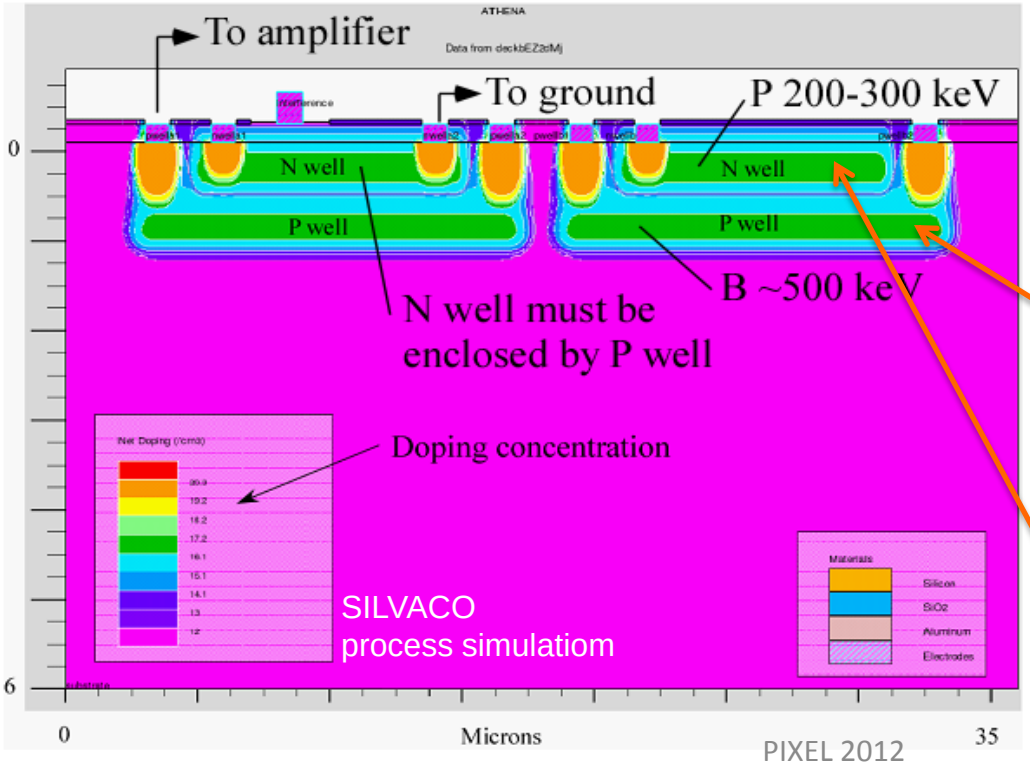
- full isolation of the electronics and the detector charge collection node,
- electric potential under any circuitry is kept constant (AC ground)
- allows designs with amplification stages and virtual ground (CSA)
- Removes parasitics feedbacks and instabilities,
- Unfortunately increases input capacitance of CSA

Purpose of the nested well structure

Shielding:

– Tripple role of shielding between the SOI electronics and detector layer:

- to avoid back-gating in transistors (DC potential underneath the BOX shifts threshold of transistors),
- to avoid injection of parasitic charges from the SOI electronics to detector,
- to avoid strong electric field in BOX that results in accelerated radiation damage.



Developed at Fermilab with KEK and OKI/Lapis

This well collects the charge carriers

This well separates digital circuits from sensor substrate and prevents back gating effects

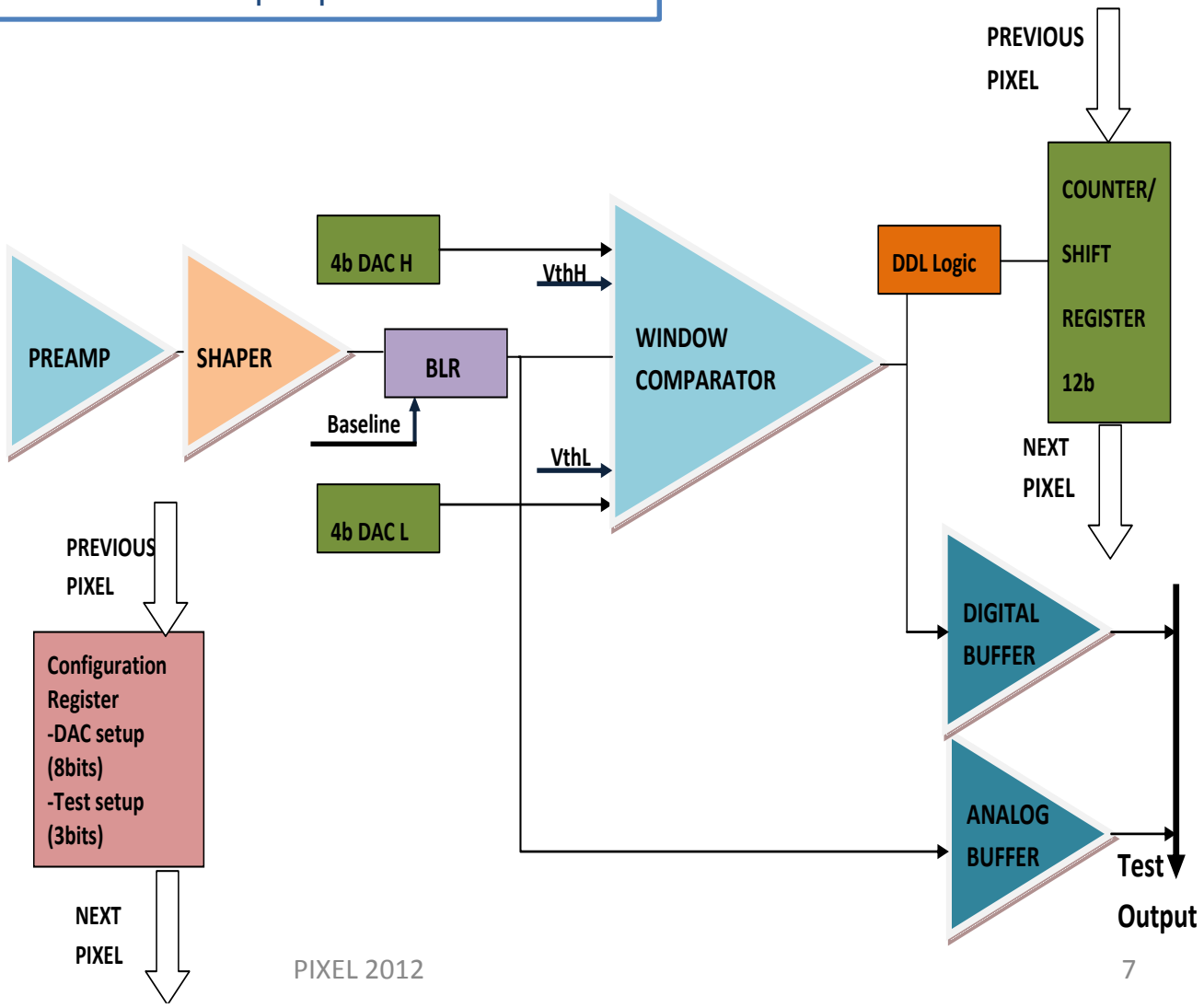
MAMBO = Monolithic Active Pixel Matrix with Binary Counters

MAMBO IV & V

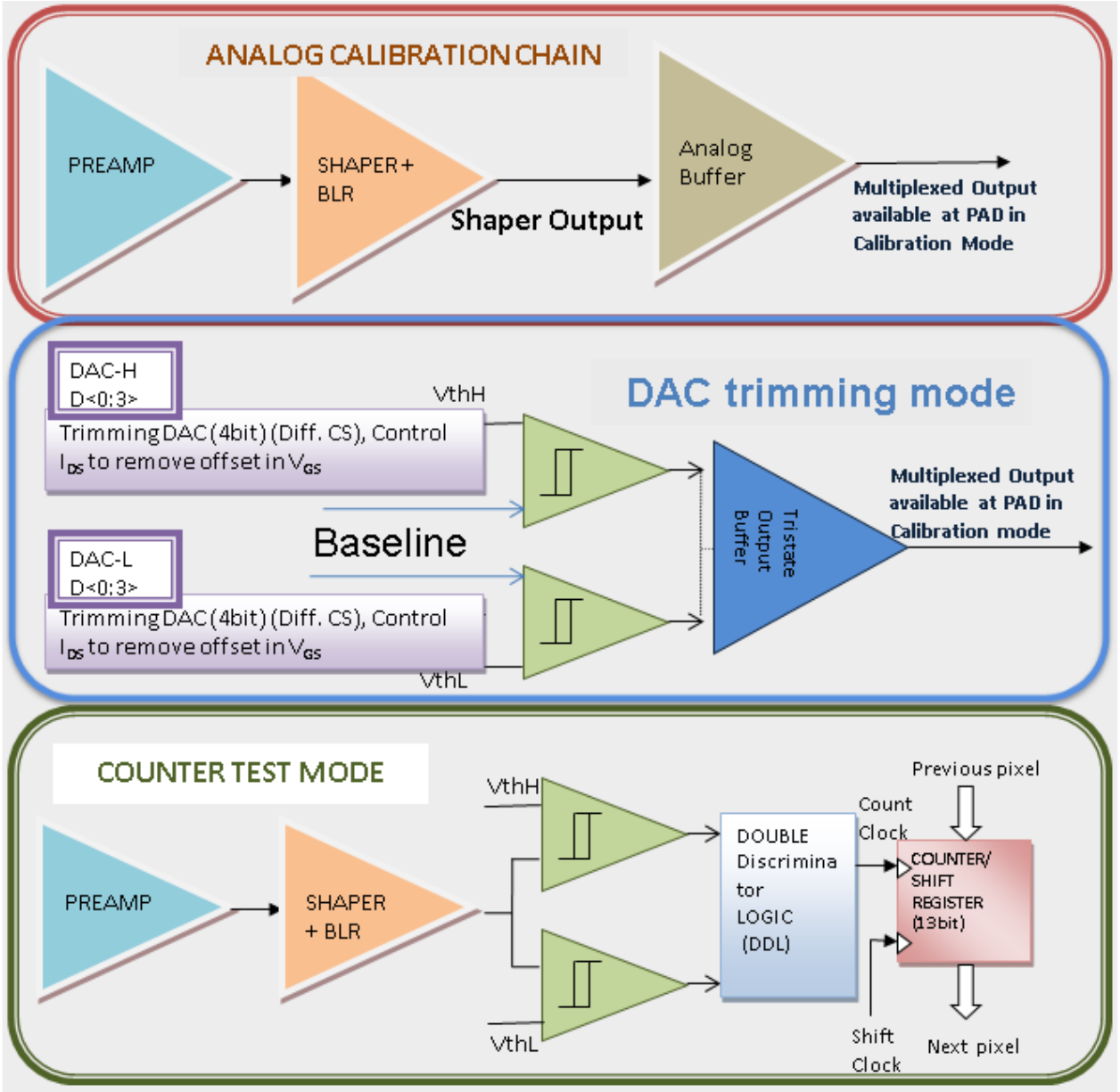
pixel design with window discriminator and per pixel counter

integrating CSA w/ p-z network,
shaping filter CR-RC^2
with τ_p=200ns;
gain=~100 μV/e$^-$,
ripple counter
reconfigurable
into shift register,
DACs for threshold adjustment,
control logic for testability

SOI LAPIS/OKI Semiconductor 0.2μm process



MAMBO test modes

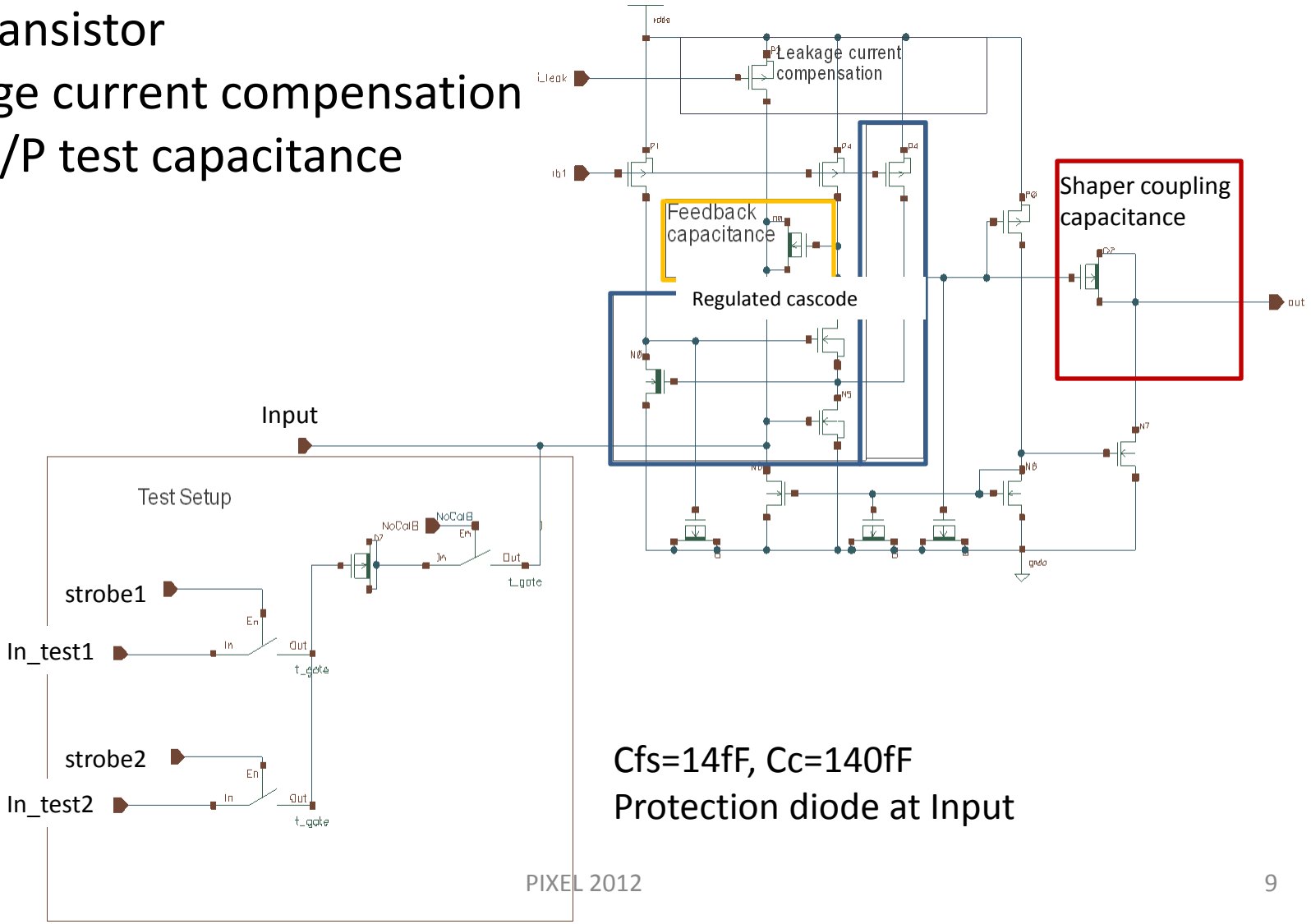


- Single pixel under test
- Selectable modes for analysis & characterization of various blocks
  - Analogue test mode; analyses: noise, linearity and Dynamic Range
  - Counter test mode
  - DAC trimming mode
  - Pixel disable mode
  - Normal Operation mode

MAMBO V 50×52 pixels- testability at pixel level for statistics analyzes

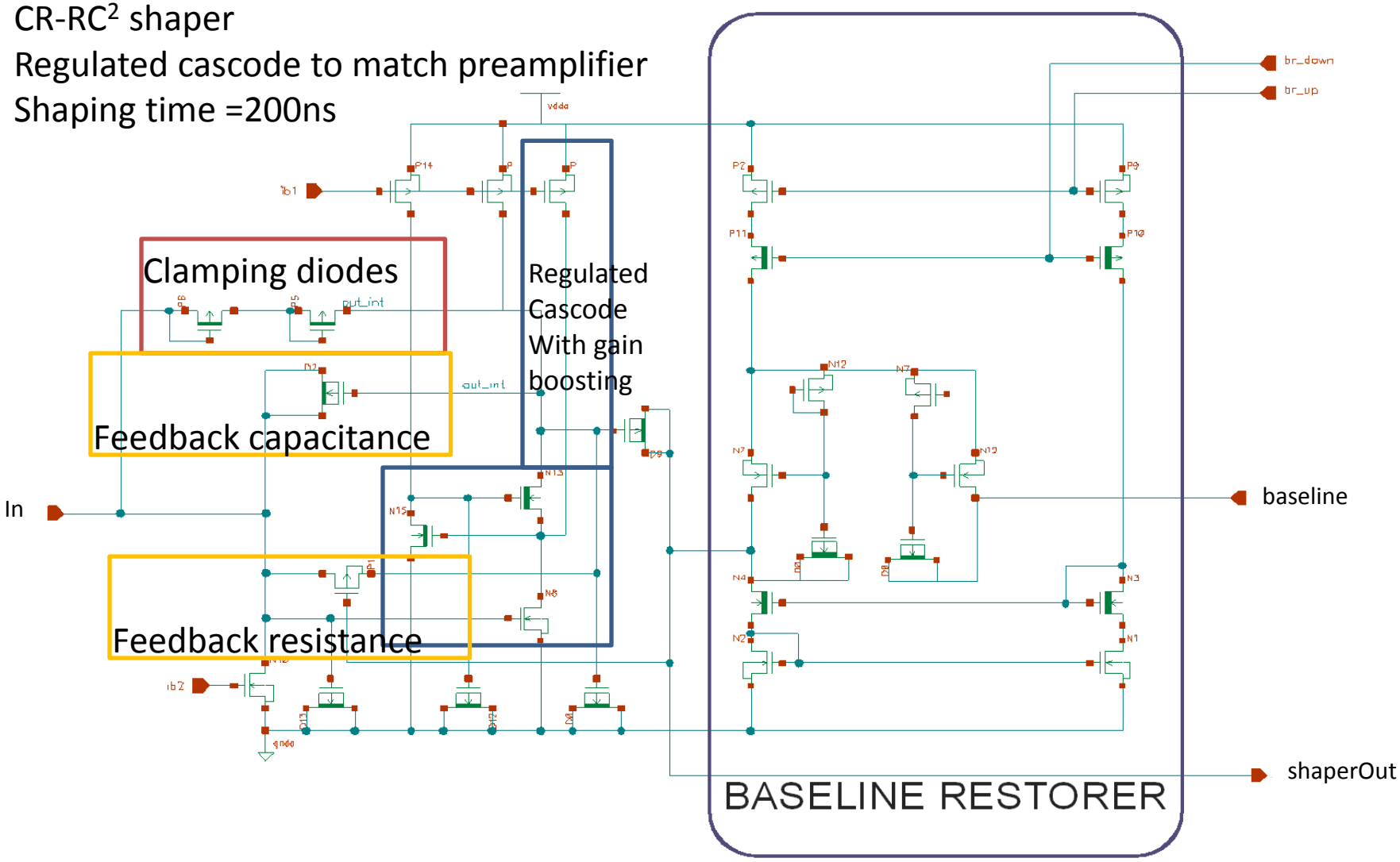
Preamplifier

- Regulated Cascode with extra current boosting to increase gm of input transistor
- Leakage current compensation
- 1.7fF I/P test capacitance



Shaper and Baseline Restorer

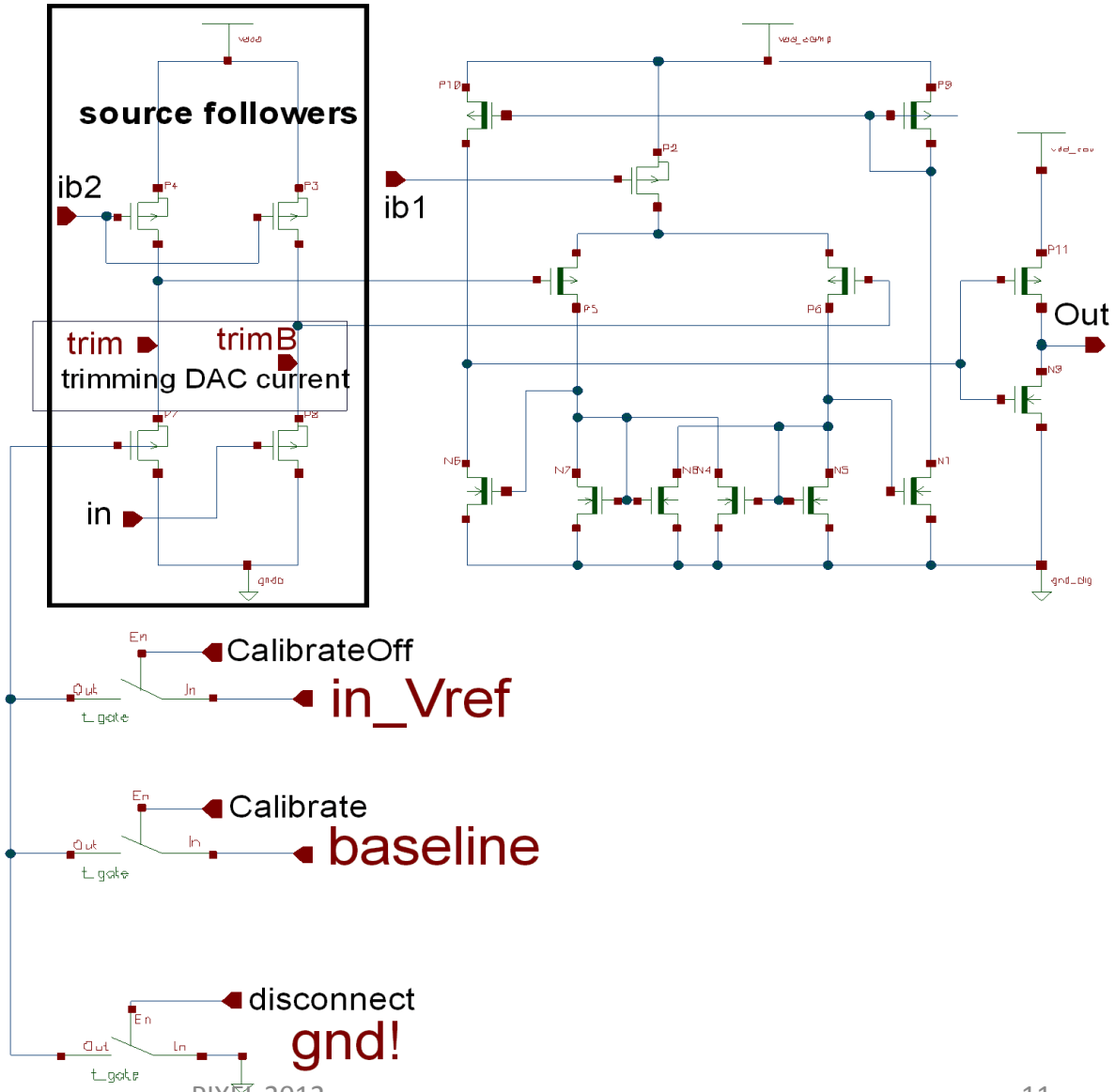
- CR-RC^2 shaper
- Regulated cascode to match preamplifier
- Shaping time =200ns



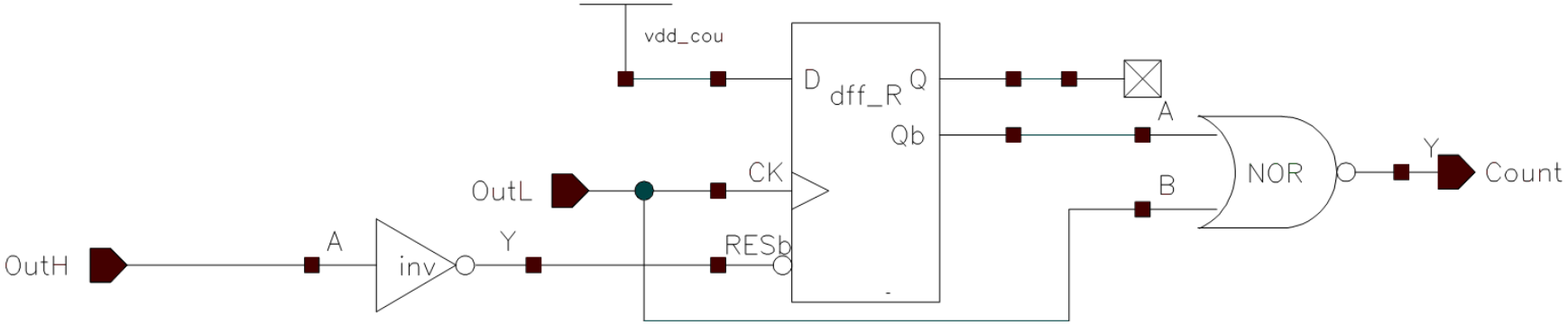
Comparator

- Hysteresis Comparator

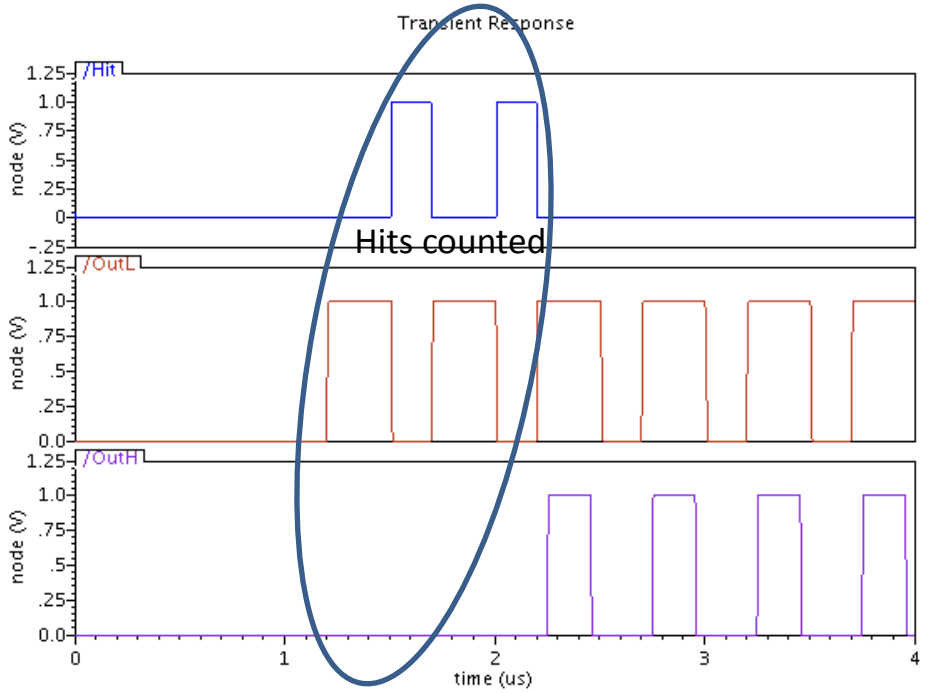
- Connected to in_Vref during normal operation
OR
- Connected to baseline for trimming
OR
- Connected to gnd! when disabled



Double Discriminator Logic

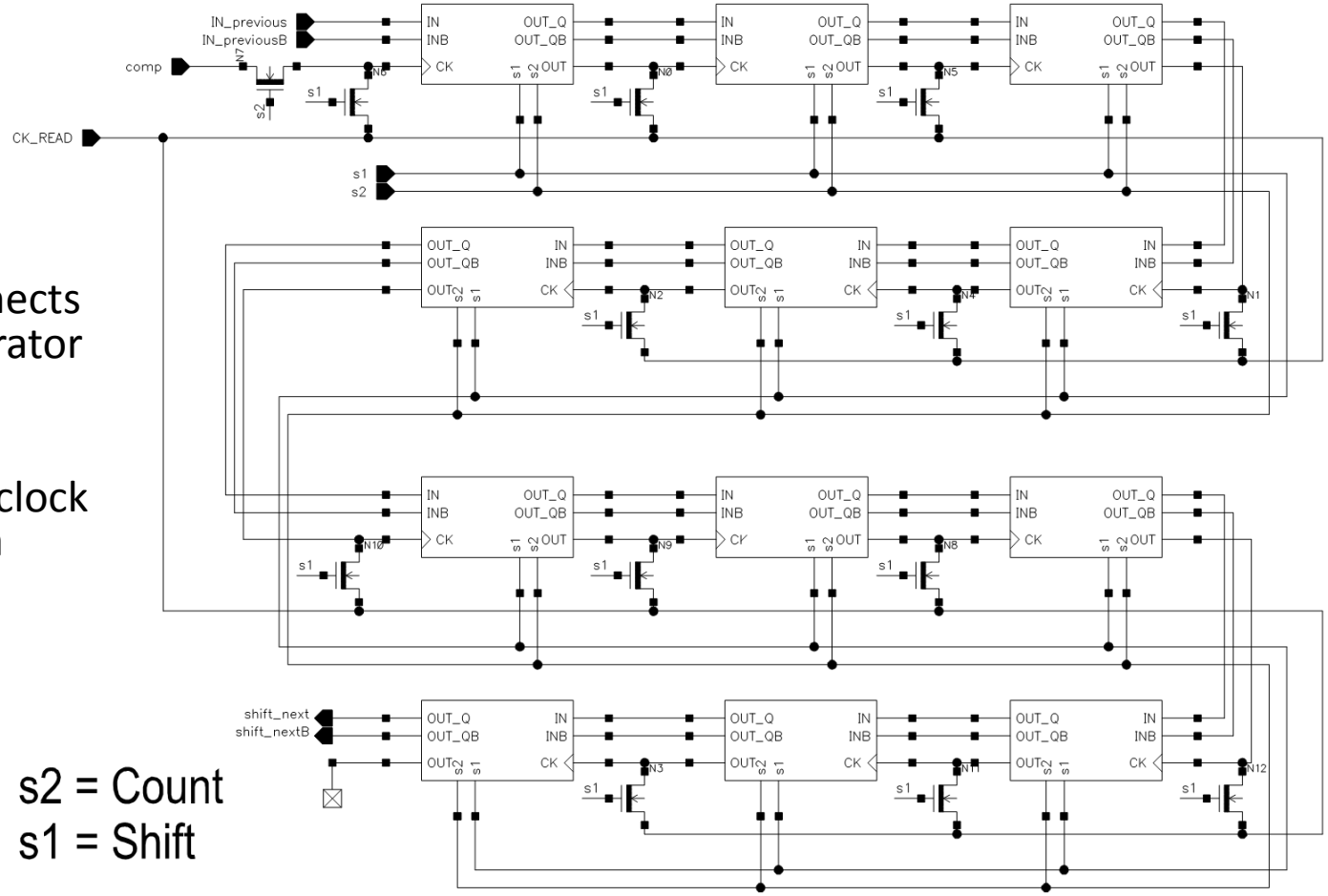


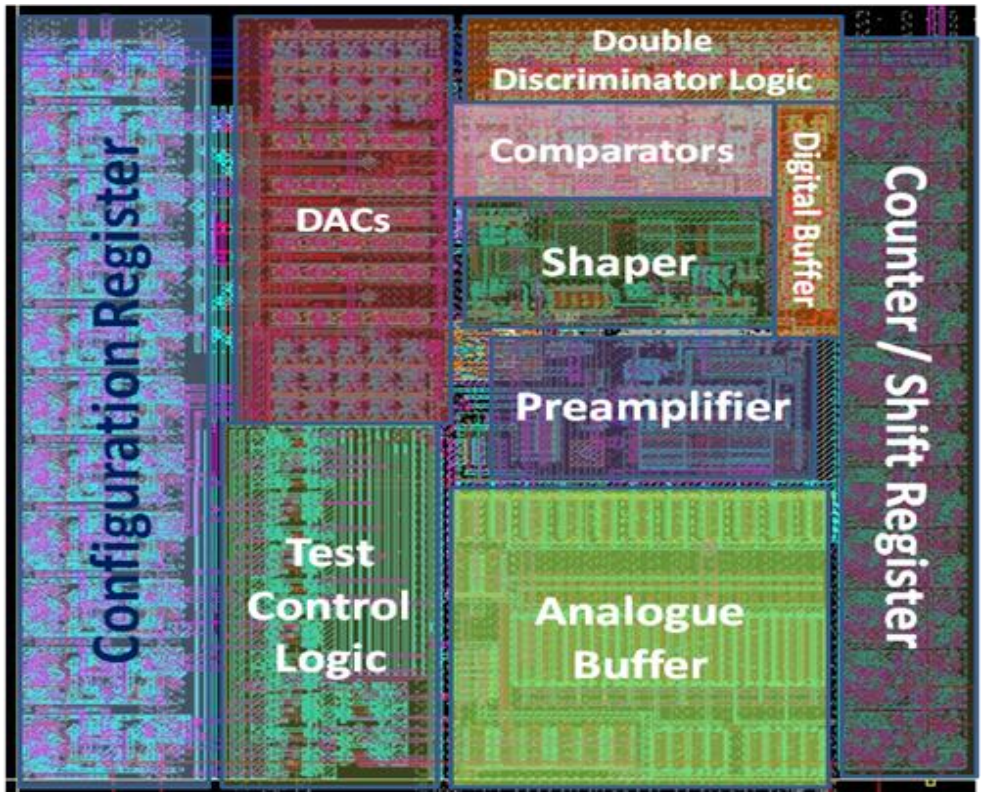
- Output of the Lower Threshold comparator behaves as a clock
- Output of the Upper Threshold comparator behaves as a Reset
- When both comparators fire the hit is not counted



Counter /Shift Register

- 12 bit ripple counter
- Count switch disconnects counter from comparator while shifting
- CK_READ is external clock used for shifting data

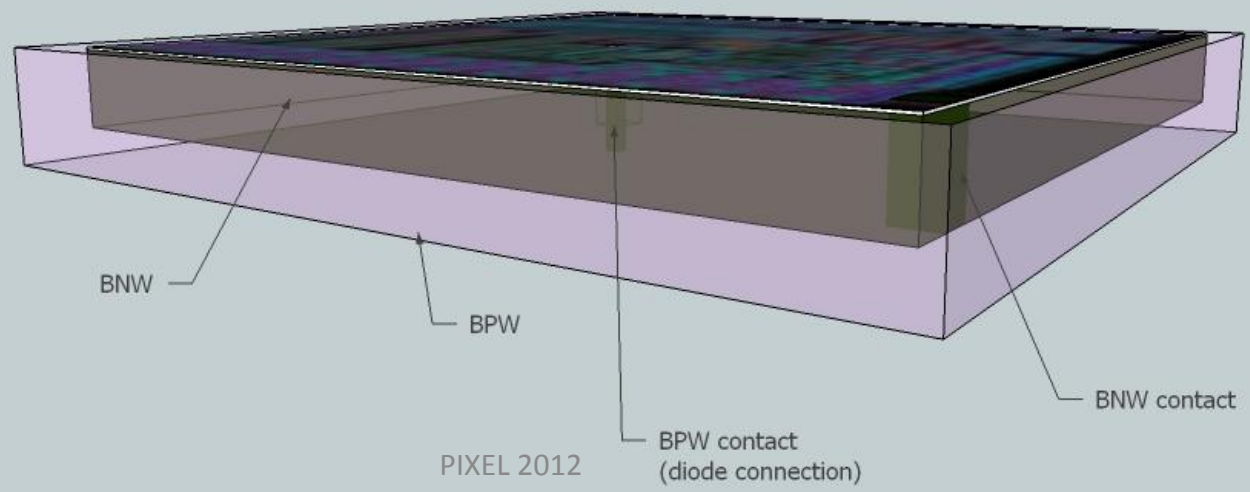




105 μm

Nested well conceptual view

Pixel Layout

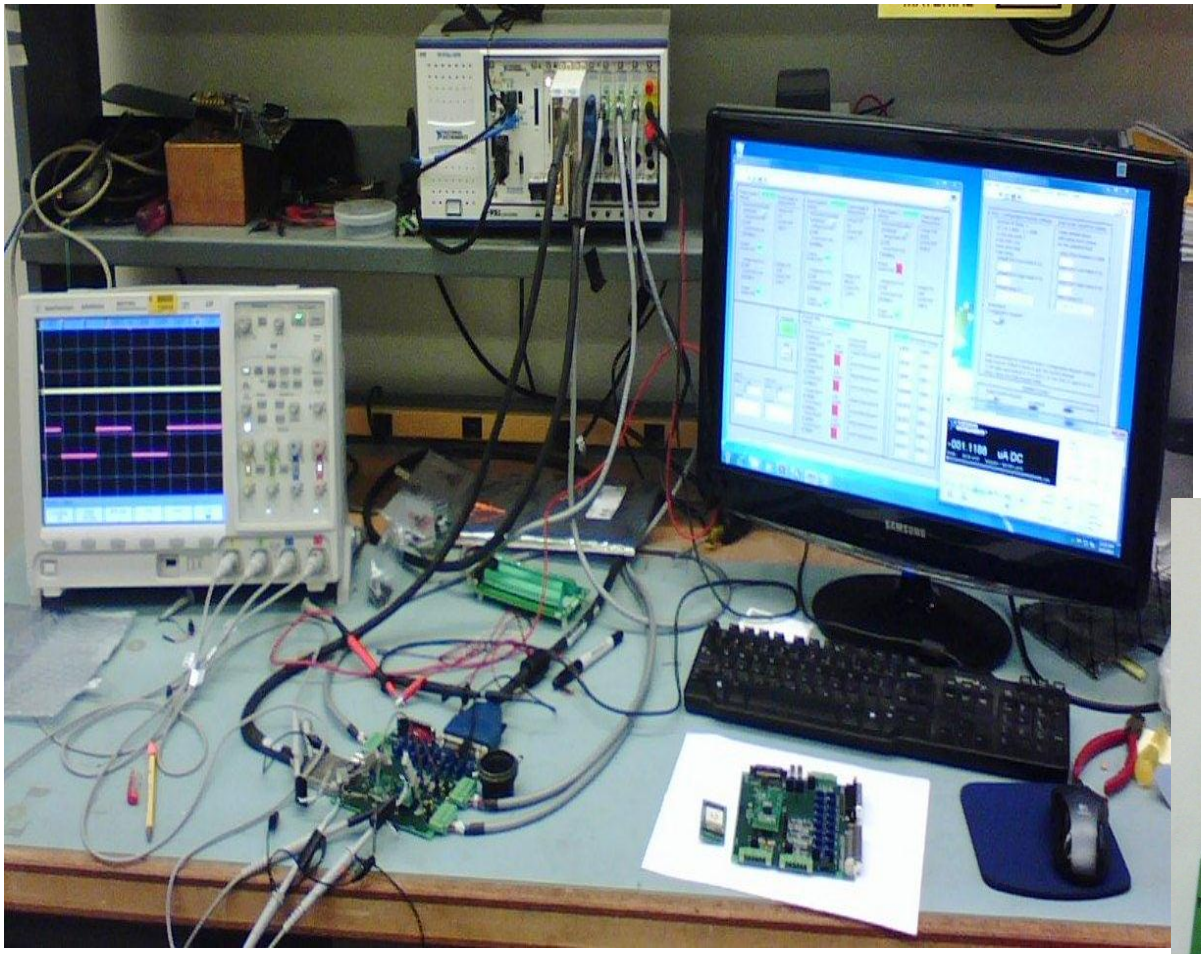


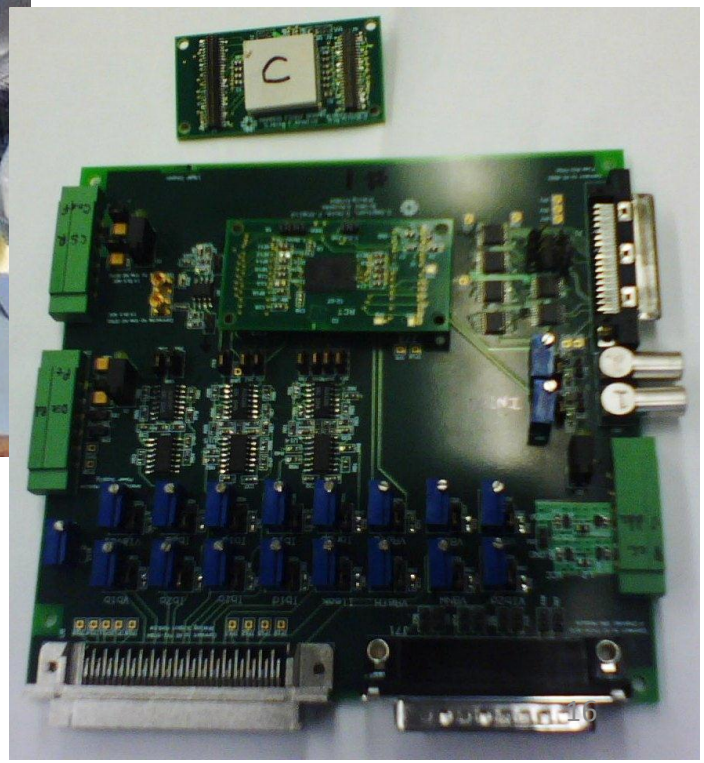
Fermilab

MAMBO: TEST RESULTS

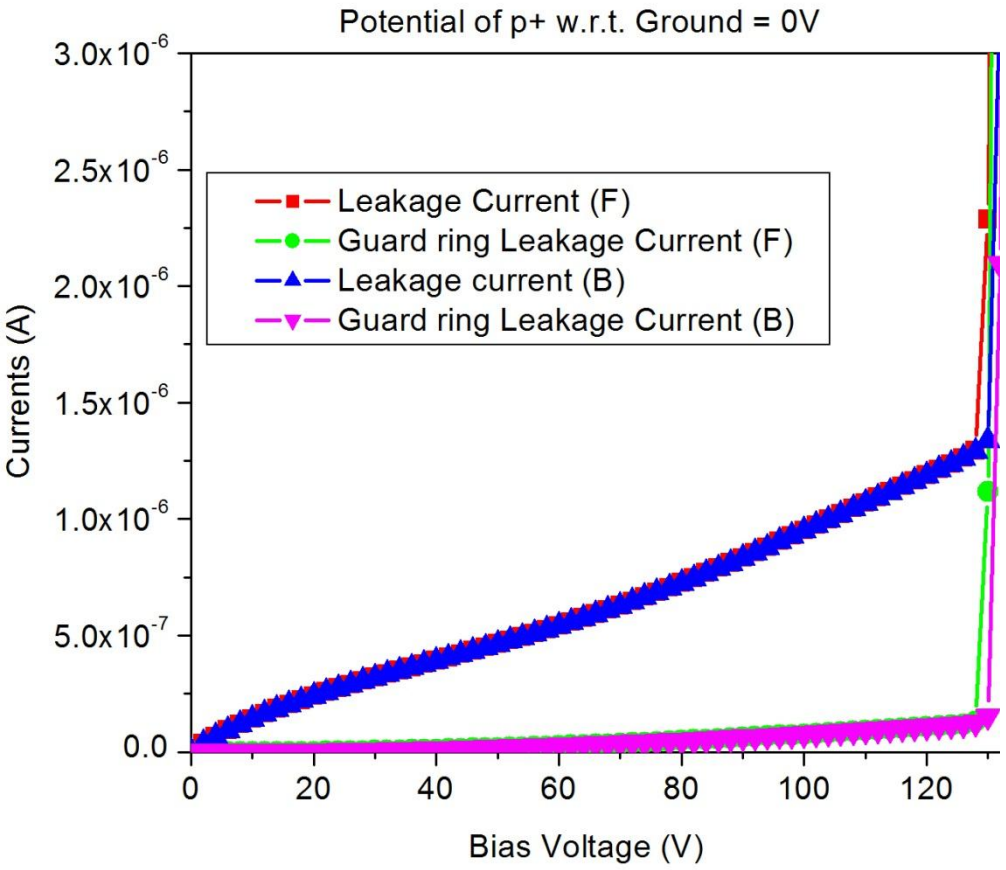
Test Setup

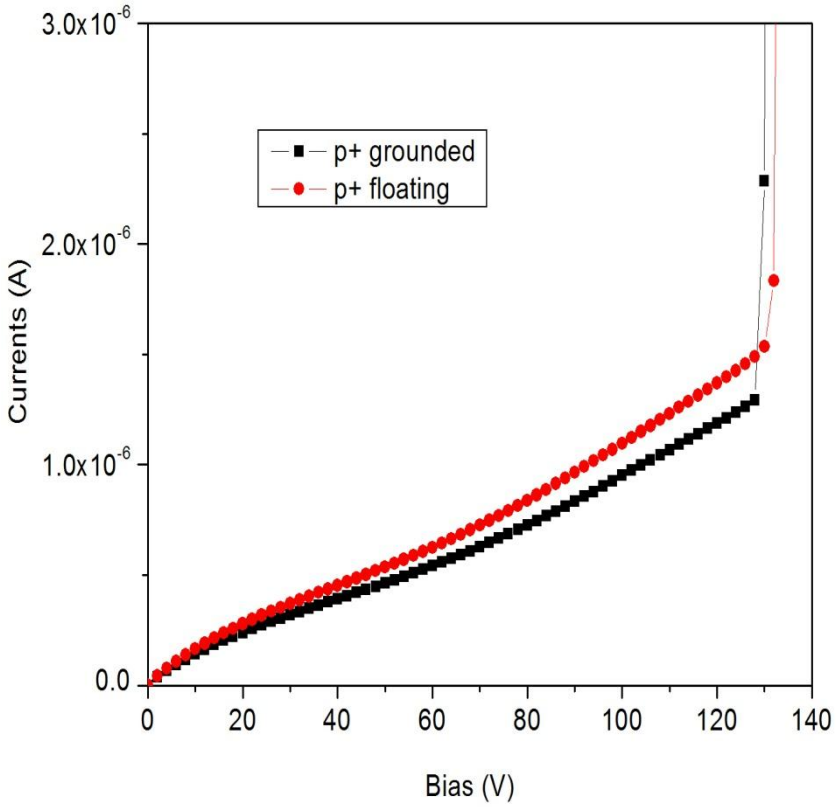
Fermilab





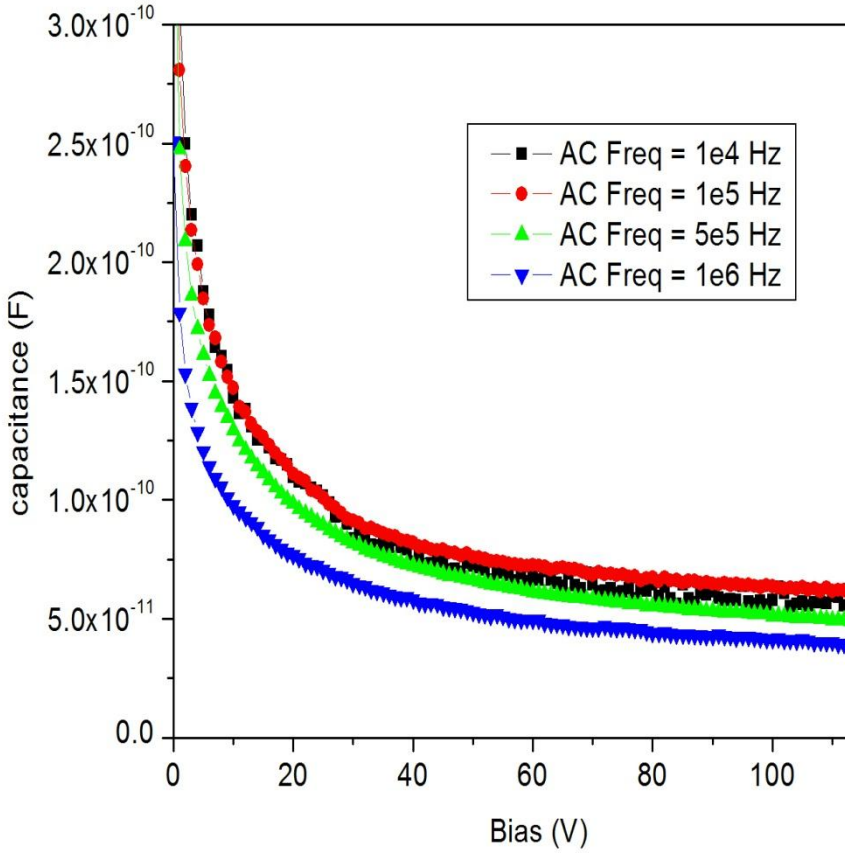
MAMBO V nested BNW/BPW:
C-V & 1/C² – V plots: HR1 substrate 325µm

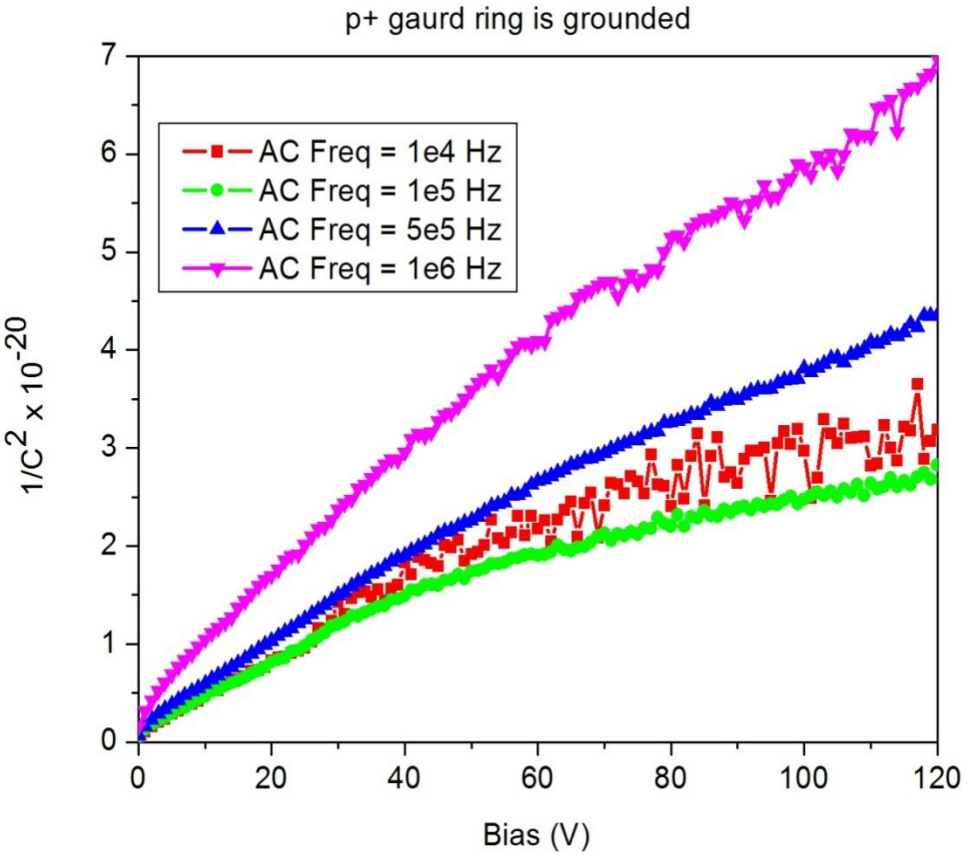




- Voltage breakdown around 130V
- Leakage current is 3 times larger compared to previous wafer (FZ)

MAMBO V nested BNW/BPW:
C-V & 1/C²-V plots: HR1 substrate < 1kΩ area (5.3 x 5.3 mm²)

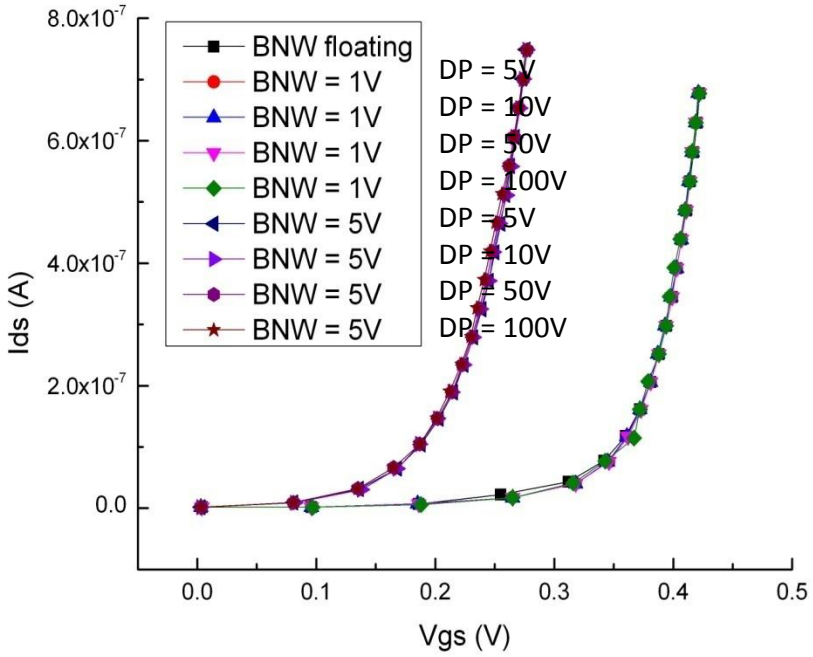


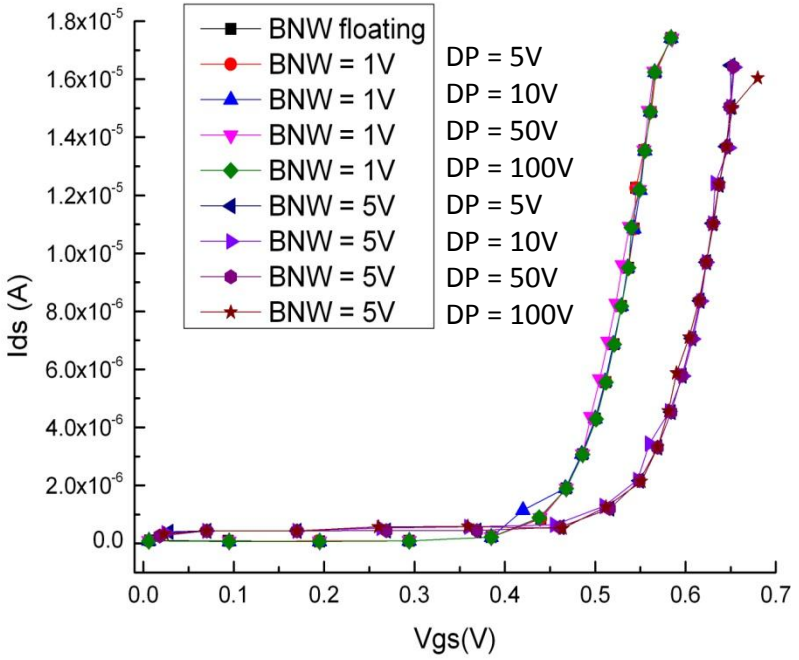


- Voltage breakdown occurs before full depletion is achieved
- Doping levels of substrate is not adequate (higher resistivity is desired)

Example of MAMBO IV results:

no shift of PMOS & NMOS transistor I_{DS}/V_{GS} in nested wells at back-gate biases ranging from 0 to 100V

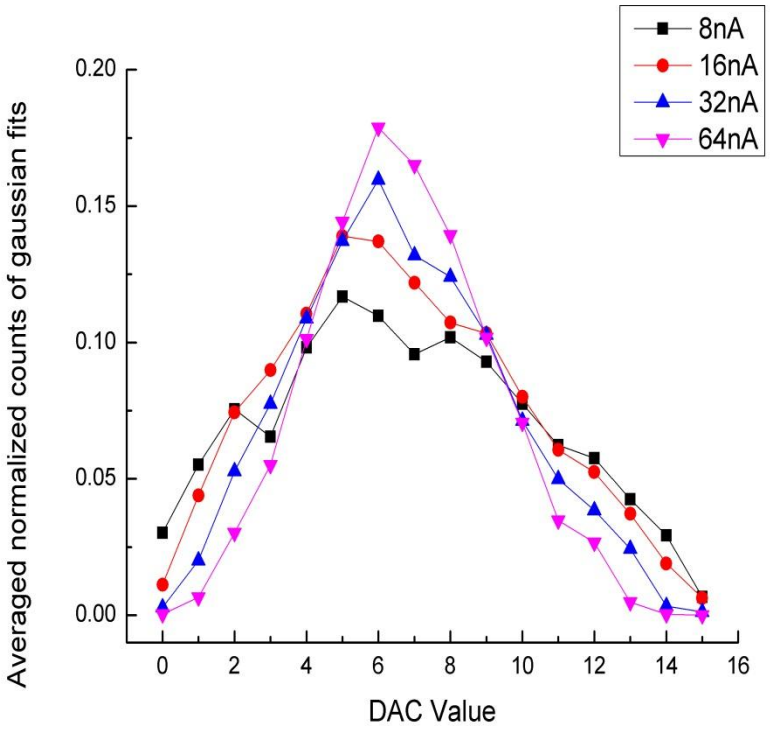




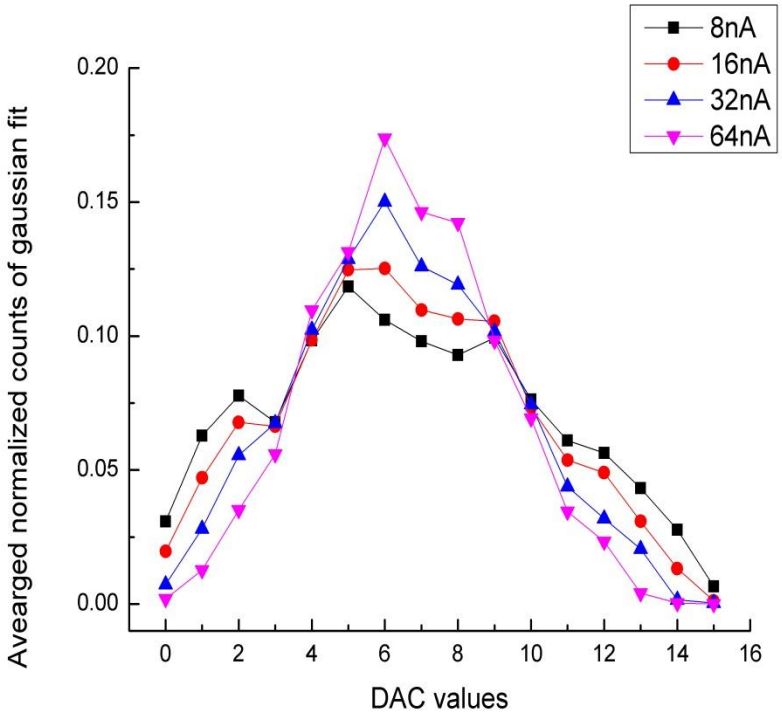
- For an NMOS transistor of size 41x(0.64µm/ 0.8µm) and PMOS transistor of size 41x(2µm/0.5µm) the plots indicate that there is no threshold voltage shifts on increasing the voltage on the die pad (V_{DP}) from 0-100V
- whereas on increasing the voltage of BNW (V_{BNW}) from 1-5V threshold voltage shifts of approximately 100mV for PMOS and 150mV for NMOS transistors is observed.

Trimming DAC threshold scans

Detector bias at 2V



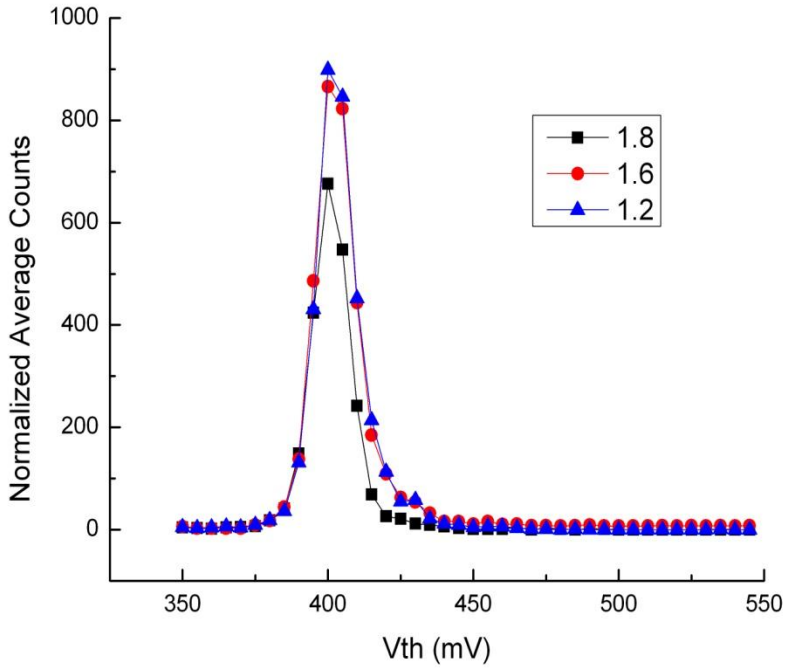
Detector bias at 20V



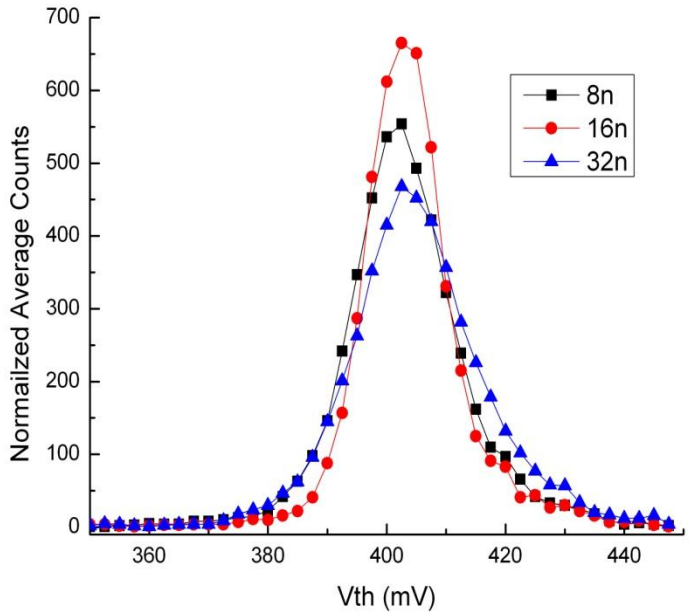
- For DAC current settings of 8nA to 64nA, with average non-linear LSB of 12mV to 27mV,corresponds to a voltage spread of ±90mV to ± 200mV respectively
- Digital circuit response independent of detector bias

DAC Scans: Count vs. Threshold (VthL)

Varying Counter voltage



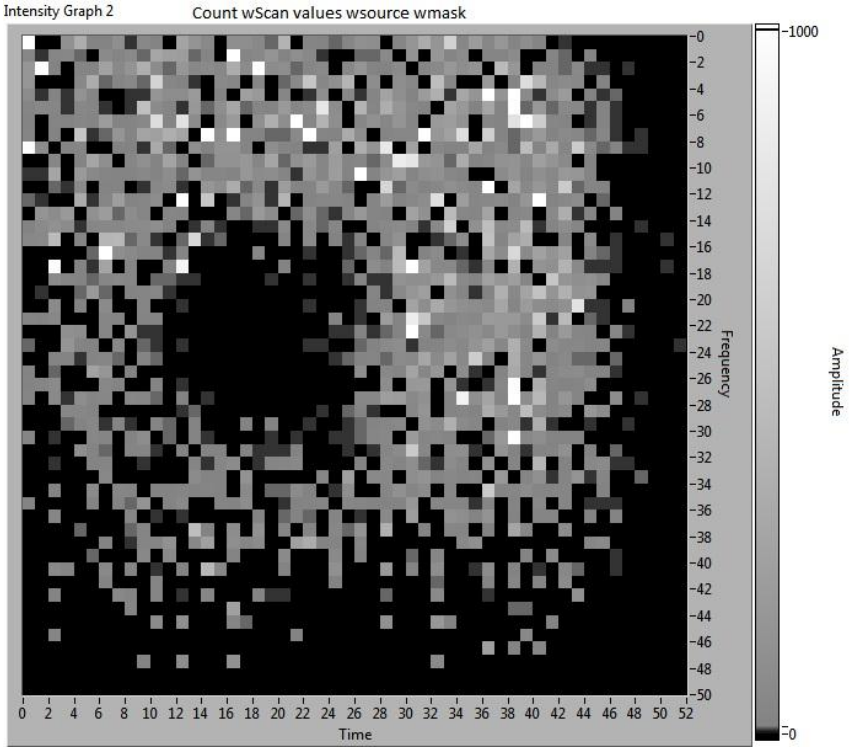
Varying DAC current



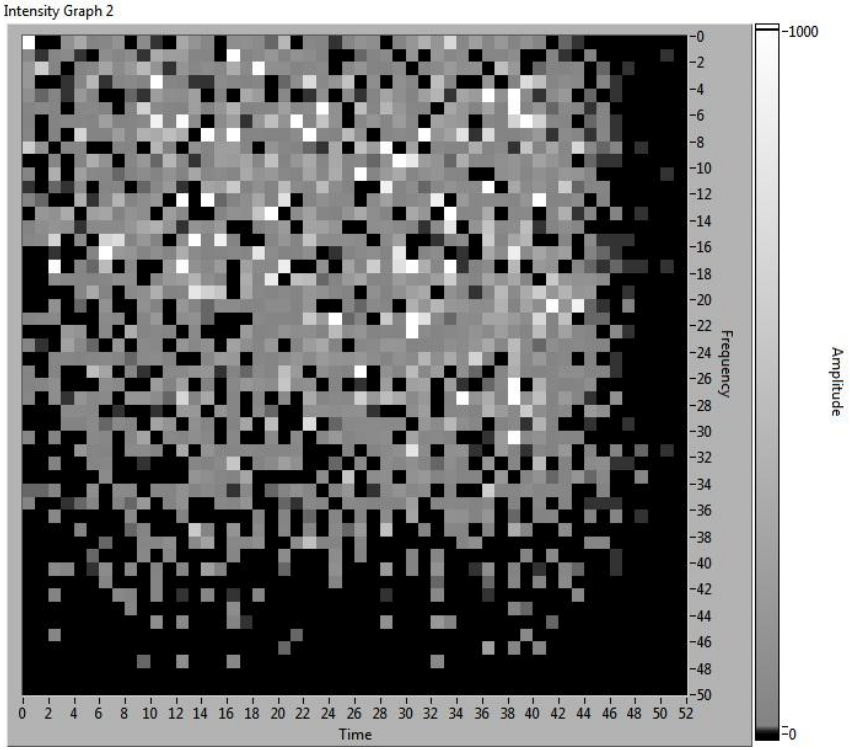
- Baseline set at 400mV
- VthL scanned from 350mV to 475mV

IMAGE with Cd^{109} source (22keV)

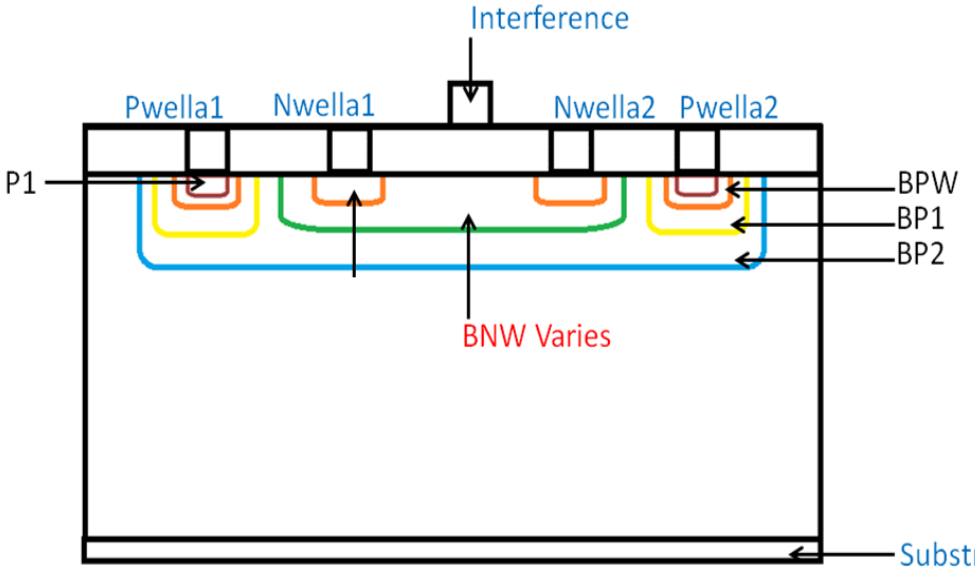
(1.9mm x 1.9mm) square mask

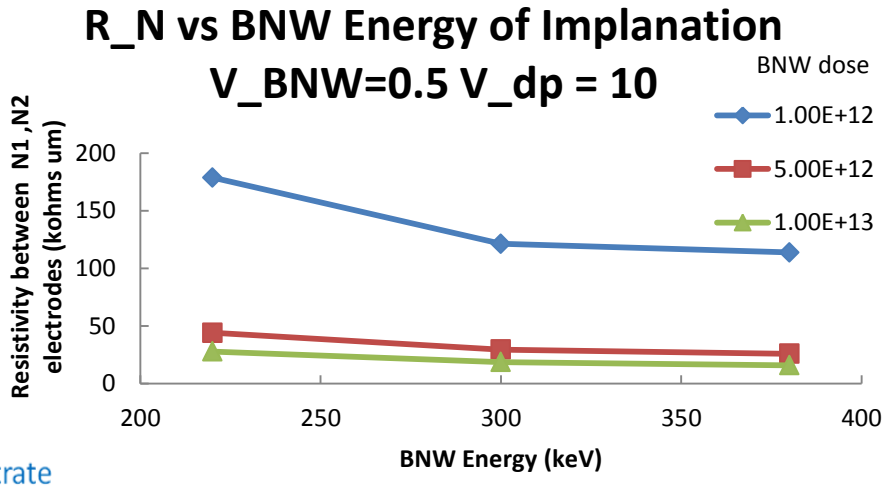


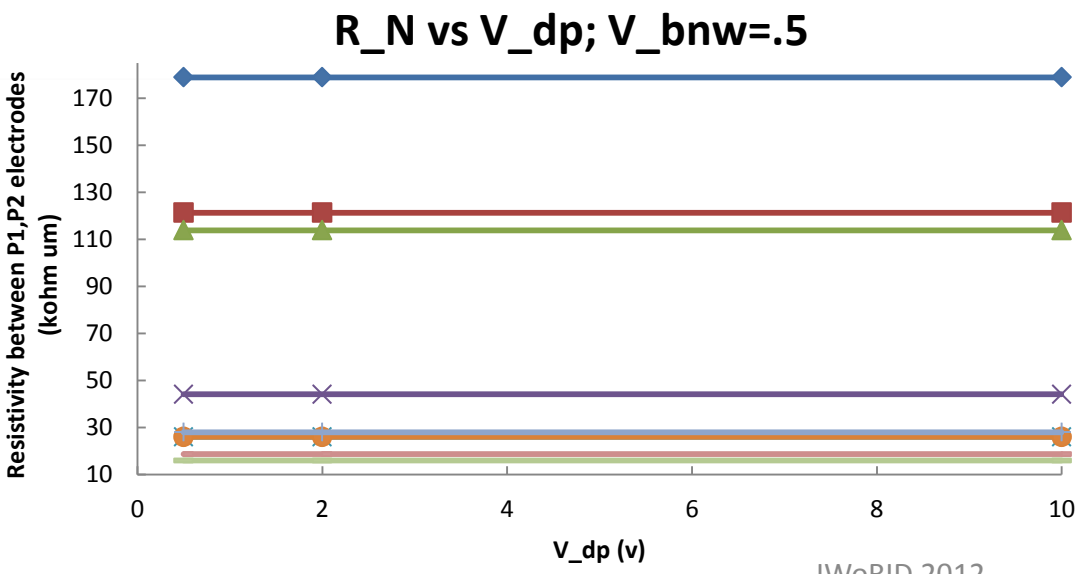
without mask



BNW resistance simulation



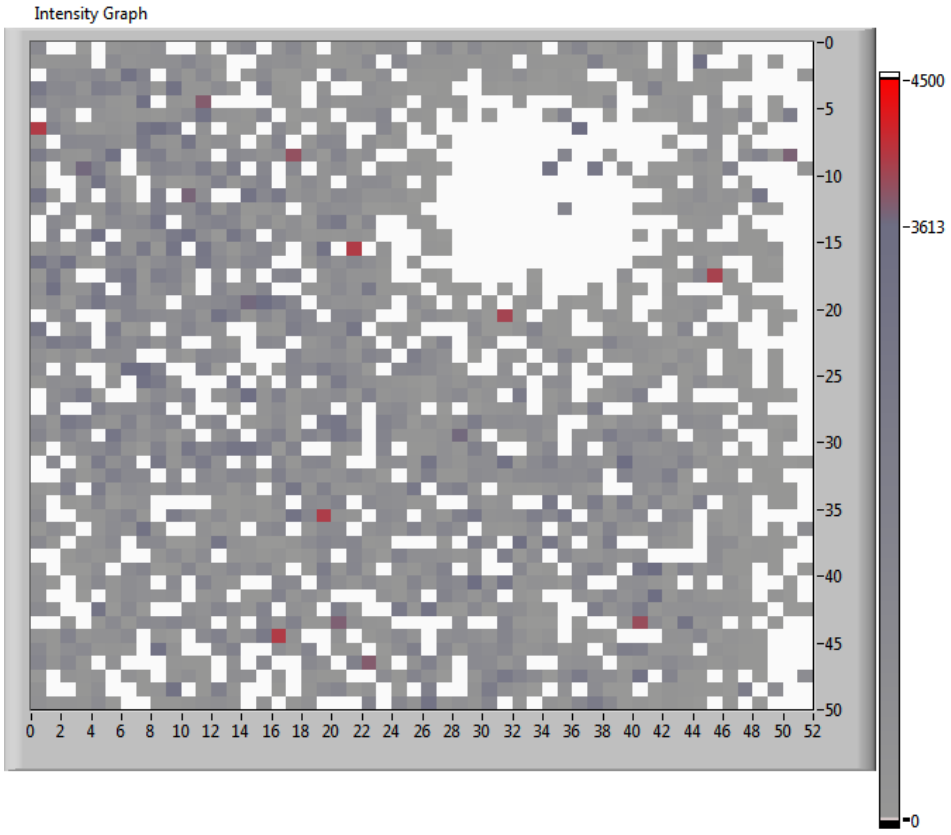




- Shallow and lower concentration of BNW produces higher resistance across the N well contacts
- The resistance is independent of the Die pad voltage

IMAGE with Cd^{109} source (22keV) with DiePad at 9V

(1.9mm x 1.9mm) square mask



- Analogue oscillations when Diepad voltage is increased beyond 3V
- Hypothesis: highly resistive BNW, requires more contacts
- Preamplifier gain reduced by operating front-end below 1V
- Image obtained with detector biased at 9V

Conclusions and Future Work

- **Extensions made to the process closer to obtain a fully functional detector with all satisfactory parameters**
- **Good effective collaboration with Lapis semiconductor**
- **First counting pixel SOI ASIC operated successfully with shielding of sensor from electronics**

• Include more BNW contacts in the pixel layout to compensate for BNW resistivity.

•Confirm and stabilize access to HR / FZ Si material

• Optimize nested wells BNW-BPW to decrease input capacitance or implement alternative shielding method

• Provide back processing (implantation and annealing); limit depth of implantation to allow entrance window for autoradiograpy at low energy of particle (w or w/o back Al)

• Optimize thickness of wafers for actual application 50-100μm for tracking 500 - 700μm or more for X-ray imaging

Questions?