Silicon Tracking Detectors: Lecture 2

Sally Seidel University of New Mexico

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The challenge of radiation damage to a silicon detector **Irradiation causes nonstop damage to the silicon, effectively producing artificial donor- and acceptor-like sites in the lattice.** Developing radiation tolerant detectors (and detectors that can be dynamically modified to respond to changing conditions) is a priority research activity.

The measurable unit of radiation is *integrated fluence*: energy deposited on a surface per unit area. Radiation damage depends on particle charge and mass – typically any damage is normalized to that of a 1 MeV neutron (" n_{eq} "). Target lifetime radiation hardness goals for LHC silicon are in the range $10^{15} - 2 \times 10^{16} n_{eq}/cm^2$, depending upon the expected distance of the detector from the interaction point.

Radiation sources in a particle collider:

- The main source of charged radiation: collisions at the interaction point, so their fluence $\Phi \sim 1/r^2$.
- The main source of neutrons: backsplash from the calorimeter, so their Φ depends on shielding and design.

Two types of effects: bulk damage and surface damage

Bulk radiation damage

Through-going particles cause **dislocations in the crystal lattice that disrupt the band structure**.

The displaced atom ("the primary knock-on atom (PKA)") becomes a silicon interstitial (Si_i) and leaves a vacancy. The recoiling PKA can strike neighboring atoms, so typically **damage** sites occur in clusters. The clusters can remain mobile and evolve, leading to macroscopic *time-dependent* effects.

- Neutrons cause cluster-like vacancy agglomerates through hard core nuclear scattering.
 Protons add isolated vacancies and interstitials: "point defects" through Coulomb interactions.
 Pions are the most common product of proton-proton collisions AND they cause
 - proton-proton collisions AND they cause
 the worst damage to silicon, through Δresonance production when they collide
 with a proton in a nucleus in the detector.



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Surface damage

Silicon in the wafer naturally develops a layer of SiO₂. Ionizing radiation generates bound charge in that layer and at the interface between the Si and the SiO₂.

The interface states become filled and saturate at about 100 kRad so for the sensors this is not as severe a problem as the bulk damage. But surface damage is a major challenge for readout electronics.

No saturation of bulk damage has been observed, up to $\Phi = a few \times 10^{15}/cm^2$.

The radiation damage changes everything about the operation of the device. Typically radiation adds donors and removes acceptors. Contemporary designs are the response to this pressure. Leakage current increases:

$$J(\Phi) = \alpha \Phi + J_{\text{intrinsic}}$$

where α is the "current-related damage constant." The $\Delta J = \alpha \Phi$ is due to production of generation-recombination centers in the semiconductor's bandgap.

Leakage current causes stochastic noise in the amplifier:

$$ENC \sim \sqrt{I_{leakage} \cdot au_{shaping}}$$

Remedy: cooling. The ATLAS pixel detectors operate at -10°C. The ATLAS strips operate at 0°C.

The effective dopant concentration of the substrate changes with fluence.

•
$$\Delta N_{eff} (\Phi) = \Delta (N_{donor} - N_{acceptor}) = N_C + N_a + N_Y$$
 where:

- $N_C = N_{c0}(1 e^{-c\Phi}) + g_C\Phi$: "stable damage" coefficient, with no time constant
- $N_a = g_a \Phi e^{-t/\tau(a)}$: "short term beneficial annealing" which is insignificant after 2 days at room temperature
- $N_Y = g_Y \Phi(1 e^{-t/\tau(Y)})$: "reverse annealing." Its value begins at 0 for t = 0 and grows to saturate at $g_Y \Phi$ as t approaches ∞



The damage continues to develop after the irradiation is over and is thought to be due to thermal mobility and aggregation or disaggregation of the defects).

This reverse annealing rate is temperature dependent and can be substantially suppressed below about -5C. **Problem:** (Recall from Lecture 1 Slide 18) the potential needed to deplete the sensor is directly related to $|N_{eff}|$:

$$V_{depl}(\Phi) = \frac{w^2 q N_{eff}(\Phi)}{2\varepsilon}$$



Notice: V_{depl} and $I_{leakage}$ both depend upon fluence Φ , so power consumption (heat generated) ~ fluence Φ^2 . This has significant impact on cooling and power budget.

Problem: after type inversion, the junction is on the back side.

In "p-on-n" sensors (p implants, n bulk): depletion zone grows from the pimplants to the backplane n-implant. These detectors can be operated underdepleted if necessary as the signalforming depletion region is always in contact with the segmented strips.



The polarity of the bias voltage remains unchanged **after inversion**, **but the signal doesn't reach the readout until the full depletion is achieved**.



Solutions to this problem: n^+ -on-p or n^+ -on-n.

Surface damage to the bonds at the silicon-SiO₂ interface grows. Implications:

- These attract electrons from the bulk to produce an "accumulation layer" of fixed negative charge between n-type implants of a detector. The isolation of adjacent structures can be compromised, leading to "microdischarge."
- The capacitance (which depends on the effective area of the implants) grows.



Remedies: structures of p-type material that disrupt the accumulation layer:

- p-stops a p-implant structure
- p-spray a diffuse layer of p-dopants matched to the surface charge saturation value is 3×10¹²/cm²
- or a combination of p-stops and p-spray Sally Seidel

Problem: Signal loss

Bulk defects produce metastable states. Delayed release of charge from these states leads directly to loss of collected signal. Example for a silicon detector of thickness 300 microns, operated at 500 V and 300 K, with $V_{depl} = 50$ V:



B. Baldassarri et al., NIM A 845 (2017) 20-23 Sally Seidel

Problem: trapping centers lead also to the development of a second junction:

Thermally generated carriers in the bulk are trapped in the course of their drift to the electrodes. Expected linear electric field across the bulk becomes parabolic and charge collection is reduced.



At this fluence, measuring $1/C^2$ versus V_{bias} will no longer predict the charge collection, as it presumes a linear E field extending across the full bulk – better to measure charge collection efficiency ("CCE") directly, typically by stimulating the sensor with a penetrating (IR) laser.

These radiation effects have stimulated technological development.

One response to the type-inversion of n-type bulk is: Build the sensors on p-type substrate to begin with. Optimize the readout for signals from n-on-p detectors. (This is the baseline for ATLAS and CMS upgrades.)

Advantages:

 n-strips on p-bulk collect electrons

Electrons' drift velocity is ~3 times faster than holes'.

 economical advantage: n-in-p sensors do not need structures to accommodate the type inversion, so they can be processed on 1 side only and are less sensitive to damage on the back side.



One response to the rising depletion voltage is to reorient the electrodes. Traditional planar detectors place the electrodes on the surface. **"3D" detectors orient the electrodes perpendicular to the surface using Deep Reactive Ion Etching (DRIE)**:



Combating the effects of radiation damage by engineering the semiconductor:

Approaches:

• Defect engineering: Enrich the silicon substrate with oxygen before irradiation: the oxygen is thought to capture vacancies in stable and electrically neutral point defects, leading to improved hardness against charged hadrons.

Observed results: reduced full depletion voltage, reverse annealing time constant increased

See: CERN RD50 Collaboration



Consider other semiconductors

Thus far silicon has outcompeted them on the basis of

- **ubiquity in industry**, leading to competition pricing, available simulation tools
- small band gap provides low threshold for signal production
- high specific density provides high signal production rate
- rigidity allows self-supporting structures to be very thin
- high mobility for both carriers permits fast charge collection

But there is a strong worldwide effort in **diamond** sensor development (see: CERN RD-42 Collaboration). Diamond is used in beam condition monitoring at LHC.

| | | | i | |
|----------------|--|--|---|---------------|
| lower noise | Diamond | Property | Silicon | |
| | 5.5 | Band gap $E_g [eV]$ | 1.12 | |
| | 107 | E _{breakdown} [V/cm] | 3×10 ⁵ | |
| | 1800 | electron mobility μ_e [cm ² /Vs] | 1450 | |
| | 1200 | hole mobility μ_h [cm ² /Vs] | 450 | |
| | 2.2×10 ⁷ | saturation velocity [cm/s] | 8×10 ⁶ | |
| | 13 | ionization energy (produce e-h pair) [eV] | 3.6 | |
| | 4.4 | #e-h pairs per radiation length | 10.1 | signal |
| | 1200 2.2×10 ⁷ 13 4.4 | hole mobility μ _h [cm ² /Vs] saturation velocity [cm/s] ionization energy (produce e-h pair) [eV] #e-h pairs per radiation length | 450 8×10 ⁶ 3.6 10.1 ← | more signa |

Putting the detector together: combining the sensor, front-end electronics, mechanical support, cooling, and connections into a module



The module typically includes:

Sensors (here there are 4, back-to-back strip sensors with small stereo angle)



Preamplifier chips (here there are 12).

Mechanical support

Aluminum wirebonds connect chips and sensors to the pitch adaptor:



But through-silicon-vias (TSV) can replace wirebonding in the upgrade era. 21

The "**hybrid**" (here it is kapton flex): wraps above and below sensors, carries

- the preamplifier chips,
- a pitch adaptor between sensors and readout chips,
- a connector to the off-detector electronics,
- copper routing for signals and power.

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A little more about strip detector modules, because modules have so many roles (using a cross section of the ATLAS SCT as an example):



- Hybrid bridges over the sensor for reduced risk of damage
- High thermal conductivity critical
- Minimize radiation length
- High mechanical strength in carbon-carbon

An example barrel of installed modules (in ATLAS):



The structure of a *pixel* module differs from that of a *strip* module because the **preamplifier chips are placed directly below their sensors:**



Connections are provided with the "flip chip technique" by metal bumps typically solder or indium of diameter about 15 µm.

Pixel detectors are typically chosen over strips for innermost tracking.

Pixel advantages:

- Very fine space-point resolution without need for stereo or double-sided detectors
- small pixel area: low geometrical capacitance --- high signal to noise ratio

And disadvantages:

The number of connections is high, and connection rework is difficult

Hybrid versus monolithic pixels

Pixel detectors that combine separate sensor and electronics, fabricated with different processes, are a hybrid technology.

The *hybrid* geometry of the detector *introduces substantial material into the detection volume*.

This can be traced to the demands this design makes on the power budget through: sensor bias, analog and digital architecture, and data transmission.

This translates to copper conductors and cooling systems, and reduced positional resolution.

Initiatives to reduce power consumption in hybrid detectors:

- reduce material per detector layer
- integrate power conductors in mechanical support
- introduce special powering systems including DC-DC converters and serial powering of modules.

A different solution: monolithic detectors....

Monolithic detectors integrate the sensor with the readout.

Monolithic silicon tracking detectors have been used by

- **BELLE-II** (DEPFET technology) and
- **STAR** (Monolithic Active Pixel Sensor –MAPS– technology).

They are under consideration for future experiments including those at CLIC, ILC, and LHC.

On the next pages: some monolithic technologies in active development.



Monolithic Active Pixel Sensors^{1,2} (MAPS) use an nchannel MOSFET transistor (NMOS) embedded in an *epitaxial* p-layer (thickness 15 microns) similar to standard CMOS chips. The nwell of the transistor collects the electrons generated by charged particles from a thin depletion layer through diffusion only.

¹ R.Turchetta, et al., Nucl. Instr. and Meth. in Phys. Res. A 458: 677-689, 2001.
 ² I. Peric, Nucl. Instr. and Meth. in Phys. Res. A 582: 876-885, 2007.

Image from: F. Reidt, "Upgrade of the ALICE Inner Tracking System," POS (VERTEX2014) 007.

Related technology: HV-CMOS and HR-CMOS

A deeper depletion layer and hence larger signals are achieved by applying higher bias voltages or by the use of high resistivity epitaxial layers.

The electrons are collected through drift.

MAPS advantage: a mature commercial process MAPS challenge: not yet LHC-level radiation hard.



Image taken from: M. Benoit et al., 2018 JINST 13 P02011.

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The Silicon on Insulator^{1,2} (SoI) sensors overcome the problem of the low signal from only partially depleted sensors by combining a high resistivity silicon sensor wafer with a low resistivity electronics wafer, chemically bonded together. Transistors implemented in the electronics wafer are connected to the implant of the sensors, which is fully depleted.



¹Y. Arai, et al., Nucl. Instr. and Meth. in Phys. Res. A 623: 186-188, 2010. ²J. Marczewski, et al., Nucl. Instr. and Meth. in Phys. Res. A 549: 112-116, 2005.

Image from "A thin fully depleted monolithic pixel sensor in Silicon on Insulator technology," S. Mattiazzo et al., PIXEL2012. Sally Seidel

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In *DEPFET (Depleted P-channel Field Effect Transistor)* detectors¹ a potential valley for electrons is created underneath the p^+ strips within the n bulk. Accumulated electrons drift underneath the gate of a field effect transistor and modify the source drain current producing a built-in amplification. Following the readout the accumulated electrons have to be swept away by an active clear.





A new technology to resolve multiple interactions at the HL-LHC: Low Gain Avalanche Detectors, Ultra-fast Silicon Detectors¹

The issue: not every one of these vertices occurred at the same time – they are separated by tenths of nanoseconds. Ultrafast timing detectors can distinguish them – simplifying pattern recognition.



H. F.-W. Sadrozinski et al., NIM A 730 (2013) 226-231.

Very thin, high resistivity n-on-p wafers, for fast collection time, to overcome saturation of drift velocity at 10⁷ cm/s. Since resolution depends on S/N, boost signal with an extra implantation step to create a p layer just under the n-layer, yielding a localized high field region that amplifies drifting electrons.

Target gain: 10, for high rate operation, good time resolution, excellent position resolution. *Target thickness:* 35-50 microns

Target time resolution: 40 psec

Key: minimize slew rate (signal/rise-time), do not amplify hole signal



Top challenge now: radiation hardness

Outlook Silicon detectors have been central to paradigm-changing particle physics discoveries for over 30 years.

Exciting new technologies are still emerging.

There is so much more to say – we have not even touched upon silicon's applications outside of HEP.

There is room for your contributions everywhere – please join the detector community!

For more information, please see S. Seidel, "Silicon strip and pixel detectors for particle physics experiments," Physics Reports 828 (2019) 1-34.

Backup

• Crystal orientation

Sensors with features registered along different crystal planes (denoted by Miller indices) may have different electrical characteristics before irradiation but are comparable after irradiation



The crystal orientation is specified by the location of the flat on the silicon wafer.

<111>:

- chosen by CDF SVX, ATLAS SCT <100>
- chosen by CDF L00, CMS pixels, ATLAS pixels, LHCb

Use of 6-inch wafers is now standard.



Summary on readout noise, from "Pixel Detectors" by L. Rossi et al. (Springer,

2006)

$$ENC = \frac{\text{noise output voltage (rms)}}{\text{signal output voltage for the input charge of 1e}}$$

$$ENC_{tot}^{2} = ENC_{shot}^{2} + ENC_{therm}^{2} + ENC_{1/f}^{2}$$

$$ENC_{shot} = \sqrt{\frac{I_{leak}}{2q}\tau_{f}} = 56e^{-} \times \sqrt{\frac{I_{leak}}{nA}\frac{\tau_{f}}{\mu s}}$$

$$ENC_{therm} = \frac{C_{f}}{q}\sqrt{\langle v_{therm}^{2} \rangle} = \sqrt{\frac{kT}{q}\frac{2C_{D}}{3q}\frac{C_{f}}{C_{load}}} = 104e^{-} \times \sqrt{\frac{C_{D}}{100 \text{ fF}}\frac{C_{f}}{C_{load}}}$$

$$ENC_{1/f} \approx \frac{C_{D}}{q}\sqrt{\frac{K_{f}}{C_{ox}WL}}\sqrt{\ln\left(\tau_{f}\frac{g_{m}}{C_{load}}\frac{C_{f}}{C_{D}}\right)} = 9e^{-} \times \frac{C_{D}}{100 \text{ fF}} \text{ (for NMOS trans.)}$$

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W, L = width and length of trans. gate $K_f = 1/f$ noise coefficient $C_{ox} =$ gate oxide capacitance C_f = feedback capacitance C_{load} = load capacitance C_D = detector capacitance τ_f = feedback time constant Evolution of the scale of silicon detector coverage in HEP experiments



Year

Binary resolution of strip sensor for pitch p

$$\sigma^{2} = \frac{-\frac{p}{2}}{\int_{-\frac{p}{2}}^{\frac{p}{2}} D(x_{r}) dx_{r}} = \frac{p^{2}}{12}$$

$$\sigma^{2} = \frac{-\frac{p}{2}}{\int_{-\frac{p}{2}}^{\frac{p}{2}} D(x_{r}) dx_{r}} = \frac{p^{2}}{12}$$

$$\int_{-\frac{p}{2}}^{\frac{p}{2}} D(x) = 1 \text{ uniform distribution of tracks}$$

$$X_{m} = 0 \text{ pixel centre}$$



Silicon wafer fabrication

Float Zone

- Using a single Si crystal seed, melt the vertically oriented rod onto the seed using RF power and "pull" the monocrystalline ingot
- Can be oxygenated by diffusion at high T

Epitaxial silicon

- Chemical-Vapor Deposition (CVD) of Silicon
- CZ silicon substrate used a diffusion of oxygen
- Growth rate about 1mm/min
- Excellent homogeneity of resistivity
- 150 mm thick layers produced (thicker is possible)price depending on thickness of epi-layer but not

exceeding ~ 3 x price of FZ wafer

Czochralski silicon

- Pull Si-crystal from a Si-melt contained in a silica crucible while rotating.
- Silica crucible is dissolving oxygen into the melt at high concentration
- Material used by IC industry (cheap). Also available in high purity for use as particle detector (MCz) 41

The environment for the experimenter characterizing the sensors

Silicon detectors can operate in air and at room temperature – but as radiation damage progresses, cooling becomes essential.

