# **TSU CONS Reliability**

**Progress Meeting - #5** 



## Study workflow Steps followed in the reliability analyses in BISv2







# **Failure rate prediction**

The first step of the analysis



#### **Failure rate prediction** 217Plus standard & Isograph

- **Objective:** establishing probabilities of failure for individual components.
- **217Plus: 2015 & Isograph:** completed by using 217Plus models [4] in Isograph [5], aided by automated scripts processing design files [6].
- Failure models: combine empirical data with physics-of-failure models, being adjustable for specific environmental and operational conditions.
  - Factors like temperature, voltage, environment adjustable for components depending on the category
  - Certain parameters can be set globally to apply to all components (see next slide).

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Prediction -		Grid Grid	Plot	💾 Plot & Grid	ibraries 🍥	Parts Library	Reports		
ProjectiD>		Predict	ion blocks	• General • 🚰 🍸	¥ 🍞 AI	l rows - 川 🥻			
0:FR=1971 FITS 2:Beam 2:FR=940			ю	Part number	Descriptio	n		Category	Failure rate
Beam 1 User Input connector:FR= S:Power Management:FR=89.63 Seam 1 BiC connector:FR=0.4674 IBeam 1 FE=040		Re	2	0-2	Beam 2			System Block	940
			2.1	10TPB47M	±20% 10V	±20% 10V ESR 0R07 Tantalum Solid C ±20% 10V ESR 0R07 Tantalum Solid C		Capacitor	0.9288
		74	2.3	10TPB47M	±20% 10V				
B 5:Be Block Properties - 2.2 : ±20			R OR07 Tant	talum Solid Capacitor w	ith Condu	h Condu ? X m Solid C		Capacitor	0.9279
🕀 🥅 7:Be							m Solid C	Capacitor	0.9279
Derating	General Parameters	Rate/Pi Fact	ors Notes	Hyperlink			PROMs	External	2
			1.00				igger	External	0
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	Adju	stment Facto	r: 1				igger	External	0
	Yearo	Manufactur	2020				DC with	IC, Plastic Encap	1.383
		Duty Cycl	: 1				pose Tra	Transistor	37.59
		Cycling Rat	: 2				pose Tra	Transistor	37.59
	Ambient Te	mp. Operatin	rating: 35			pose Tra	Transistor	37.59	
	Ambient T	emp, Non-Op	.: 25				pose Tra	Transistor	37.59
	c	apacitor Typ	Auminum	1	~		pose Tra	Transistor	37.59
	Capaciti	ince (Micro F	): 47				pose Tra	Transistor	37.59
	Elec Stre	ss Calc Mod	: Calculate	d	~		pose Tra	Transistor	37.59
	Voltag	e Stress Rati	0.1				pose Tra	Transistor	37.59
	Operati	ng Voltage (N	): 1	1			pose Tra	Transistor	37.59
	Rat	d Voltage (V	10				pose Tra Transistor	Transistor	37.59
	Ambient-Ca	se Temp Ris	: 10				er Chip C	Capacitor	0.3395
							er Chip C	Capacitor	0.3503
	Stress= Tem	p=			OK	Cancel	er Chip C	Capacitor	0.3395
-			2.58	CC0603_10NF_	10% 50V	X7R SMD Multila	yer Chip C	Capacitor	0.3503
			2.55	CC0603_10NF_	5 ±10% 50V	X7R SMD Multila	yer Chip C	Capacitor	0.3395
			2.59	CC0603_10NF_	5 ±10% 50∨	X7R SMD Multila	yer Chip C	Capacitor	0.3503
			2.56	CC0603_10NF_	5 ±10% 50V	X7R SMD Multila	yer Chip C	Capacitor	0.3503
			2.50	CC0603_10NF_	5 ±10% 50V	X7R SMD Multila	yer Chip C	Capacitor	0.3503
			2.51	CC0603_10NF_	5 ±10% 50V	X7R SMD Multila	yer Chip C	Capacitor	0.3503
			2.57	CC0603_10NF_	5 ±10% 50V	X7R SMD Multila	yer Chip C	Capacitor	0.3395
			2.18	CC0603_100NF	±10% 50V	X7R SMD Multila	yer Chip C	Capacitor	0.3396
			2.19	CC0603_100NF	±10% 50V	X7R SMD Multila	yer Chip C	Capacitor	0.3396
			2.13	CC0603_100NF	±10% 50V	X7R SMD Multila	yer Chip C	Capacitor	0.3529
			2.20	CC0603_100NF	±10% 50V	X7R SMD Multila	yer Chip C	Capacitor	0.3396
			2.21	CC0603_100NF	10% 50V	X7R SMD Multila	yer Chip C	Capacitor	0.3396

Screenshot of Isograph Reliability Workbench [2] (tool used for FMECA analysis)



#### **Assumptions** Global parameters and mission profile

Year of manufacture: 2020

Duty cycle: 1 (i.e., always on)

Cycling rate: 2 (i.e., two power cycles in a year)

Ambient temperature, operating: 35

Ambient temperature, non-operating: 25

Relative humidity: 0.5

#### 2.2.1.1 Global Constants

Several variables are common to all 217Plus<sup>TM</sup> component models. These are known as global parameters. These global parameters are as follows:

- Y =Year of manufacture
- D = Duty cycle (the percent of calendar time that the system in which the component is operating is in an operational state)
- $T_{AO}$  = Ambient temperature, operating (in degrees C)
- $T_{AE}$  = Ambient temperature, nonoperating (in degrees C)
- CR =**Cycling rate** (the number of power cycles per year to which the system is exposed). In this case, it is assumed that the system transitions from a nonoperating environment to an operating environment at the same time that the power is applied.
- RH = Relative humidity

Excerpt from the 217Plus document [7]

Parts assumed to be used within their ratings, no modifications made to quality and process factors (217Plus standard assumed).





# **Trigger Synchronization Unit Board**

Statistics of the project and preliminary failure rate estimation



#### Number of components in categories Total number of components: 739





#### **Distribution of components across pages** Total number of components: 739





## **Total FITS of design pages** Total FITS of components in a given page (66,997)





### **Total FITS of design pages (w/o U\_Config)** Total FITS of components in a given page (2,618)





## FITS of component categories Distribution of number of predicted failures in 10<sup>9</sup> hours across categories







# **TSU Rear Transition Module Board**

Statistics of the project and preliminary failure rate estimation



#### Number of components in categories Total number of components: 207





#### **Distribution of components across pages** Total number of components: 207





#### **Total FITS of design pages** Total FITS of components in a given page (299)





24 May 2024

#### TSU CONS Reliability Study #5

### FITS of component categories Distribution of number of predicted failures in 10<sup>9</sup> hours across categories





Average FITS in a given category



24 May 2024

#### TSU CONS Reliability Study #5

#### Failure rate prediction summary Conclusions of the first step

The total failure rates are the following:

- **TSU Board:** 2,618 FIT (w/o rotary switches).
- TSU RTM Board: 299 FIT.

Results comparable to boards of similar size in BISv2 project.

Continuing the analysis to establish single points of failure as individual failure modes leading to critical failures could **further the confidence in the reliaiblity** by decreasing (potentially) the estimations **by orders of magnitude**.





## Next steps

Failure mode apportionment and end-effects



## Failure mode apportionment Based on FMDs and past experience

#### **Objective:**

- Identify failure rates for different end-effects (defined in top-level FMECA)
- Exclude possibility of common mode blind failures (across paths A & B)
- Weigh the trade-offs between end effects (e.g. false async vs. blind single path)

**Emprical data:** Completed by using models apporting overall failure rate to individiual modes based on field data, such as FMD-91 and FMD-2016.

#### Example

- Capacitor C1, failure rate 2.49 FIT:
  - Short (30%) 0.7 FIT.
  - Parameter change (61%) 1.5 FIT.
  - Open (6%) 0.1 FIT.

#### **End Effects from Top-Level FMECA**

- sync beam dump
- async beam dump
- missed beam dump
- no timestamp for Post Mortem, IPOC, etc.
- downtime



## **End-effects assignment**

		Component	Failure mode	Mode failure rate FIT	Expert-assigned end-effect
	C1	Capacitor	Drift	19.98	NO EFFECT
Experts & designers	C1	Capacitor	Shorted	10	BEAM DUMP
	D1	Diode	Shorted	4.57	NO EFFECT

- Designers assigning end-effect for the entire system to each failure mode (could be limited to critical parts of the design)
- Followed by a common review with designers, experts, reliability team
- Work-intense element of the study, requiring deep knowledge of the system
  - "What is the impact of a component failing one way on the entire board?"
  - As much support as possible provided.





## End Effects Example from another project

Blind failure (single path).	
Blind sync	Not generating asynchronous dump request.
Blind async	Not generating a synchronous dump request.
Blind	Not generating asynchronous nor synchronous dump requests.
Blind failure (both paths)	
Blind both paths sync	Not generating asynchronous dump request on both paths.
Blind both paths async Blind both paths	Not generating a synchronous dump request on both paths. Not generating asynchronous nor synchronous dump requests on both paths.
False dumps	
False dump async	Spuriously generate ONLY asynchronous dump request.
False dump sync	Spuriously generate ONLY synchronous dump request.
False dump	Spuriously generate asynchronous and synchronous dump requests.
Maintenance	Failure will cause maintenance action after the mission (LHC fill) is finished.



#### **Conclusions**

#### • Rotary switches – very high failure rate in 217Plus standard

- Establishing non-criticallity of their failures could let us focus on the remaining faults.
- Next steps:
  - Failure mode apportionment and end-effects assignment.
  - FMECA Tables are ready for both boards projects.





[1] MIL-HDBK-338B, US Department of Defence, 1 October 1998, <u>https://www.navsea.navy.mil/Portals/103/Documents/NSWC\_Crane/SD-18/Test%20Methods/MILHDBK338B.pdf</u>

[2] Failure Mode/Mechanism Distributions – 2016, Reliability Databook Series, Quanterion Solutions Inc., <u>https://www.quanterion.com/product/tools/failure-mode-mechanism-distributions-fmd-2016/</u>

[3] Table FMD-CB.csv, https://gitlab.cern.ch/mblaszki/fmeca-assist-tool/-/blob/cd5826e15fc053132d3b6e6cfb34f6e50755b08b/resources/FMD-CB.csv

[4] HDBK-217Plus:2015 Notice 1, Quanterion Inc., 15 January 2017, https://www.quanterion.com/products-services/tools/217plus/

[5] Isograph Reliability Workbench, Isograph Ltd., <u>https://www.isograph.com/software/reliability-workbench</u>

[6] Automatizing Component-FMECA Analyses for Electronics Assemblies, Joint RAWG & Electronics Forum Meeting, 11 April 2024, <a href="https://indico.cern.ch/event/1398920/">https://indico.cern.ch/event/1398920/</a>

[7] HDBK-217Plus:2015, Quanterion Solutions Inc., 15 December 2014, https://www.quanterion.com/product/publications/hdbk-217plus-2015/





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