# Updates from Japan group

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On behalf of the ATLAS ITk Japan group
Studies mainly by K. Imamura (Kyushu U.), K. Itabashi (KEK),
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2024/02/02 at ITk Pixel module QAQC Japan-LBNL discussion

# Updates since last discussion

- ~120 modules have been assembled
  - ~30 with a cell
- Follow-ups from the last discussions
  - Yield plots for each QC parameters
  - Further looks into the LPM issue
  - Bump disconnection study: comparison among the three methods (discbump scan, zerobias scan, X-ray scan)
- New topics
  - High noise near ASIC edge and its mitigation by LCC enabled
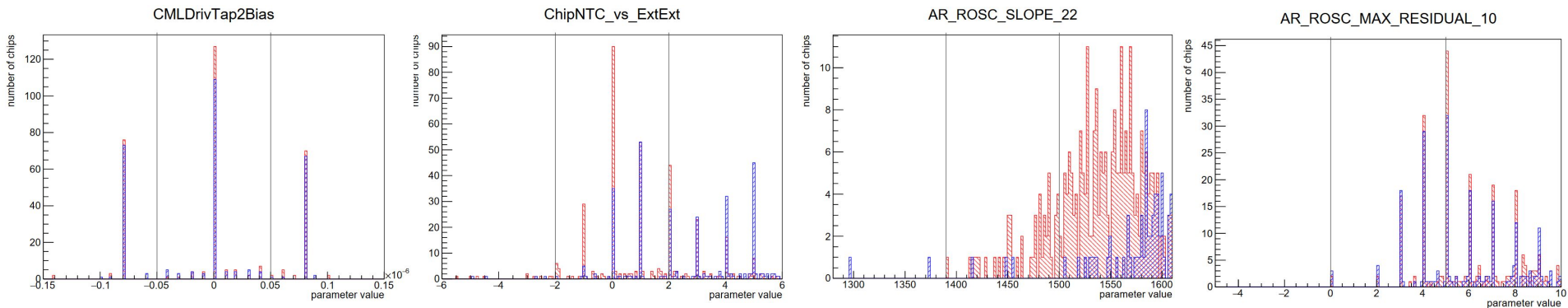
# Yield in elec. QC: analog readback

- Counted the numbers of passed/failed in each QC analysis in INITIAL_WARM
  - Selections are based on mqat v2.2.2rc0; these may not be always latest...



CMLDrivTap2Bias

NTC-related

RO slope (19, 21, 22, 23)

RO max. residuals
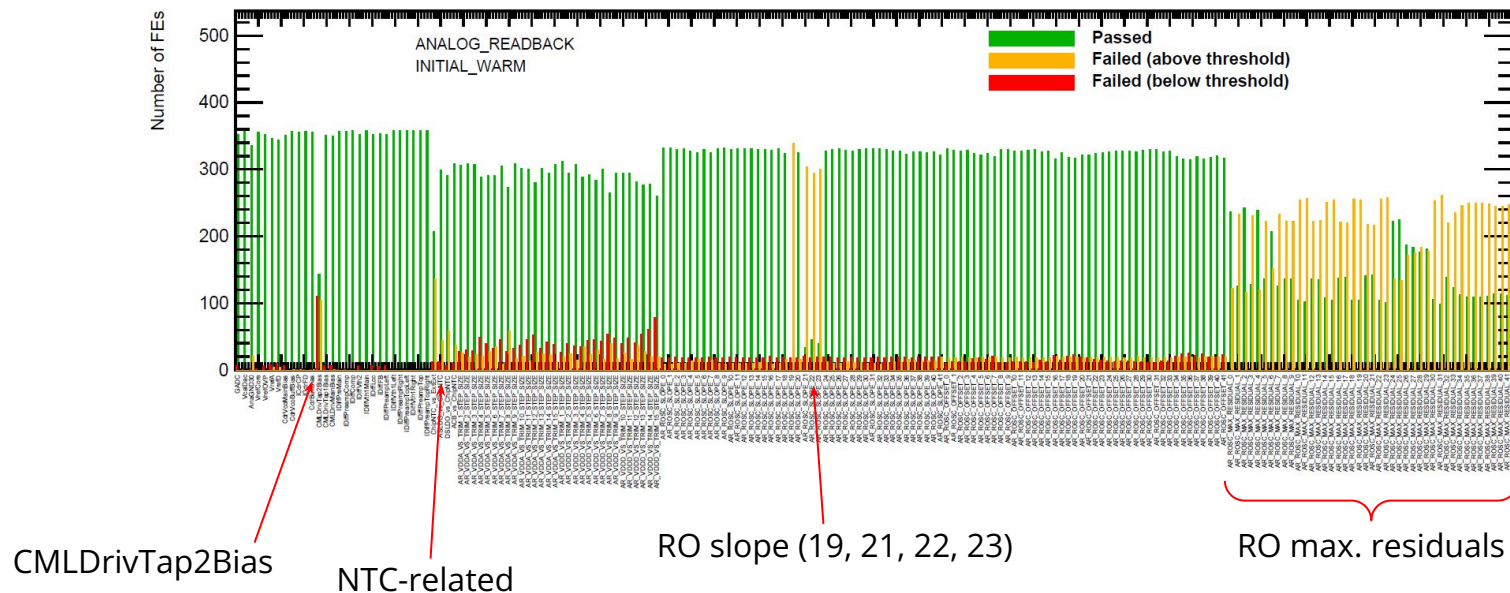
# Yield in elec. QC: analog readback

- Typical distributions



CMLDrivTap2Bias | ChipNTC_vs_ExtExt | AR_ROSC_SLOPE_22 | AR_ROSC_MAX_RESIDUAL_10

→ Will be removed from
QC judgement

# NTC-related parameters

- Checked Chip NTC - external NTC distribution
    - Some chip dependence? (smaller variation in FE2 than other FEs etc.)
    - Indication that the size of variation reflects quality of the contact between module and cooling head



Implemented an improvement on the contact between a module and cooling head

OB modules (w/ a cell)
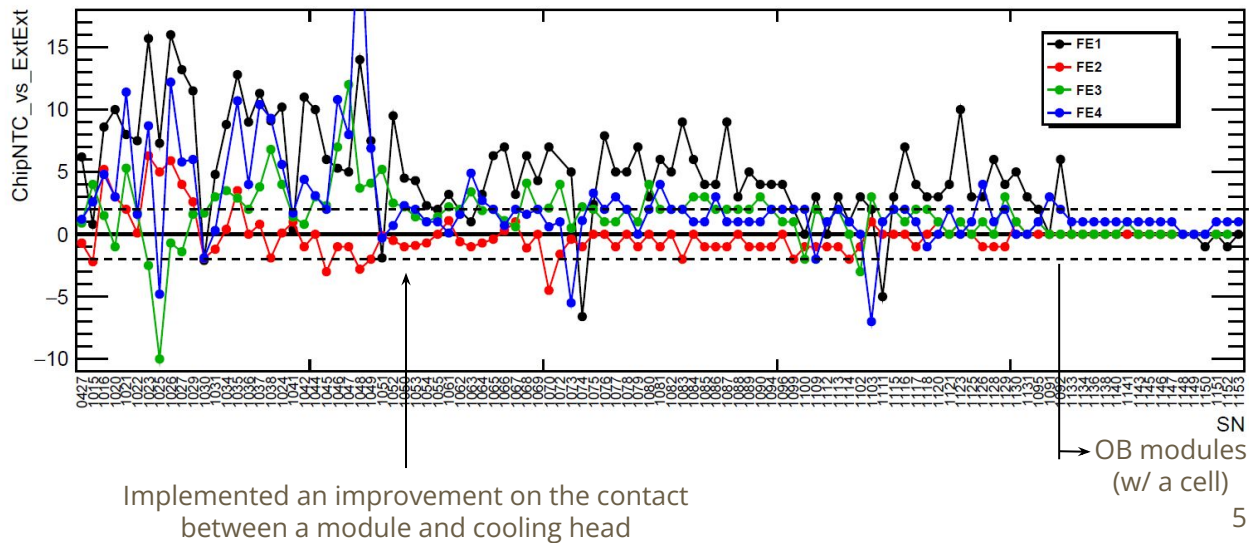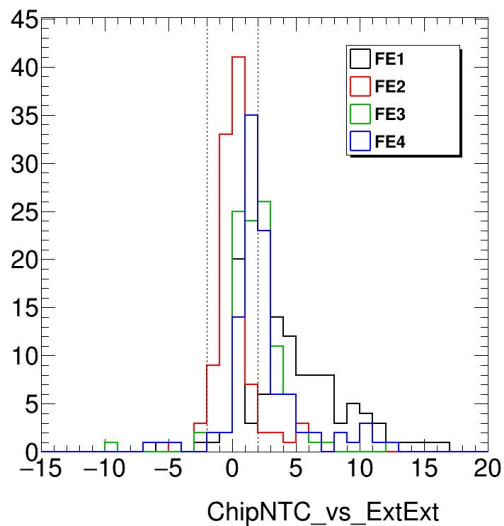
# Yield in elec. QC: SLDO

- Some failures observed in the SLDO test
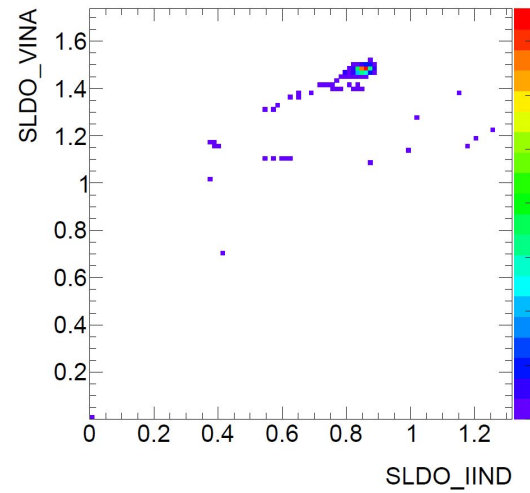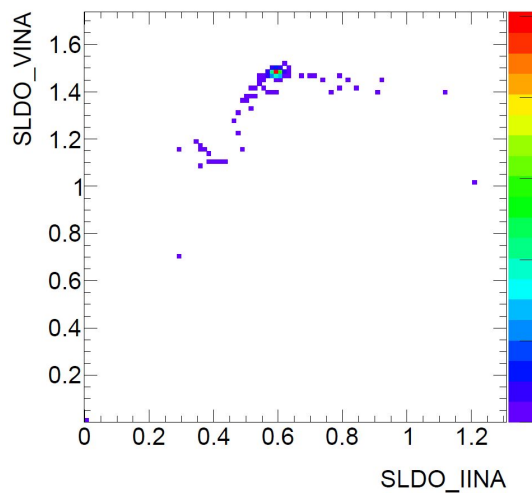- Checked correlation as well, as requested at the last discussion on December
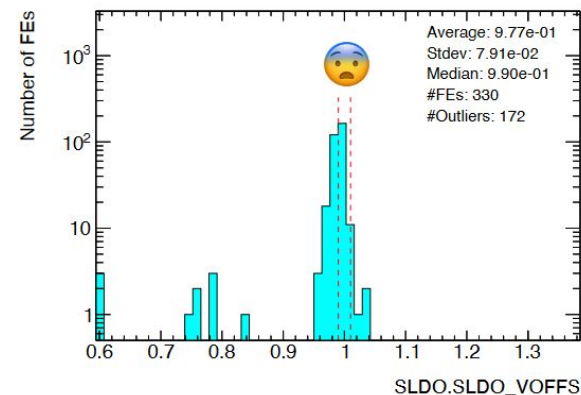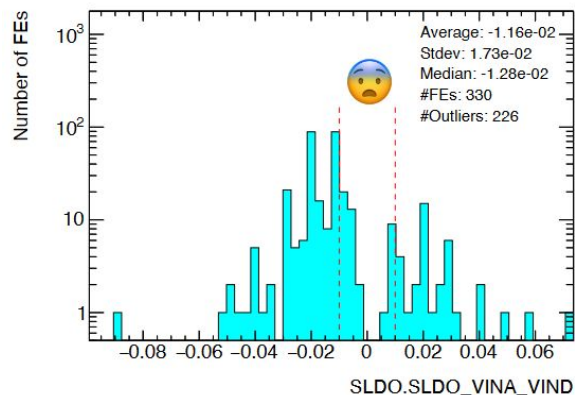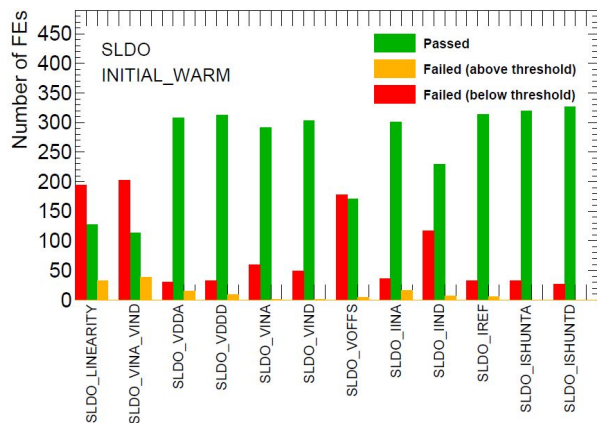


Plots from Hide's slides on 7th December

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# Yield in elec. QC: SLDO

- Retrieved linear correlation factors from each combination of the parameters
- Strong correlations among some of the parameters
  - Are we probably imposing redundant QC checks?
- Correlation between VinA/D and IinA/D: outliers has different correlations from the nominal ones?
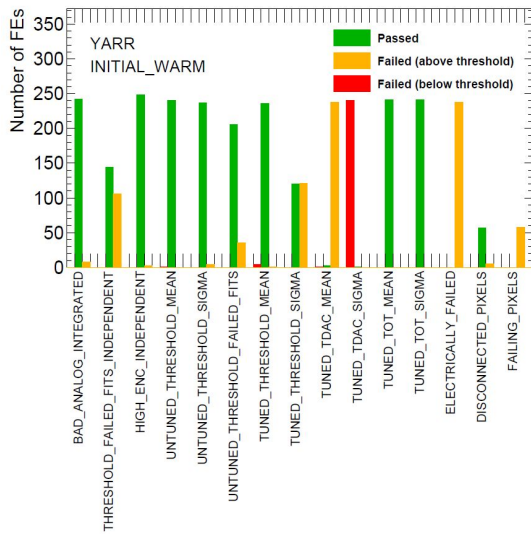
# Yield in elec. QC: LPM, OVP, USP

- Counted the numbers of passed/failed in each QC analysis
- No recent update as the tests with LP mode are currently suspended
  - Some follow-ups on the LP mode issue later
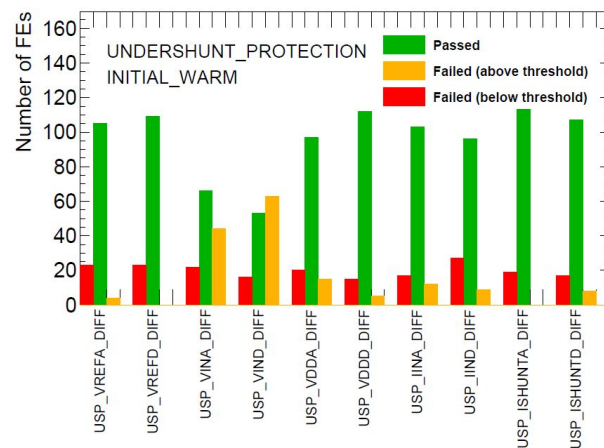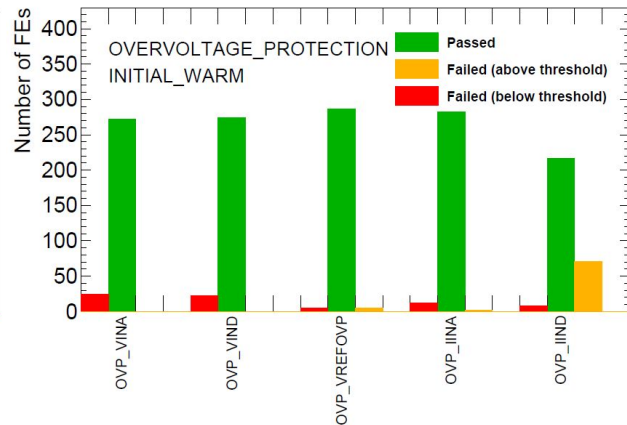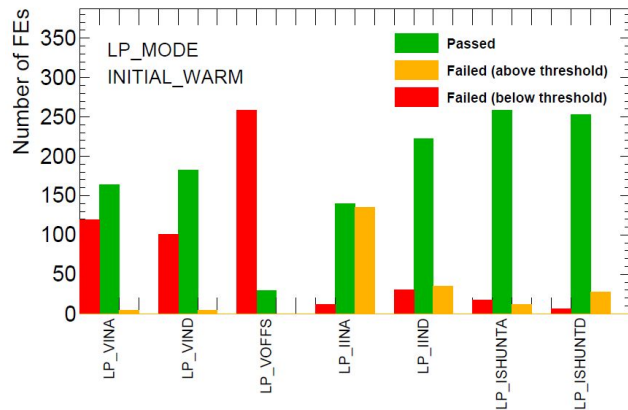
# Yield in elec. QC: MHT, TUN, PFA

- Many failures in tuning (as discussed on December) and PFA
  - As already discussed at the last meeting



| | INITIAL_WARM | INITIAL_COLD |
|---|---|---|
| Total # of FEs analysed | 237 | 224 |
| DEAD_DIGITAL | 17 | 4 |
| BAD_DIGITAL | 1 | 7 |
| DEAD_ANALOG | 17 | 10 |
| BAD_ANALOG | 12 | 10 |
| HIGH_ENC | 0 | 0 |
| HIGH_NOISE | 0 | 1 |
| MARGED_BUMPS | 0 | 1 |

Core column masks

Bad analog FEs on a line

Many noisy pixels

Detailed statistical analysis is underway to better identify origins of the failed pixels
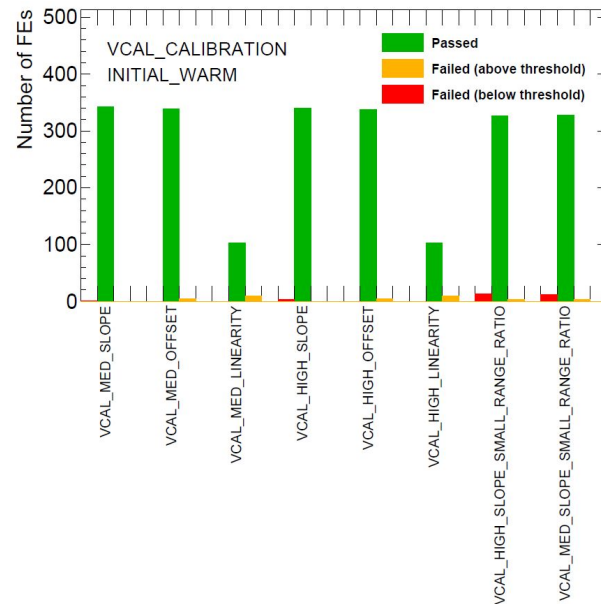
9
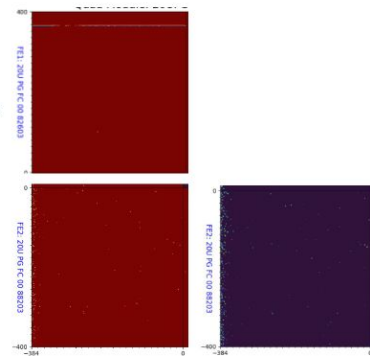
# Yield in elec. QC: other tests

- Good yields in ADC calibration, data transmission, injection capacitance and Vcal calibration
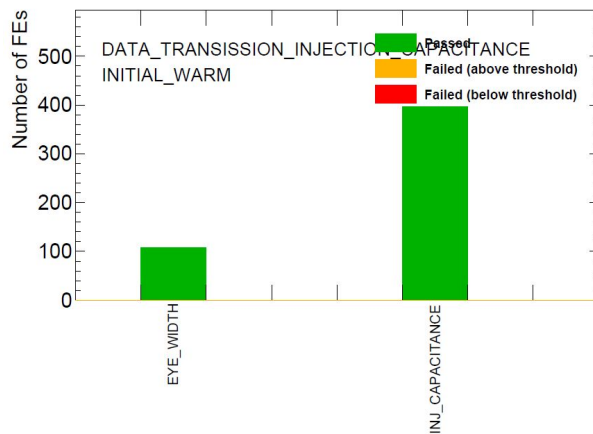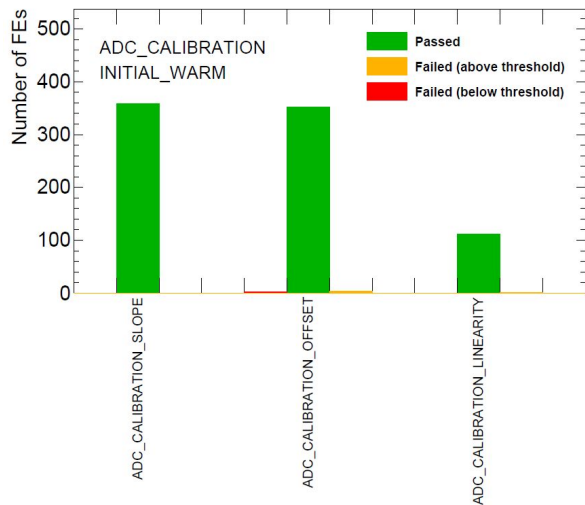
# LP mode issue

- After power cycle, there are some cases that a healthy module (i.e. which has good communication in the normal power mode) cannot be configured
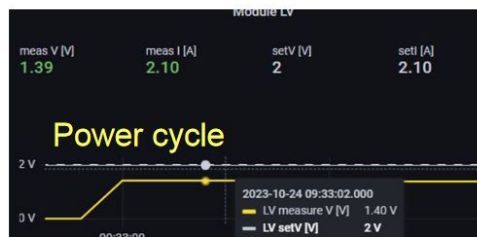- Investigated relation w.r.t. slew rate of the power supply



Plots from Hide's slides on 7th December

# LP mode issue

- Previously we used Mpod with slower slew rate
  - Decided to change it from 500 V/s to 3000 V/s
  - Early tests were done with 500 V/s
- First check: testing communication with power cycle at the firster slew rate
  - Chose a module with a good condition
  - Wasn't able to establish communication in LP mode after power cycle, while successful without power cycle



LowPower test w. power cycle (default setting)

```
[16:50:49:357][ info ][ ScanConsole ][13493]: ^[[1;31m#####################^[[0m
[16:50:49:357][ info ][ ScanConsole ][13493]: ^[[1;31m## Configure FEs ##^[[0m
[16:50:49:357][ info ][ ScanConsole ][13493]: ^[[1;31m#####################^[[0m
[16:50:49:378][ info ][ ScanConsole ][13493]: Configuring 0x15782
[16:50:49:668][ info ][ ScanConsole ][13493]: Configuring 0x1578a
[16:50:49:958][ info ][ ScanConsole ][13493]: Configuring 0x15762
[16:50:50:248][ info ][ ScanConsole ][13493]: Configuring 0x15777
[16:50:50:538][ info ][ ScanConsole ][13493]: Sent configuration to all FEs in 1180 ms!
[16:50:50:538][ info ][ ScanConsole ][13493]: Checking com 0x15782
[16:50:50:539][ info ][   SpecRx   ][13493]: Active Rx channels: 0x4
[16:50:50:539][ info ][   SpecRx   ][13493]: Active Rx lanes: 0x1
[16:50:50:539][ info ][   SpecRx   ][13493]: Rx Status 0x0
[16:50:50:539][ info ][   SpecRx   ][13493]: Number of lanes: 1
[16:50:50:539][ error ][   SpecRx   ][13493]: Channel 2 Lane 0 not synchronized!
[16:50:50:540][ error ][   Rd53b   ][13493]: Did not receive any data for 0x15782
[16:50:50:540][critical][ ScanConsole ][13493]: Can't establish communication, aborting!
```

LowPower test w/o power cycle

LP_MODE for 0x15782

| Parameter | Analysis result | QC criteria | Pass |
|---|---|---|---|
| LP_VINA | 1.482 | [1.468, 1.518] | True |
| LP_VIND | 1.482 | [1.468, 1.518] | True |
| LP_VOFFS | 1.308 | [1.304, 1.354] | True |
| LP_IINA | 0.23 | [0.18, 0.22] | False |
| LP_IIND | 0.32 | [0.28, 0.32] | True |
| LP_ISHUNTA | 0.0865 | [0.0001, 0.1] | True |
| LP_ISHUNTD | 0.0866 | [0.0001, 0.1] | True |

20UPGM22601103 chip1

# LP mode issue

- Would like to test the LP mode with a faster PS
  - A good candidate is RIGOL DP821A
  - Need arrangement to bring modules to KEK...
- Weird behaviour in Vin (as discussed on email) was due to a locally implemented switching to LP mode
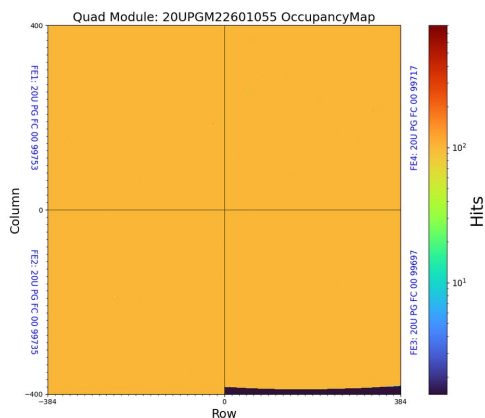  - Seems implemented just as a test mode; removed it and the behaviour has been fixed

# Bump disconnection

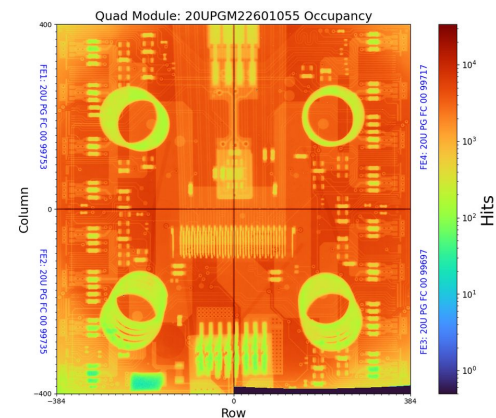- Disconnected bumps are evaluated using the three types of scans
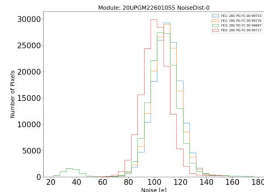
Noise from threshold scan (zero bias)
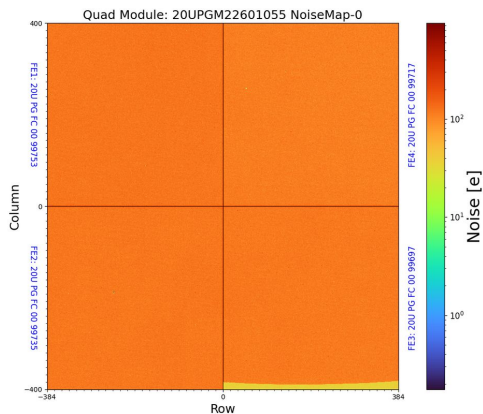
Occ. from disc. bump scan

Nhits from X-ray scan
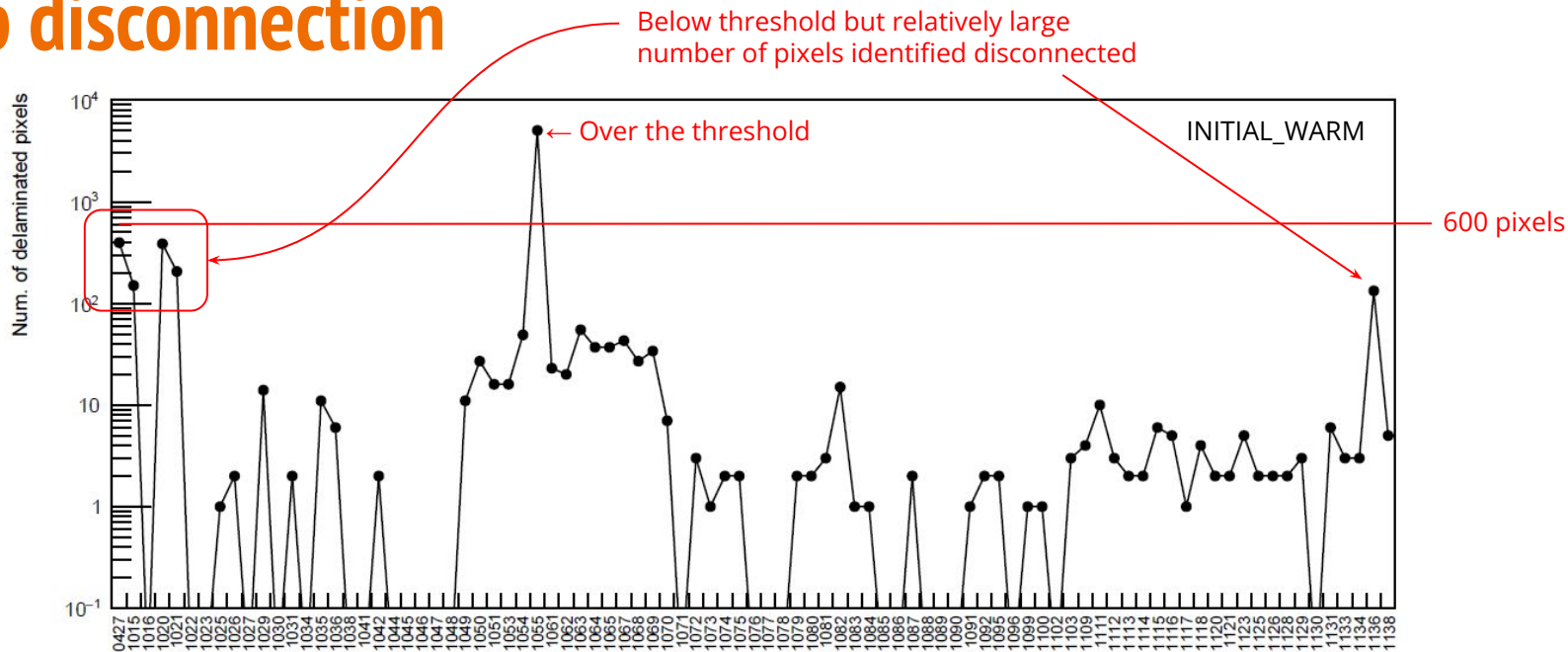


**Cond. for disc. bump:**
18.7e < noise < 56.7

**Cond. for disc. bump:**
Occ. < 50%

**Cond. for disc. bump:**
Nhits < 10

Note: pixels failing analog scans are excluded
→ Updating the algorithm to reply on pixel config.

# Bump disconnection



Below threshold but relatively large number of pixels identified disconnected

← Over the threshold

INITIAL_WARM

600 pixels

- AND of all the three types of scans
  - Observed 6 modules with some disconnection (out of them, 1 failed the threshold)

# Bump disconnection
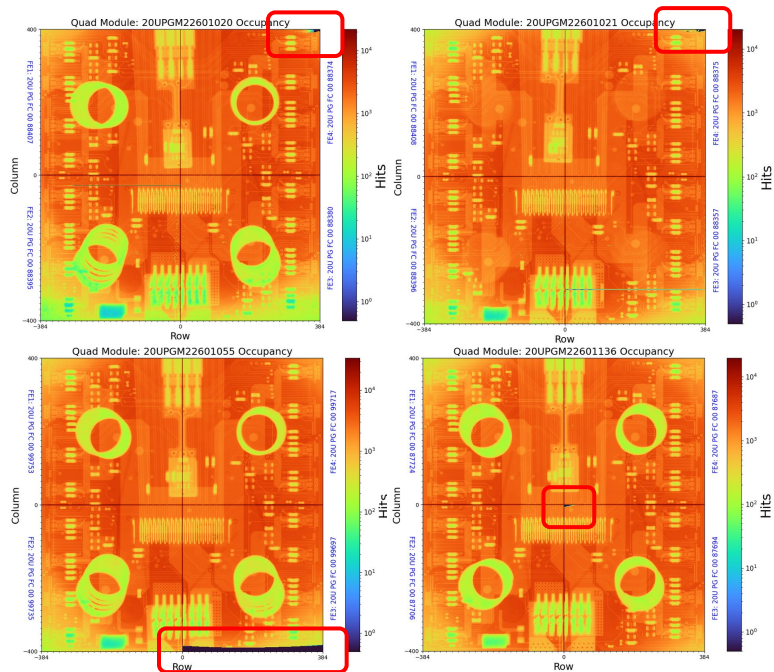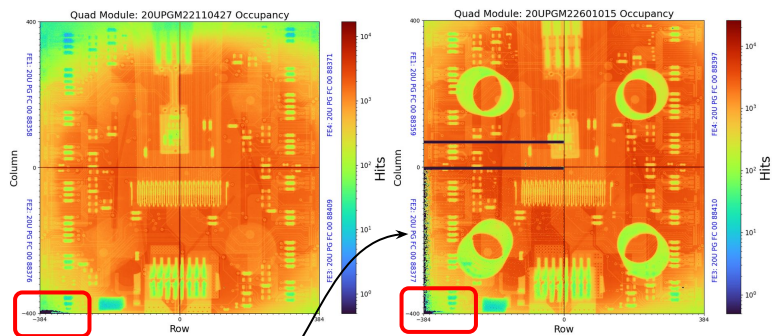


Tuning problem

- Observed 6 modules partly with disconnected bumps
  - 0427 FE2, 1015 FE2, 1020 FE4, 1021 FE4; these share the same dicing line → Potential cause in the dicing process identified, and confirmed that will not happen in the production
  - 1055 FE3, 1136 FE4: these chips are from the wafer edge → Known that bump formation is incomplete for these chips (so should not have been used…)
- All 6 cases have been understood, and feedback given to the manufacturers

# Comparison of bump evaluation methods
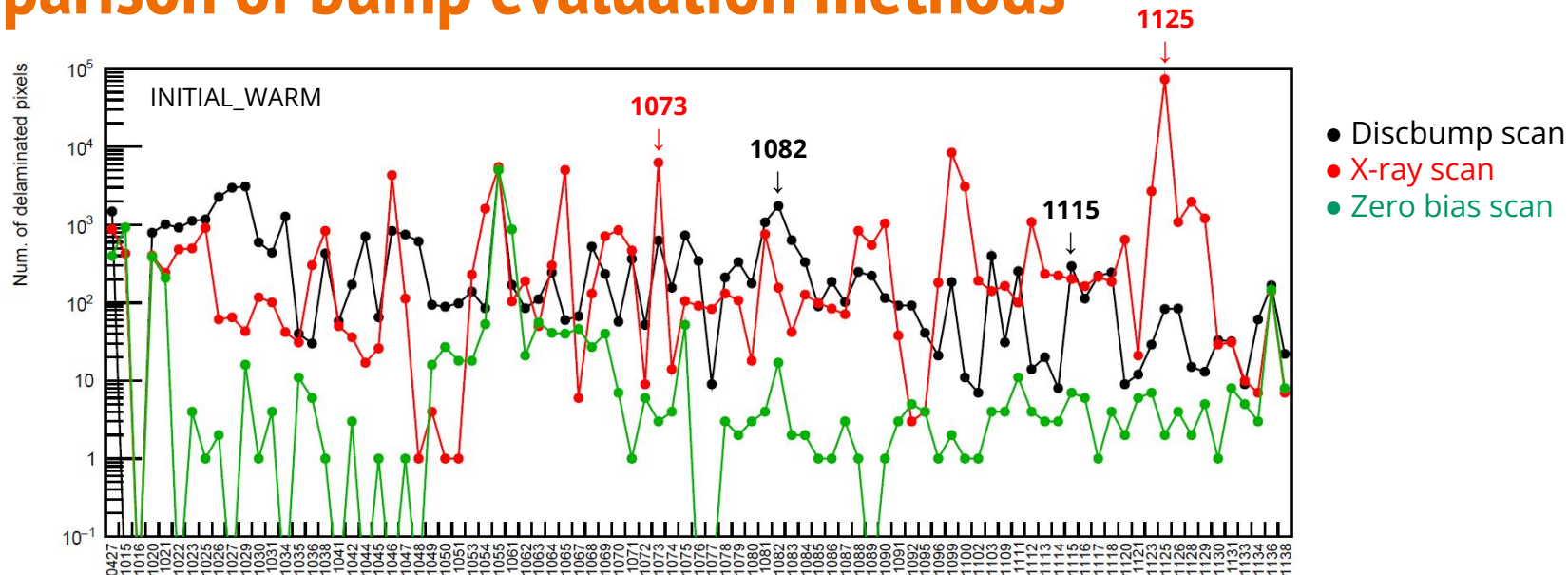


- Disconnected bump scan and X-ray scan show many 'disconnected' bumps
  - But probably that's not true, as the results from noise in zero bias scan are low
  - ...and we didn't see any delamination-like cluster of disconnected bumps in any of the 2D maps during elec. QC
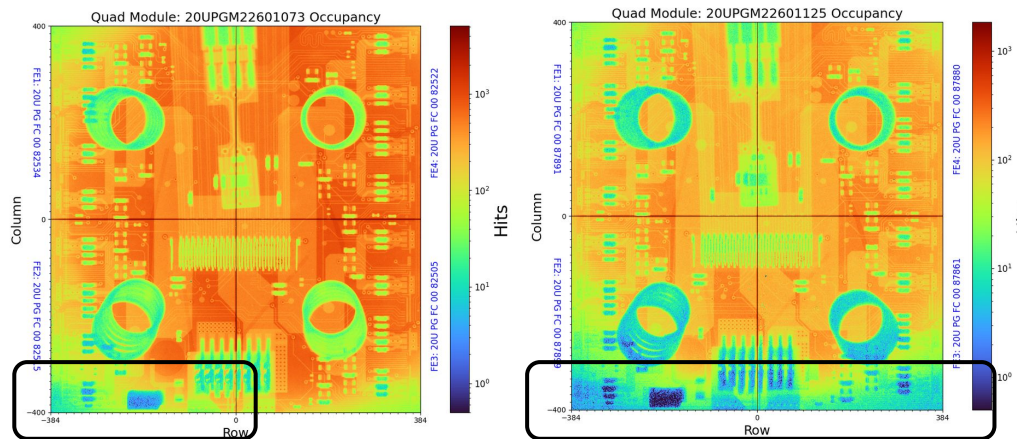
17

# Disconnected bump scan
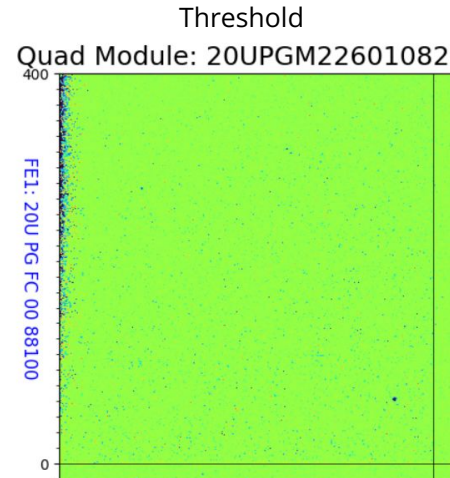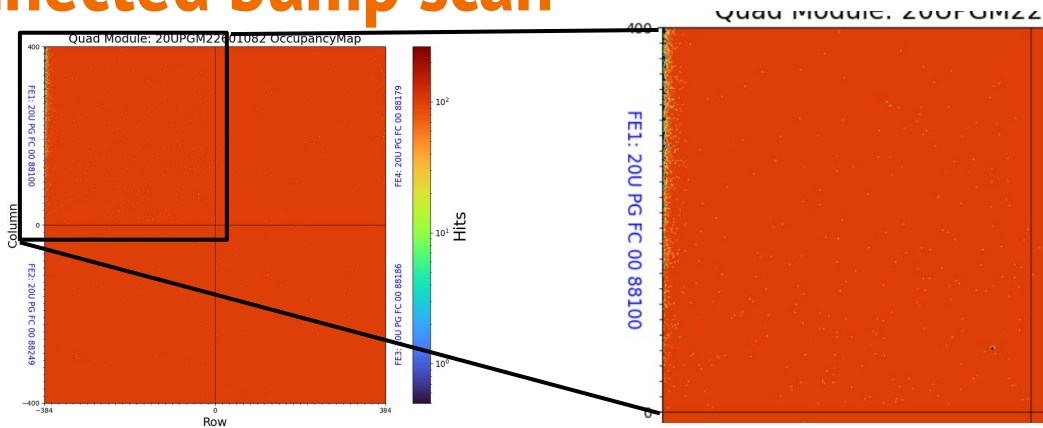


- There seems frequent cases where occupancy in discbump scan is low due to mis-tuned thresholds?
- Similar pattern observed even after LLC enabled
  - Though the effect is marginal…
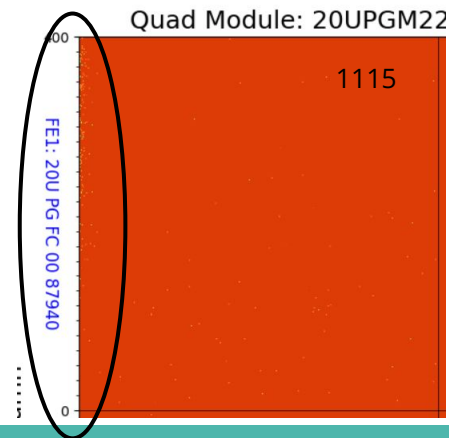
# X-ray scan



- Need enough irradiation on the HV capacitor
  - If the X-ray box is slightly tilted (upwards on these figures), then irradiation to the bottom part of the module may be slightly sparse
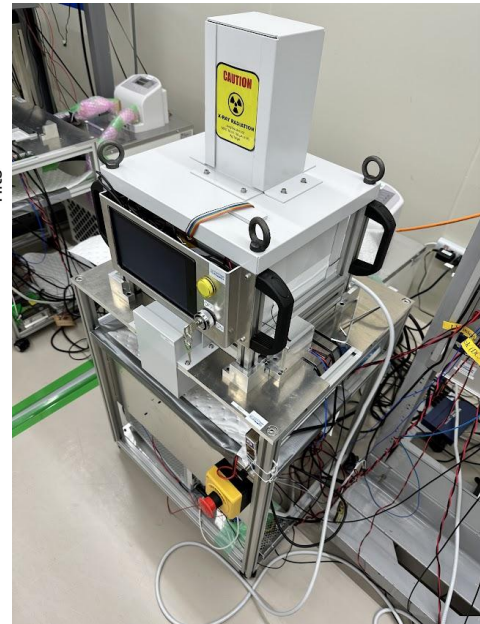
# Noise from zero bias scan

- Good separation between ASIC noise and module noise
  - Probably thanks to the slightly high noise in the HPK sensors



ASIC noise
(disconnected region)

Module noise
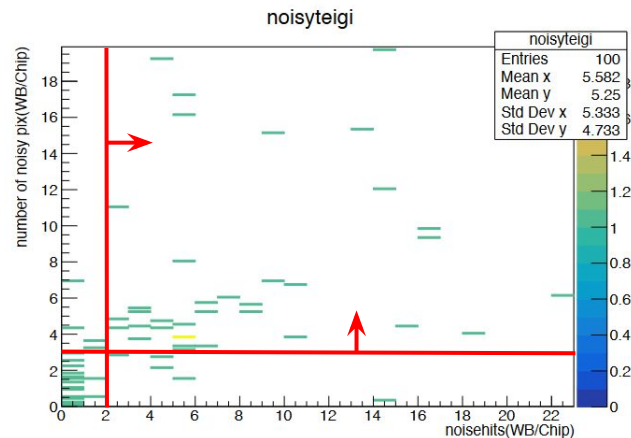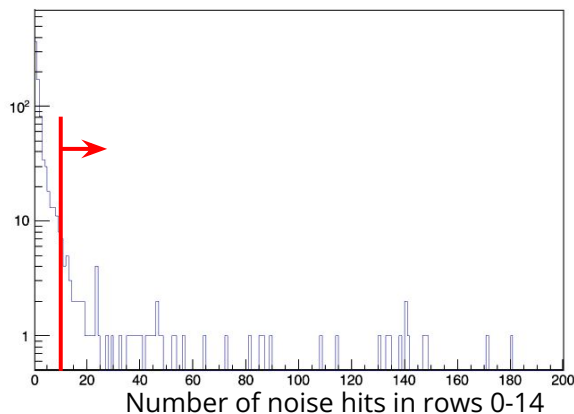$= \sqrt{(\sigma_{ASIC}^2 + \sigma_{sensor}^2)}$
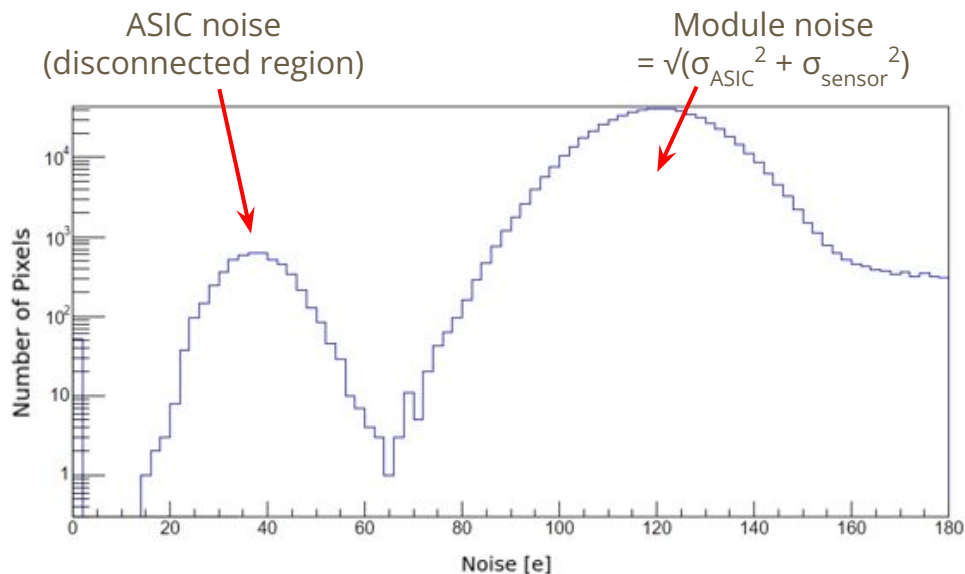
# Noise around WB pads (chip bottom)

- Some modules show high noise near the chip bottom
  - They are concentrated on around rows 0-14
- This feature may be correlated to mis-measurements in disconnected bump scan?
- Investigated effects of enabling LCC



Quad Module: 20UPGM22601023 Occupancy
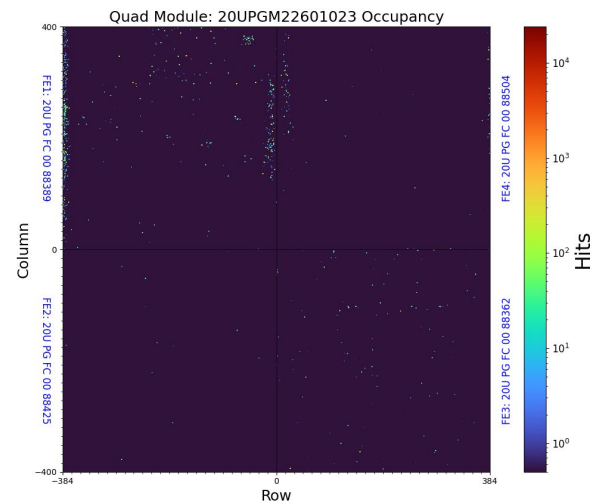
# Noise around WB pads (chip bottom)

- Define 'module with high noise around WB pads'
  - Consider rows 0-14 as 'around WB pads'
  - Number of noisy pixels (Nhit(rows 0-14) > 0 in noise scan) to be greater than 10
  - Fraction of noisy pixels in rows 0-14 to that in rows 15-383 to be greater than 4
  - Fraction of Nhit in rows 0-14 to that in rows 15-383 to be greater than 2
- Very preliminary selection, but seems not so bad...



Number of noise hits in rows 0-14



noisyteigi

| noisyteigi | |
|---|---|
| Entries | 100 |
| Mean x | 5.582 |
| Mean y | 5.25 |
| Std Dev x | 5.333 |
| Std Dev y | 4.733 |

# Noise around WB pads (chip bottom)

| (INITIAL_WARM) | LCC off | LCC on |
|---|---|---|
| Num. of chips tested | 310 | 60 |
| Num. of noisy chips | 17 | 0 |
| Fraction | 5.5% | 0.0% |
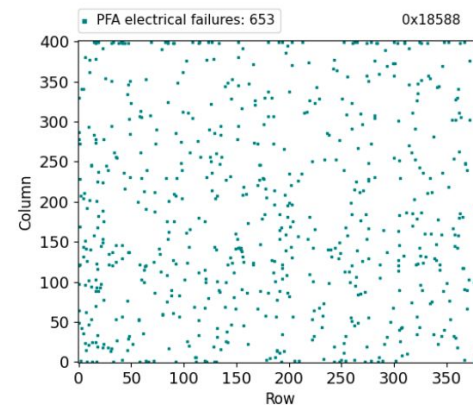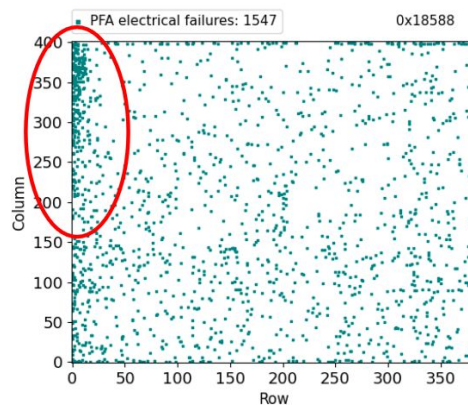


- So far we observed no 'noisy' module after enabling LCC by default
  - Good indication of effectiveness of the LCC
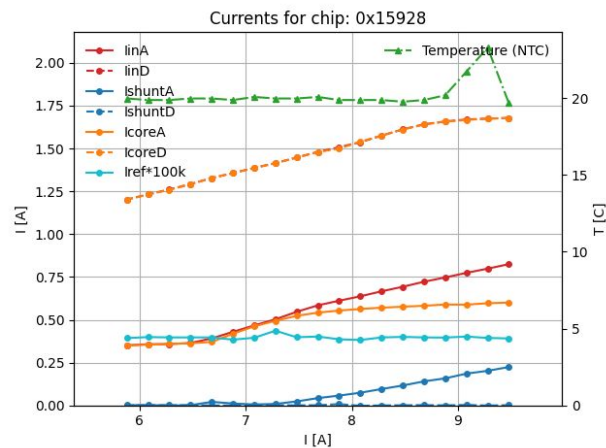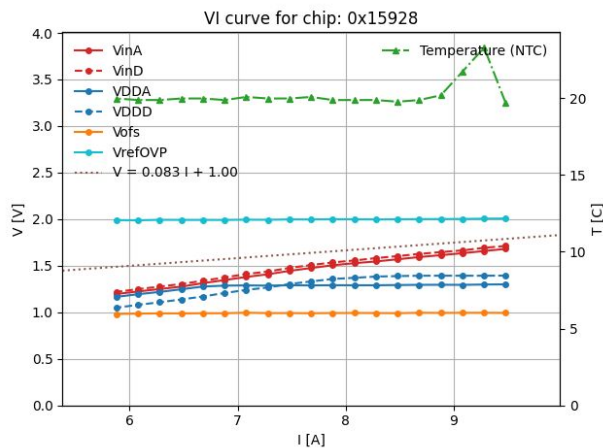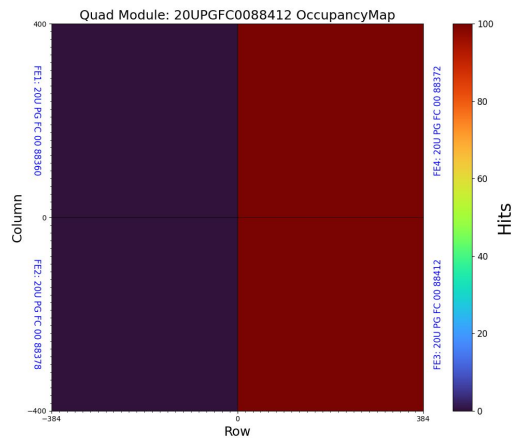- Will check also results from the cold tests too

# 20UPGM22601015

Failed tuning at FE2
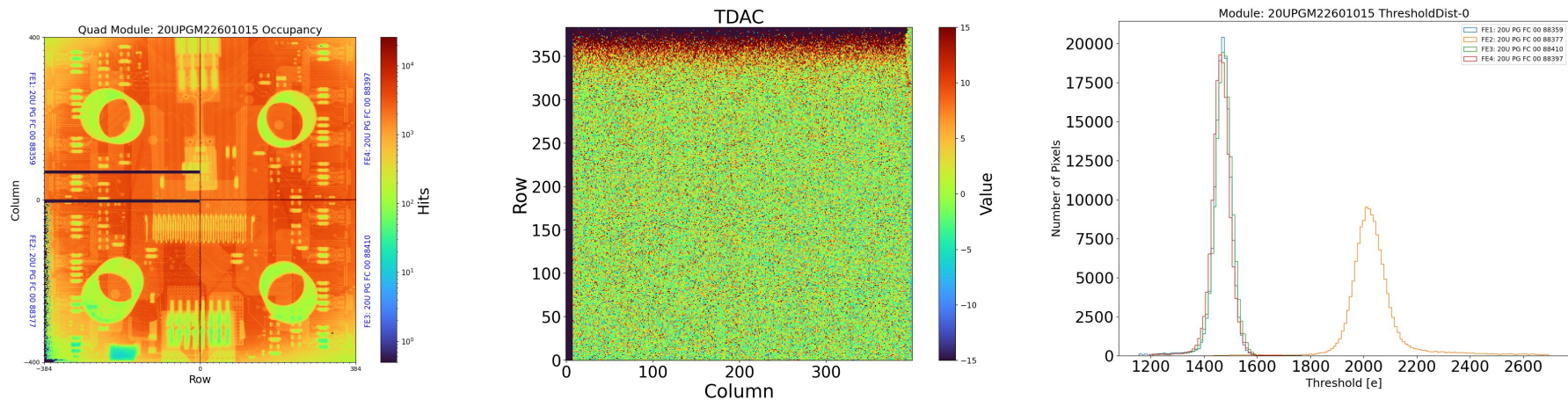
# 20UPGM22601016

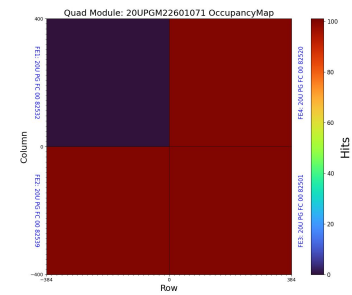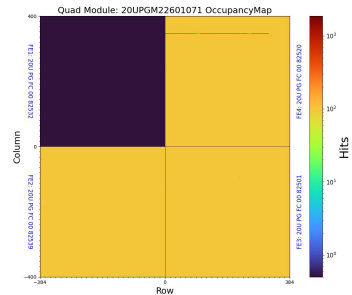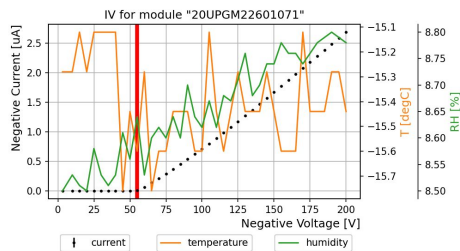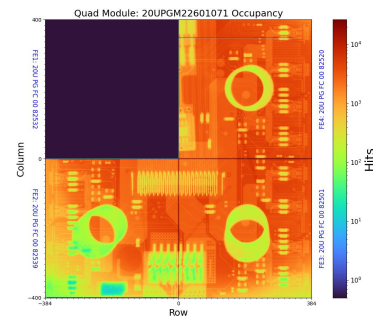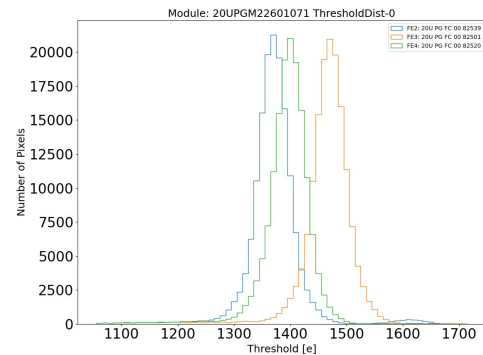FE1 and 2 disabled (FE1 has a problem on SLDO results)

# 20UPGM22601071

chip 1 disable → **コミュニケーションとれず**

- INITIAL_WARMではEnCoreCol2: 0011 1111 1111 1111
- INITIAL_COLDでchip 1がdisableされている

chip 3のthreshold高め

Chip 4: analogが一部読めてない
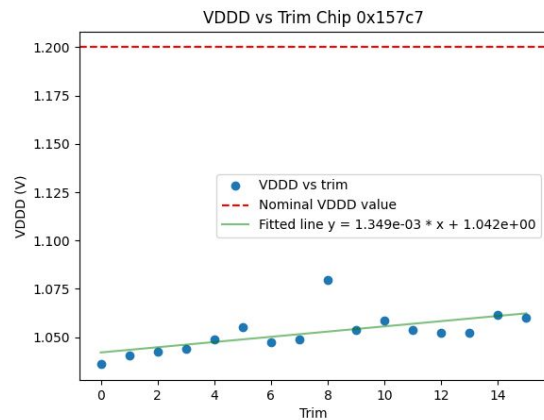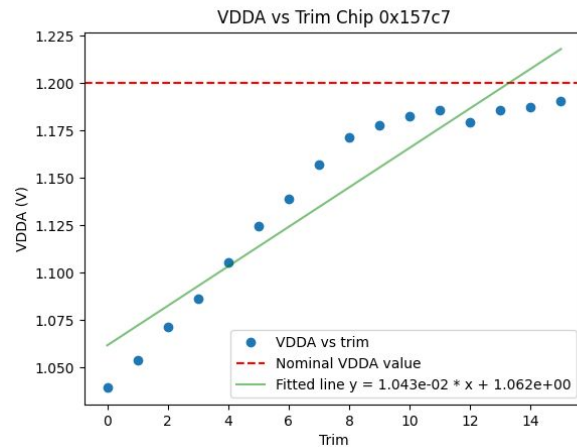
IV break at ~60 V

# 20UPGM22601094

Chip 4 EnCoreColumn2: 1111 1110 0111 1111
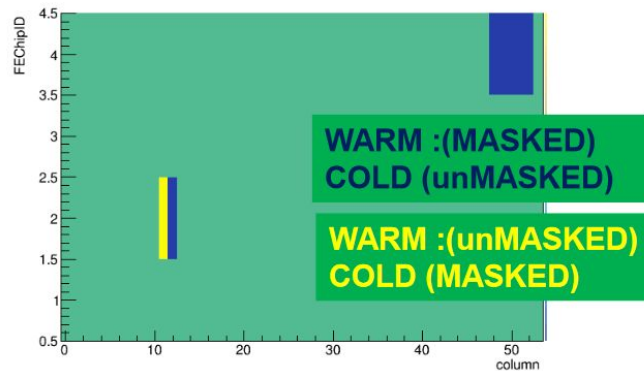
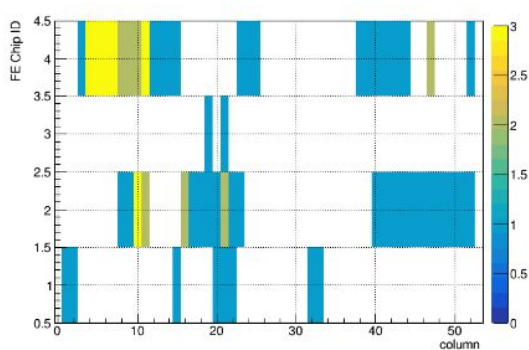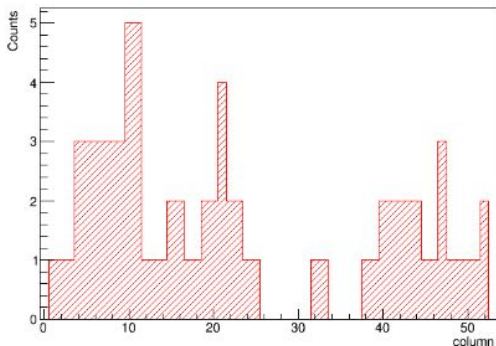Chip 4のVDDA/Dの出力が1.2 Vに達しない
→ failの理由

# CoreColumn mask

- Some problematic FEs disturb communication
  - Communication can be established by masking a (few) core column(s)
- 40 out of 744 [FEs*(initial_warm or initial_cold)] have at least one core columns masked
  - Slightly high in FE2 and FE4?



**WARM_CONFIG**

**CoreColm [colmn/4]**

# Cooling box



- For OE modules, thermal contact is not very robust
    - Cooling head directly contacts the ASIC side
    - Try to push the module with springs