BISv2 CIBF Reliability Study

Quantitative summary of the FMECA



List of contents

- 1. Preliminary results
- 2. Distribution of component types and locations
- 3. Failure rate prediction statistics
- 4. Failure effects per design location
- 5. Causes of false dumps



Reliability Targets CIBU (indicative)

End Effect	Target reliability FITS
Blind Failure (per channel)	100
Blind Failure (both channels, i.e., A/B)	0.05
False Dump	70

Approach

The approach applied for other BISv2 boards was based on a thorough balancing of individual targets for each board type so that **together they meet the overall goal**. The overall target for the entire system is **1 critical failure in 1,000 years** (risk matrix). Based on the:

- approximate complexity,
- number of boards' instances,

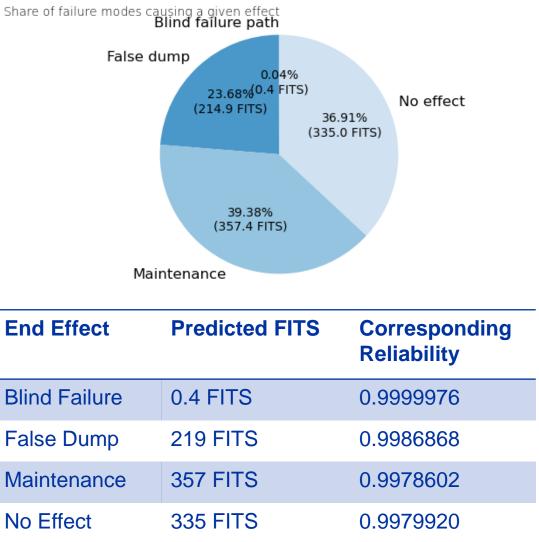
We reach the reliability targets presented above.



Preliminary results

- Relatively small fraction of blind failures – 0.04%
 - ✓ 0.4 FITS = 1 failure every 285,388 years
- False dumps similar to the numbers in other boards 24%
 - ✓ 215 FITS = 1 failure every 531 years
 - ✓ Still beyond requirements, but MIL-HDBK-217 estimates generally conservative
- Maintenance 39%
 - ✓ 357 FITS = 1 failure every 320 years
- 37% of failure modes have no impact
 - ✓ 335 FITS







Blind Failures

- CIBF 2 failure modes:
 - Components IC2 and IC19 (FOD060L): optocouplers stuck low in User Permit A/B;
 - Components IC3 and IC21 (74LVT14D): inverter stuck high in User Permit A/B;

• CIBU:

•

- Same for user permit optocoupler and inverter (although "stuck high/low" mismatch + an additional "input open" inverter)
- Additional blind failure on RS-485 transceiver on input open (to CIBM)
 - Fail-safe property of RS-485

Reliability Monitoring Results

Quarters: Q1/2022 to Q4/2022

Based on structural similarity

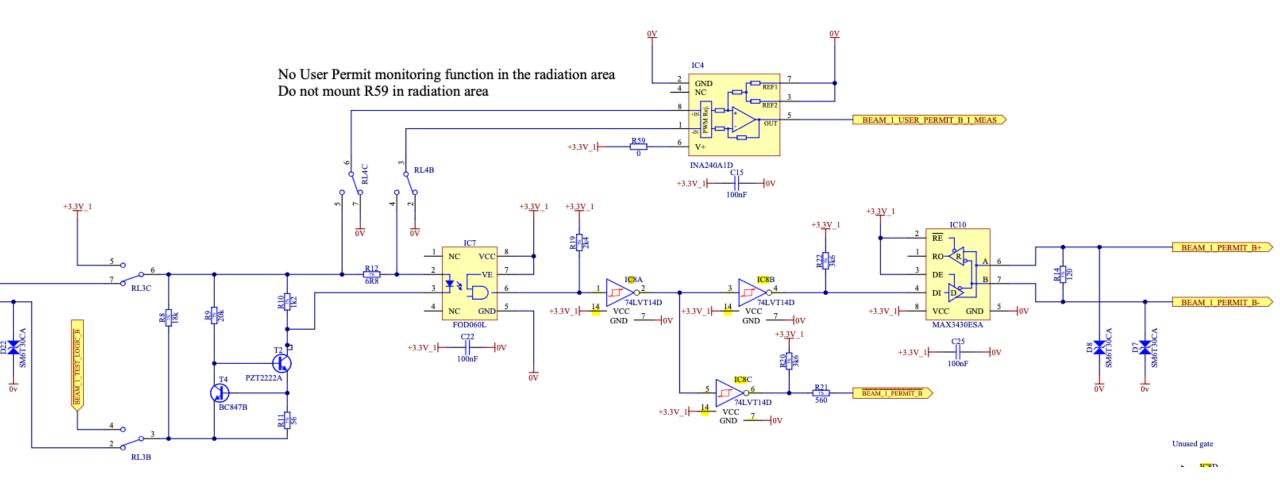
Supplie	er	User Part Number				
Nexperia	a B.V.	74LVT14D				
Fun Proc	escription: Hex inverter So ction Family: LVT cess family: Sub micron kage family: SO	hmitt-trigger				
JESD47	7 Test	Test Conditions	Duration	# Lots	# Quantity	# Rejects
# 1	TEST Pre- and Post-Stress Electrical Test	Tamb = 25 °C	N/A	see below	all parts	see below
# 2	PC Preconditioning	JESD22-A113 MSL 1	N/A	460	29380	0
# 5a	HTOL EFR High Temperature Operating Life Extrinsic	JESD22-A108 Tj = 150°C $V_{CCMAX} \le V \le 1.2*V_{CCMAX}$	48 hours or 168 hours	132	33268	0
# 5b	HTOL IFR High Temperature Operating Life Intrinsic	JESD22-A108 Tj = 150°C $V_{CCMAX} \le V \le 1.2*V_{CCMAX}$	≥500 hours	89	7065	0
# 7	TC Temperature Cycling	JESD22-A104 -65 °C to 150°C	≥500 cycles	69	17630	4
# 9	uHAST / HAST unbiased or biased High	JESD22-A101 Tamb = 130 °C,	96 hours	202	11750	0

nexperia

https://assets.nexperia.com/documents/quality-document/74LVT14D_Nexperia_Product_Reliability.pdf

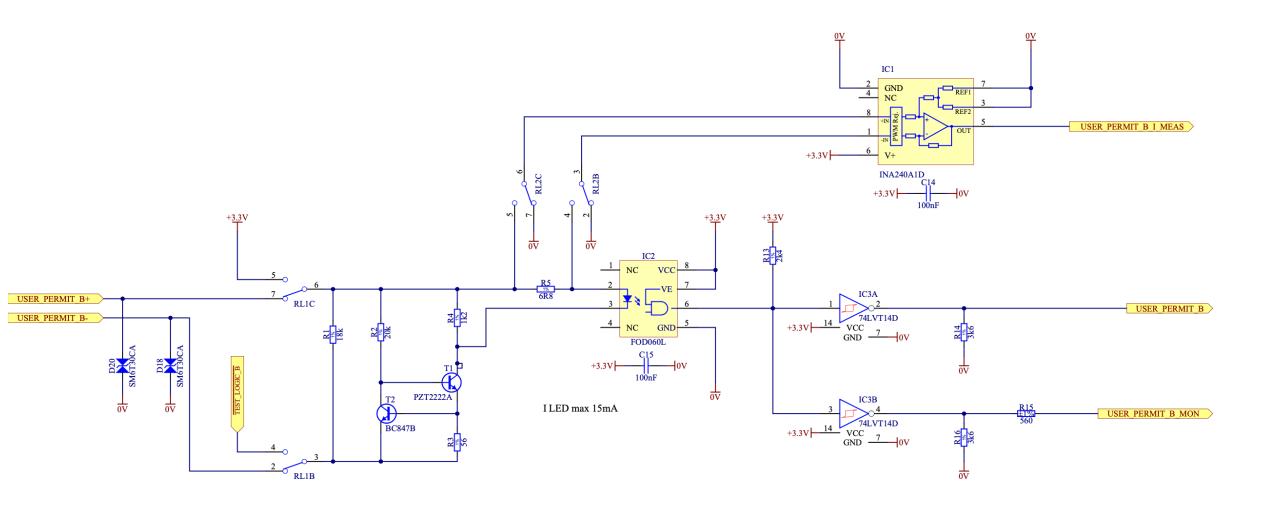


CIBU





CIBF





Blind Failures

• 2 failure modes:

- Components IC2 and IC19 (FOD060L): optocouplers stuck low in User Permit A/B;
 - failure rate: 0.13 FITS (10% of total 1.38 FITS assigned to the component from 217Plus standard)
 - Between 8 (35°C, 90% CL) to 39 FITS (55°C, 90% CL)
- Components IC3 and IC21 (74LVT14D): inverter stuck high in User Permit A/B;
 - failure rate: 0.05 FITS (10% of total 0.5 FITS from the producer).
 - Alternative: up to 8 FIT.

CERN

ne<mark>x</mark>peria

Reliability Monitoring Results

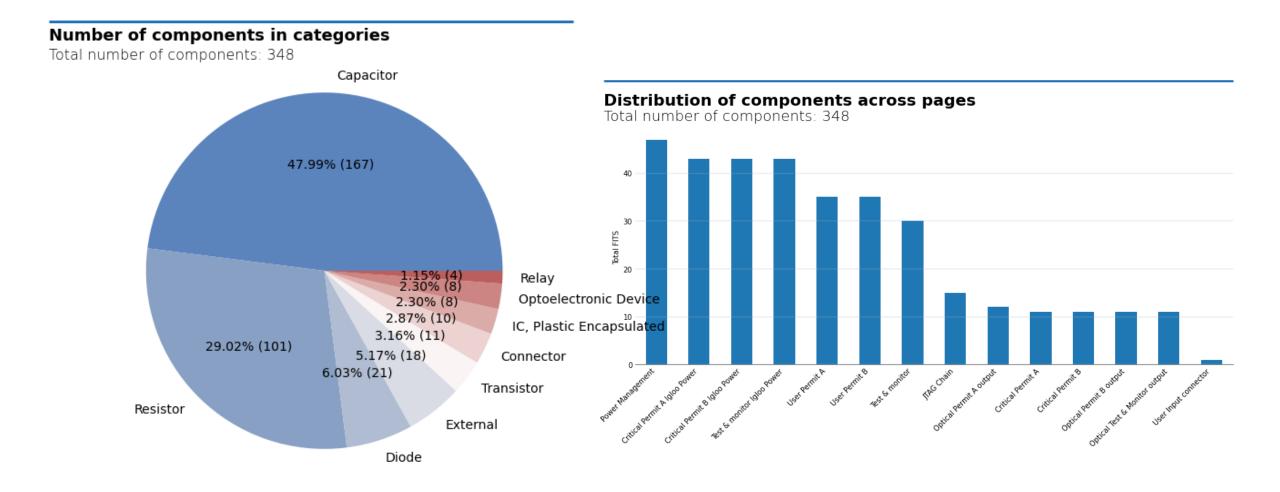
Quarters: Q1/2022 to Q4/2022

Based on structural similarity

Supplie	er	User Part Number					
Nexperia	B.V.	74LVT14D					
Fund Proc	escription: Hex inverter So ction Family: LVT cess family: Sub micron kage family: SO	hmitt-trigger					
JESD47	7 Test	Test Conditions	Duration	# Lots	# Quantity	# Rejects	
# 1	TEST Pre- and Post-Stress Electrical Test	Tamb = 25 °C	N/A	see below	all parts	see below	
# 2	PC Preconditioning	JESD22-A113 MSL 1	N/A	460	29380	0	
# 5a	HTOL EFR High Temperature Operating Life Extrinsic	JESD22-A108 Tj = 150°C $V_{CCMAX} \le V \le 1.2*V_{CCMAX}$	48 hours or 168 hours	132	33268	0	
# 5b	HTOL IFR High Temperature Operating Life Intrinsic	JESD22-A108 Tj = 150°C $V_{CCMAX} \le V \le 1.2*V_{CCMAX}$	≥500 hours	89	7065	0	
# 7	TC Temperature Cycling	JESD22-A104 -65 °C to 150°C	≥500 cycles	69	17630	4	
# 9	uHAST / HAST unbiased or biased High Accelerated Stress Test	JESD22-A101 Tamb = 130 °C, PH = 85% V = Variant	96 hours	202	11750	0	

https://assets.nexperia.com/documents/quality-document/74LVT14D_Nexperia_Product_Reliability.pdf

Distribution of component types and locations

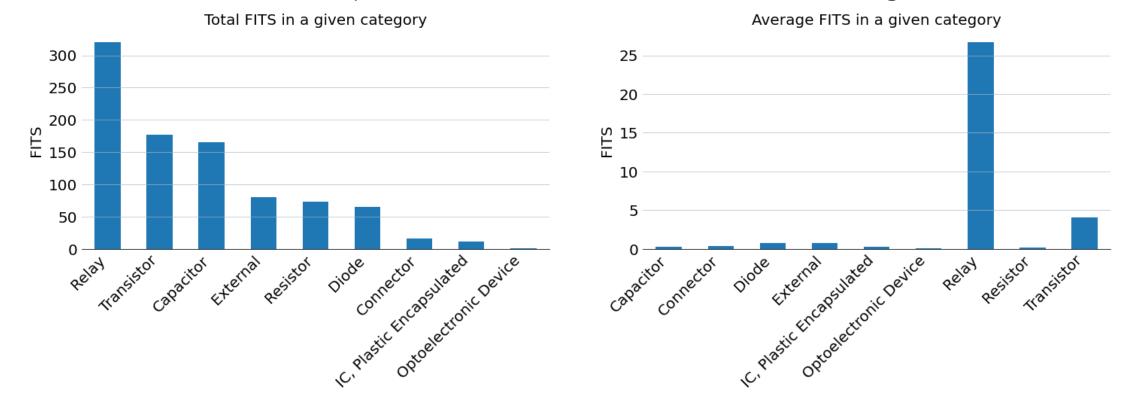




Failure rate prediction - statistics

FITS of component categories

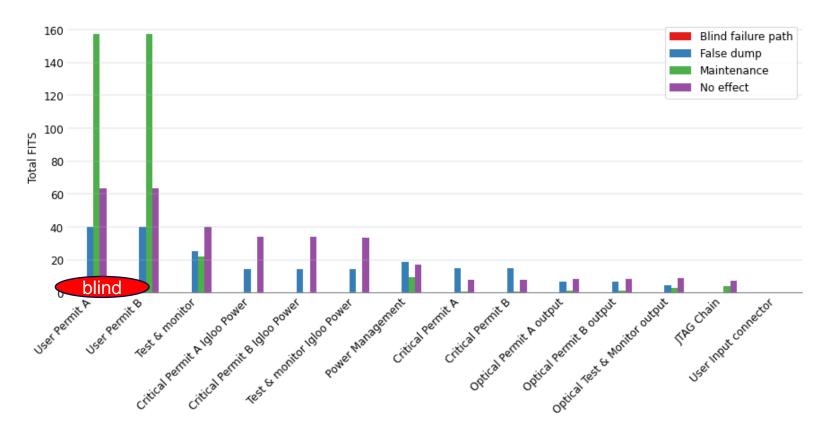
Distribution of number of predicted failures in **10⁹** hours across categories





Failure effects per design location

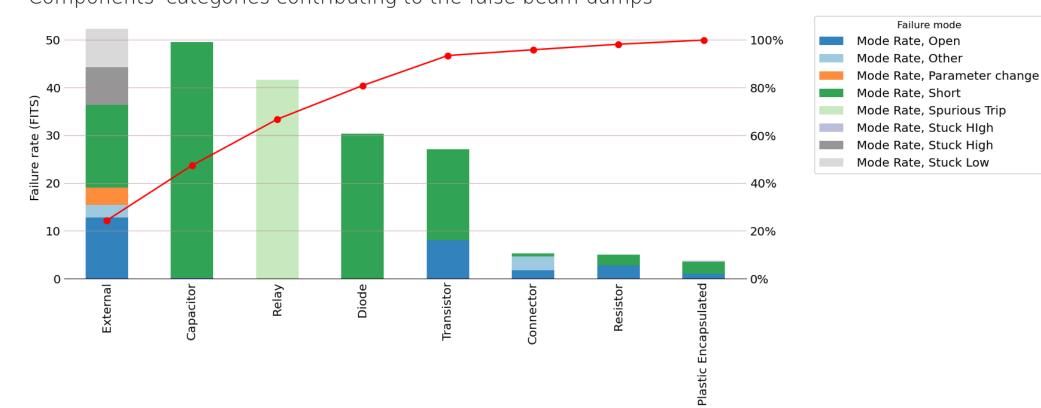
FITS of design pages Predicted number of failures in 10⁹ hours





Causes of false dump failures

Group contributors to false beam dumps Components' categories contributing to the false beam dumps



Ú





> SFP

A "daughter board" to be included in the FMECA. EDA-04670-V1.

Global model

As the study of the entire BISv2 system nears completion.

> CIBDS

The next board in the BISv2 study





home.cern