BISv2 CIBDS Reliability Study

Top-level functions, functional diagram, FMECA

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Top level functions
Overview

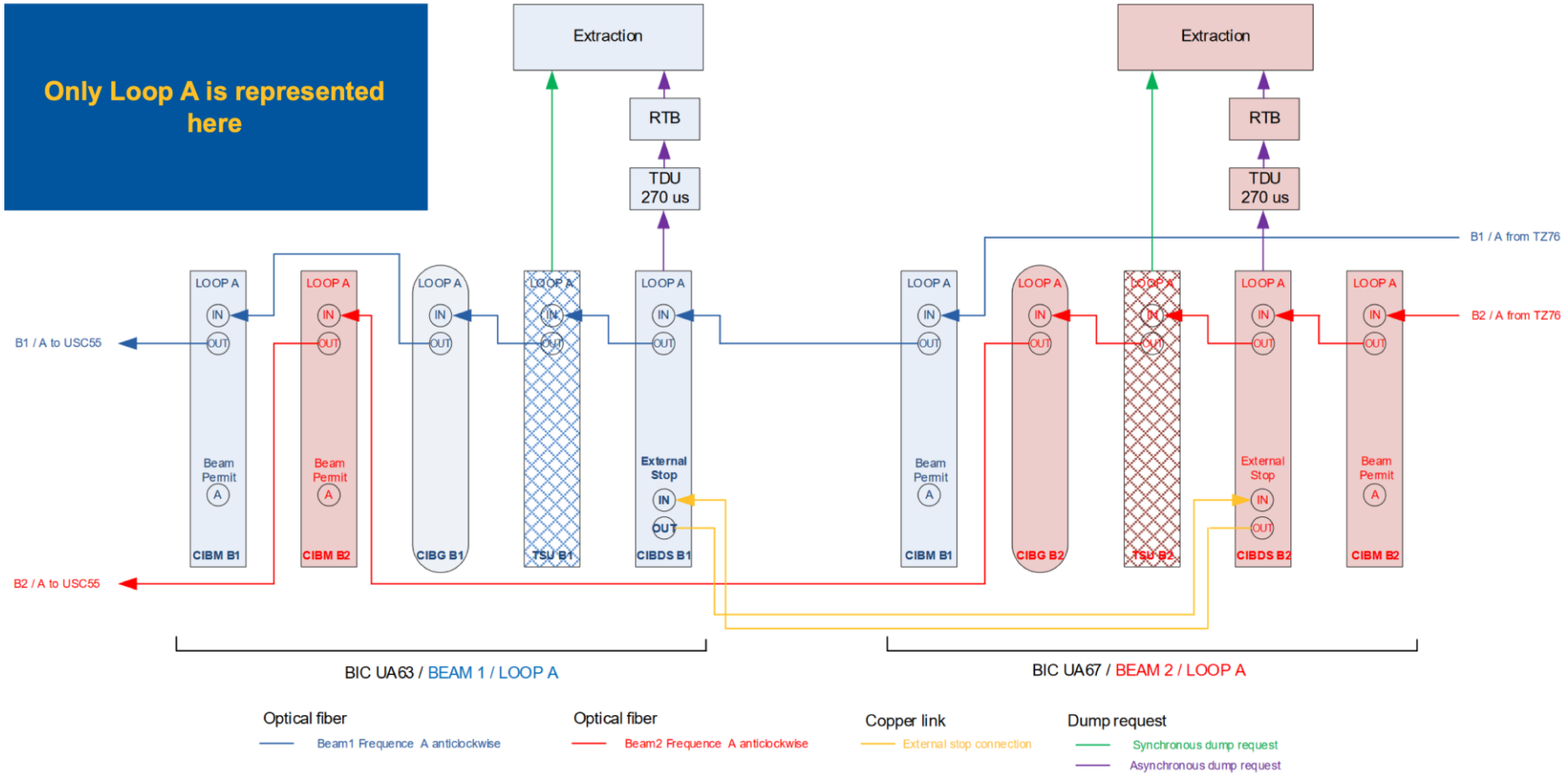
- **Main – critical:** sending asynchronous dump request to the TDU (Trigger Delay Unit)
- **Link Mode:** dumping the second beam depending on the status of an SMP flag.
- **Secondary**:
  - sending synchronous dump request to ???
  - Arming process.
- **Diagnostics.**

Top-level functions FMECA

Situation	Function	Failure	Effect	Criticality
Normal operation	Keep the BIS loop closed	Opening the beam permit loop	Downtime	
		Spurious trigger	Asynchronous dump, downtime	
		Assuming the LBDS is in the LOCAL mode while it is in REMOTE (failure of path A and B)		
The beam is being dumped	Regonize change or lack of signal and send an asynchronous dump request	Not sending an asynchronous dump request	Downtime	
			If TSU not dumping the beam and it CIBDS both A and B paths fail then missed beam dump	
The other beam dumped	Depending on the link mode flag status, removing beam permit and sending a delayed asynchronous dump request	Not removing the beam permit	Beam remains in the machine and does not have beam-beam kick effect (both A and B paths failing)	
		Not sending a delayed asynchronous beam request		
Arming	Check status and confirm readiness	Unable to arm when conditions allow	Downtime	
		Arming when conditions not allow	Risk of being unable to dump asynchronously when needed	
Diagnostics	Collect diagnostics data and send to Post-Mortem	Lack of diagnostic data	Downtime	

CIBDS in the BIS loop

Schema from the BISv2 developments for LS3 presentation

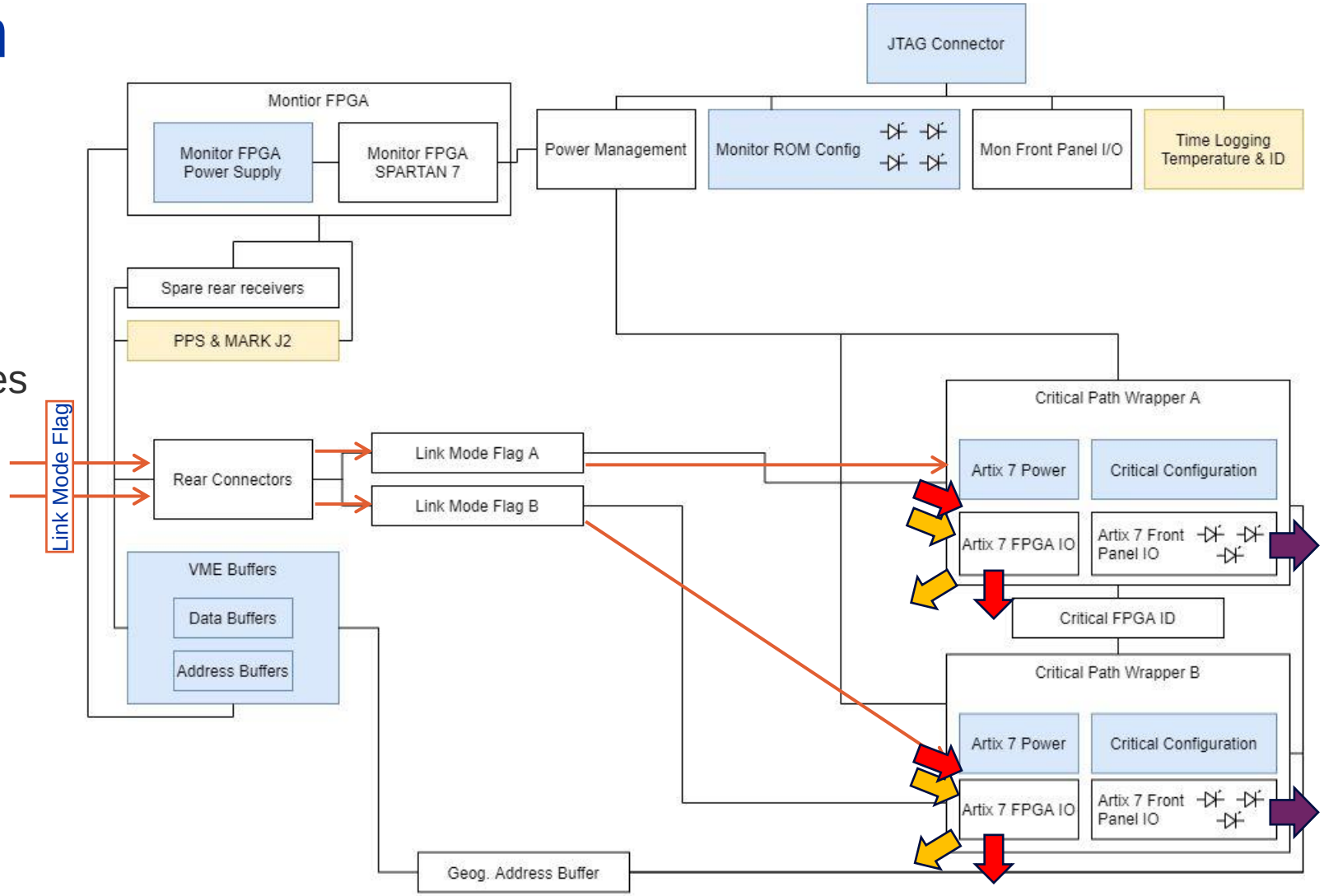


https://indi.to/KWLHR, I. Romera Ramirez

Functional Block Diagram
Elements of the design

The blue and yellow boxes indicate pages which are listed as ”unmodified”.

Missing input and output flows.



Component-level FMECA
Concept

What is FMECA?

- Each component is assigned failure rate prediction from 217 Plus standard, applicable failure modes and their share of the failure mode
- Each failure mode is to be assigned one of the end-effects listed to the right

End-effects:

- ~~Blind failure (whole board)~~
- ~~Blind failure (per path)~~
- ~~False dump (asynchronous)~~
- ~~False dump (synchronous)~~
- ~~Maintenance~~
- ~~No effects~~

Designator	Description	Part Number	Category	Page	Failure mode	Failure rate	End Effect
C1	10% 50V X7R…	CC0603…	Capacitor	CRITICAL_CONFIG	Open	0.02	No Effect
C1	10% 50V X7R…	CC0603…	Capacitor	CRITICAL_CONFIG	Short	0.1	Beam dump
…							
IC4	IttyBitty	MIC15…	Integrated Circuit	CRITICAL_CONFIG	Short	0.98	Beam dump
…							

Questions
For failure rate prediction

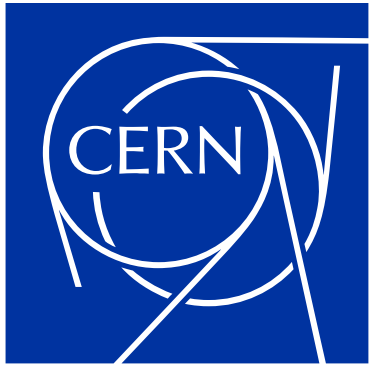
1. Is the transistors' applied voltage always equal to 3V?

2. "Quad Channel Optocoupler, Phototransistor Output": assigned category "IC, Plastic Encapsulated"; type: linear?

3. The derating of the capacitors is much lower than in other boards. Still, maximum up to values above 50%.

4. "High speed switching diodes" assigned type "Current regulator".

Firmware reliability assurance



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