

CIBAB Study Kick-off meeting

BISv2 Reliability Study Progress Meetings

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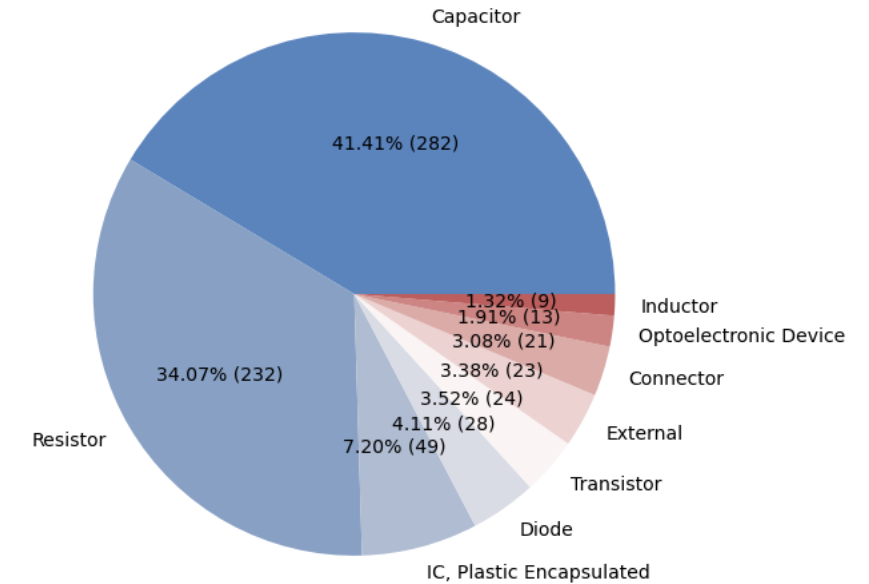
Failure rate prediction results

General statistics

- **681 components across 31 pages**
 - Isograph count is 731 due to dual transistors
- **Identified operating voltage for 263 mounted capacitors**
 - Remaining 19 were assumed the default 3.3V.
 - All below 50% - with 42 capacitors close to that value.

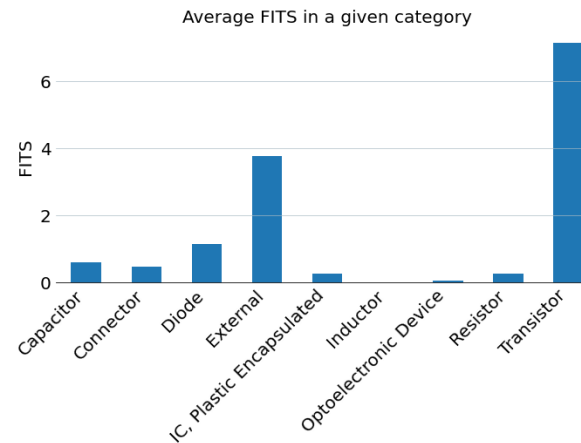
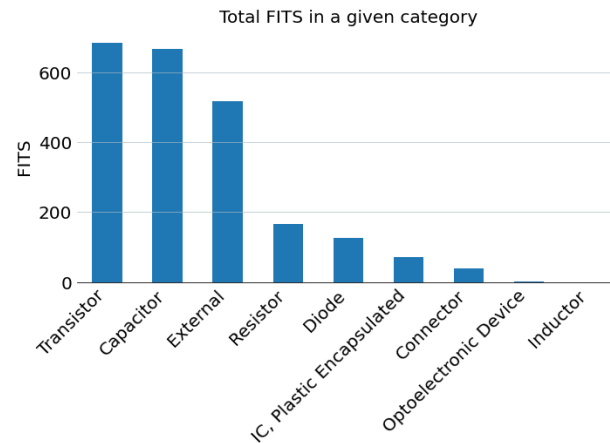
Number of components in categories

Total number of components: 681



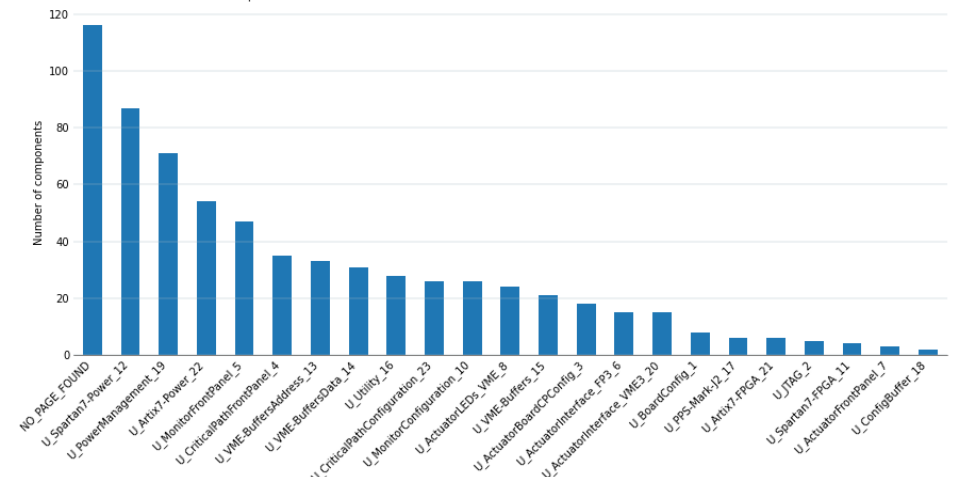
FITS of component categories

Distribution of number of predicted failures in 10^9 hours across categories



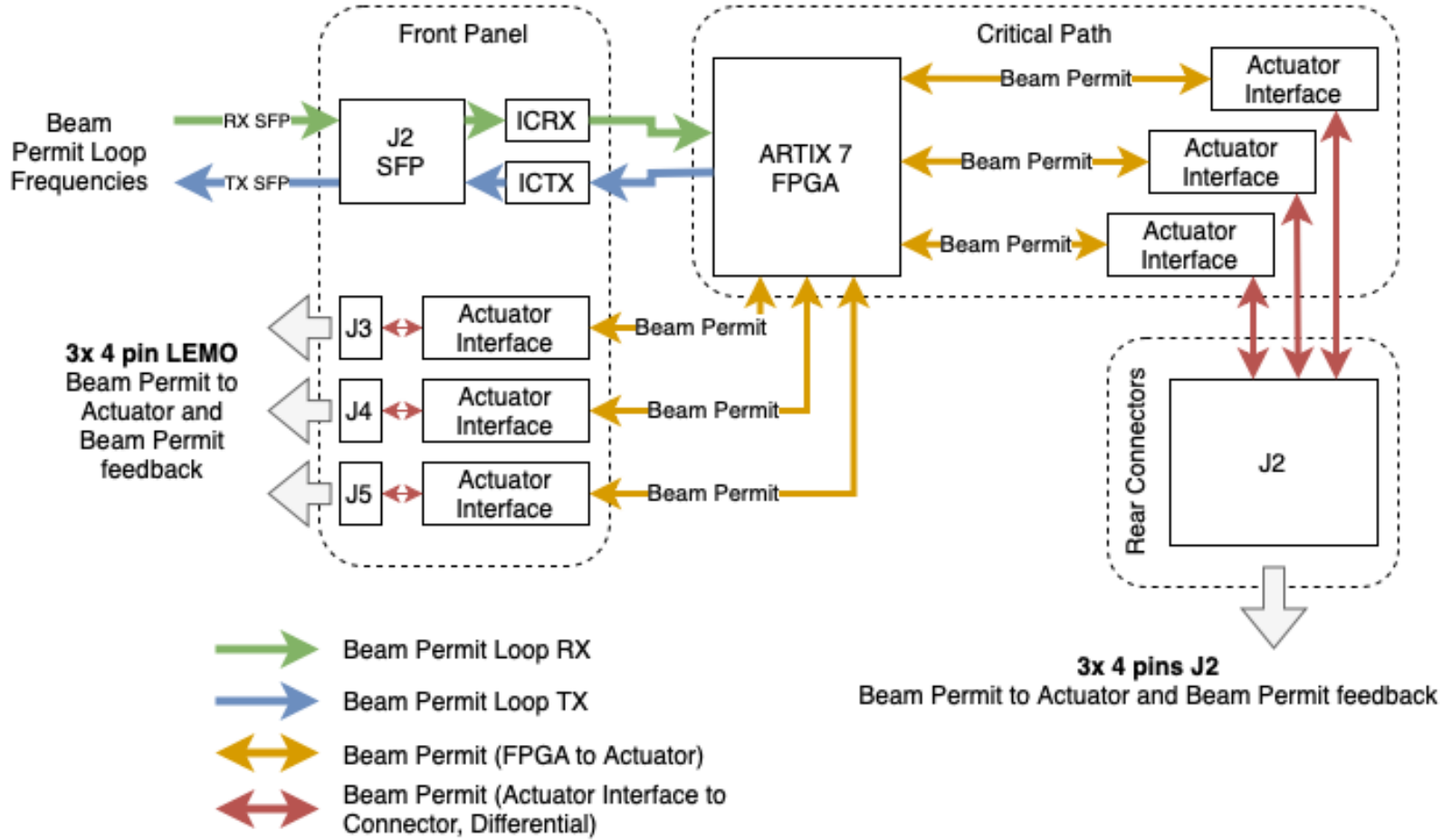
Distribution of components across pages

Total number of components: 681



Critical Path

Simplified diagram



End-effects

BISv2 list

1. **Blind failure**

When occurring, the CIBAB will not be able to dump the beam when required (i.e., when detecting ruptured BIS loop).

2. **False dump**

The failure would result in an unnecessary beam dump, stopping the LHC fill and likely causing follow-up interventions.

3. **Maintenance**

Maintenance actions such as repairs or replacements will take place after finishing a running LHC fill.

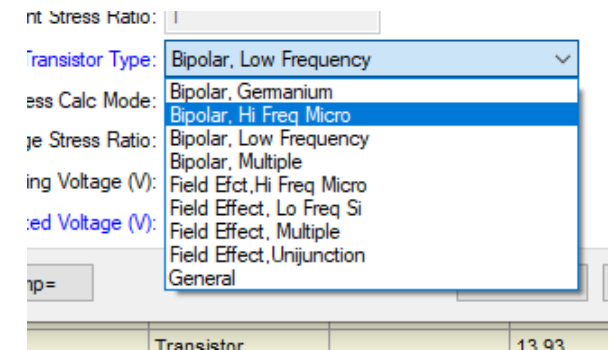
4. **No effect**

Given failure mode occurring will not result in any direct or indirect consequences.

Main contributors to total failure rate

Part I

- 1. Transistor, Dual N-Channel 2.5V:** 2 x 21.88 FITS (source: 217Plus)
 - Assigned “Field Effect, Multiple” category
- 2. 23 transistors, Dual NPN General Purpose:** 2 x 13.93 FITS (source: 217Plus)
 - Assigned “Bipolar, Low Frequency” category
- 3. 14 SMD Multilayer Ceramic Capacitors:** 12.31 FITS (source: 217Plus)
 - Operating voltage 3V, rated: 6.3V
 - Capacitance: 47 μ F
- 4. FPGA Artix 7 and FPGA Spartan 7:** 11 FITS (source: manufacturer HTOL test)
- 5. SMD Multilayer Ceramic Capacitors:** 10.07 FITS (source: 217Plus)
 - Operating voltage 3V, rated: 6.3V
 - Capacitance: 4.7 μ F
- 6. 3 CFPS-73 oscillators (OSC1 - OSC3):** 7.76 FITS (source: CFPS-73 mails)



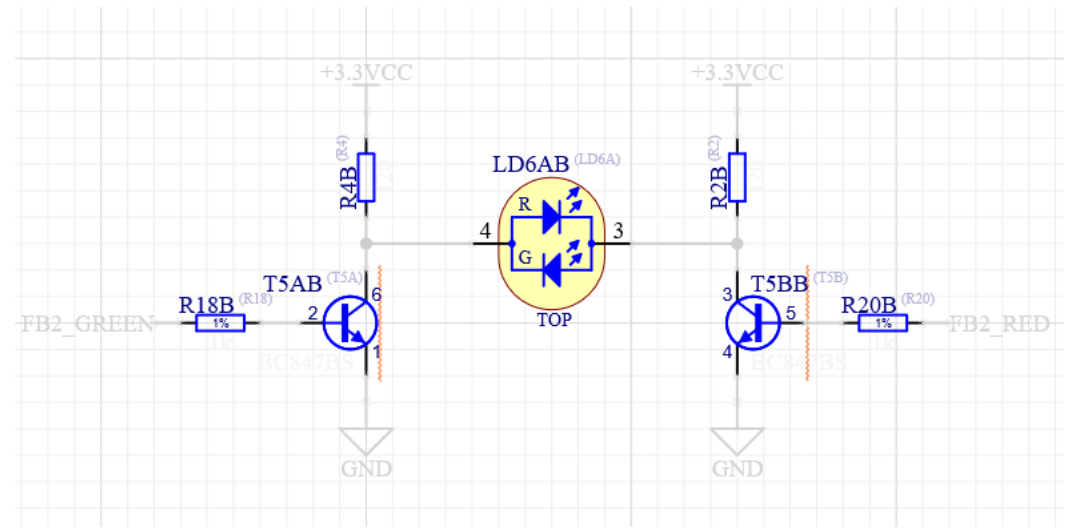
Main contributors to total failure rate

Part II

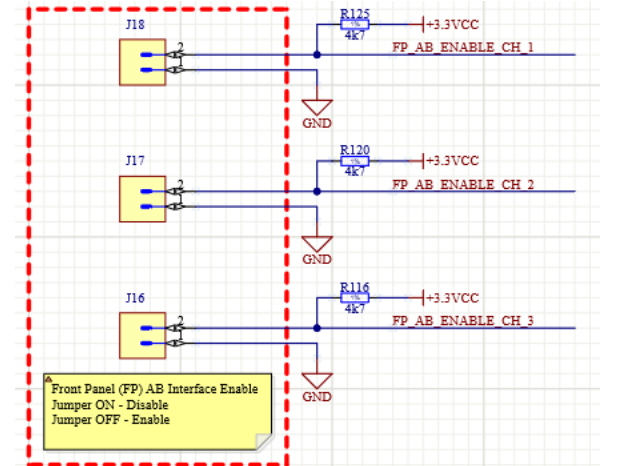
7. **4 TVS diodes:** 5.7 FITS (source: 217Plus).
 - Operating voltage set to rated voltage (3.3V).
8. **ADCs (MAX1239EEE):** 5.71 (source: manufacturer data).
9. **2 Translators (Differential to LVTTTL/LVCMOS and vice versa):** 4.83 FITS (source: manufacturer data).
10. **2 SMD Multilayer Ceramic Capacitors:** 4.32 FITS (source 217Plus).
 - Operating voltage 3V, rated: 10V.
11. **24 TVS diodes:** 4.3 FITS (source: 217Plus).
 - Operating voltage 3.3V (default), rated: 30V
12. **2 IttyBitty Oscillators:** 3.5 FITS (source: manufacturer data).

Questions

1. Why are there 3 instead of 2 sets of signals on the output?
 - I.e., BEAM_PERMIT_1, BEAM_PERMIT_2, BEAM_PERMIT_3 (OUT_P, OUT_N, FB_P, FB_N).
2. Is there a designator naming convention?
 - See the example below.
 - Letters at the end also used to refer to the same component in multiple places (i.e., FPGA).
3. Can a misconfiguration of enabling/disabling Front Panel or Rear Connectors modes impact operation?
4. Temperatures assumed for failure rate prediction:
 - 25°C non-operating,
 - 35°C operating,
 - 10°C case temp rise (where applicable).



Actuator LEDs (VME)



Actuator Board CP Config



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