CIBAB FMECA

BISv2 Reliability Study Progress Meetings

List of contents

1. Summary statistics

2. End-effects' FITS in design pages

3. Blind failures
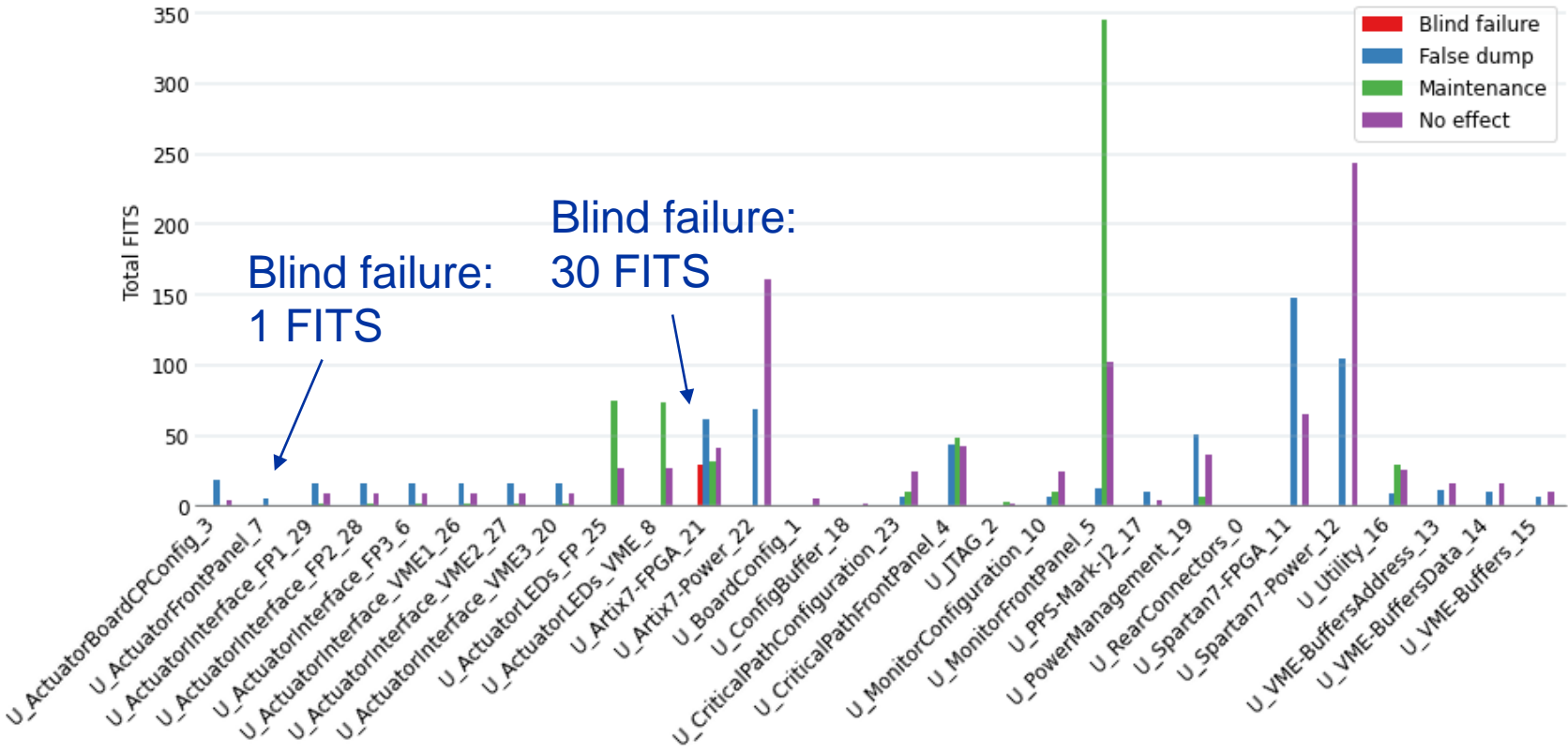
4. False dumps

5. Questions

Summary statistics

- **Total number of components: 681**

- **Total FITS: 1,867 FITS**

- **Failure rates:**

  - Blind failure rate: 31 FITS

  - False dumps: 451 FITS

  - Maintenance: 591 FITS
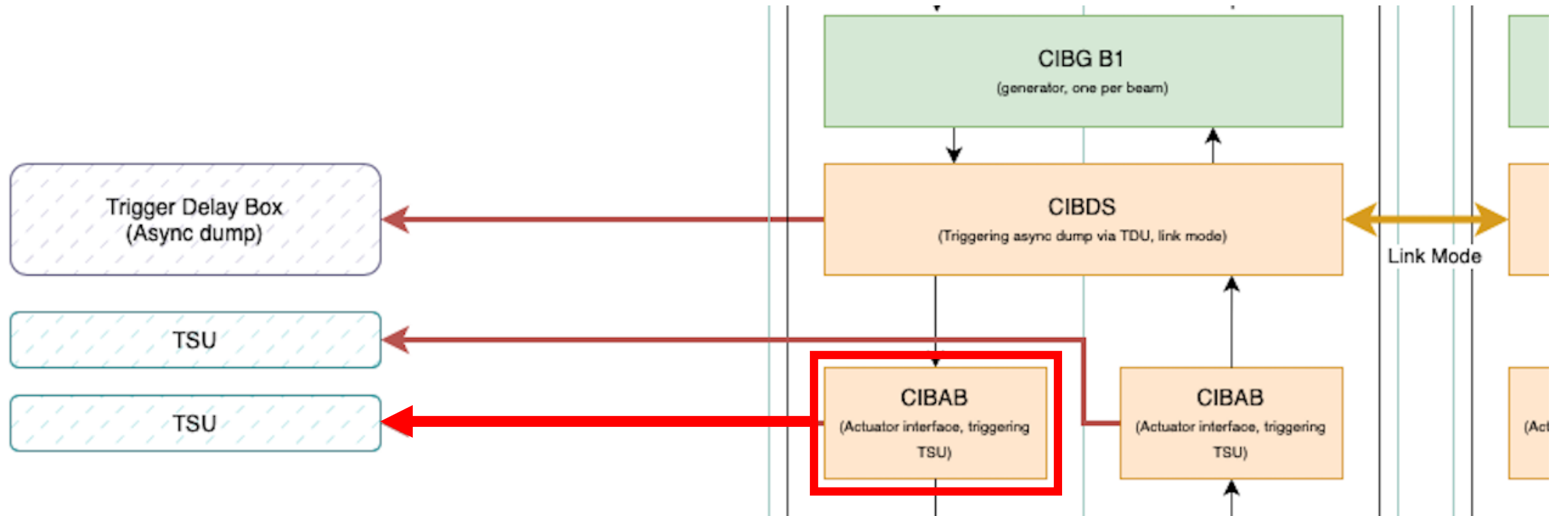
  - No effects: 794 FITS

End-effects' FITS in design pages

Blind failure

Considered from a perspective of a single CIBAB. Failures within the red box preventing the signal from the CIBAB card go to TSU via the red arrow.

Blind failures
## Causes

- **Short** or **stuck low** of the **Artix 7 FPGA**: 11 FITS (each failure mode)

  - Comment on short: "Short between actuator output and GND -> equivalent to BP true"

  - Comment on stuck low: "Stuck low on actuator output = Beam permit TRUE"

- **Parameter change** of the **oscillator OSC2** in **Artix 7 page**: 7.8 FITS

  - "Potentially if the timing constraints within the FPGA are not met anymore, though very unlikely because the BPL detection consists of two separate mechanisms + the PLL will become unlocked if it shifts too much. Probably False Dump then" – to be discussed

- **Short** of **connectors J3, J4, J5** in **Actuator Interface**: 0.3 FITS each

  - Comment: "if short between FB and OUT?"

- **Short** of **har-bus J20** in Rear Connectors: 0.02 FITS

  - Comment: "if short between FB and OUT?"

False dumps

- **Individual components triggering a dump of the beam because of an error**

- **Top contributors:**
  - Transistor FDS9926A, T2, short - 35 FITS
  - Spartan 7 FPGA (open, short, stuck) – 7.3 FITS
  - Oscillators (OSC1, OSC2) in the FPGA pages – 6 FITS.
  - 4 diodes (D25-D28) – 5.7 FITS.
  - Capactiors in the FPGA pages – 3.7 FITS.
  - Artix-7 FPGA (open, stuck high) – 3.6 FITS.
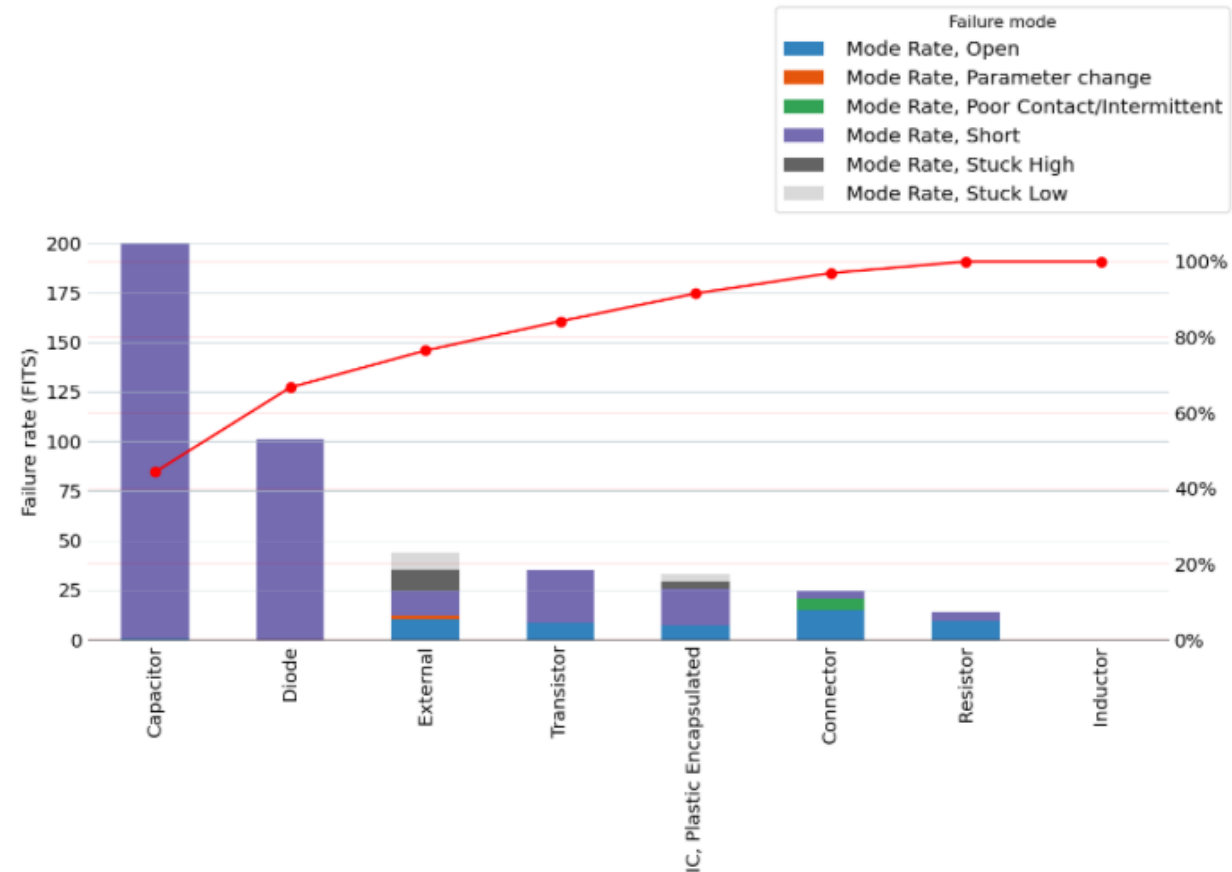
Transistor reliability
In different standards on BC847BS example

STANDARD	FITS	MAIN PARAMETERS	COMMENTS
217PLUS	15.12	**Type**, temperature, electric stress	Assuming it is "bipolar, low frequency"
MIL-HDBK-217F	0.6	Application, quality, temperature, power and voltage, connection type, number of pints, theta case/ambient and theta junction case	With some not-exact parameters
TELCORDIA	0.12 – 0.87	Power, voltage, type, packaging, **quality**	Depending on quality factor
FIDES	10 – 38	Type, case, **quality**, experience. Placement, theta junction ambient, power	Depending on quality factors
MANUFACTURER	0.23	High Temperature Reverse Bias test	60% CL

Questions

- **"Not sure if post mortem/preop check will check the state of this signal, probably not"**

  - Should we take a specific approach? End-effect: "Maintenance"

  - Similar "post mortem could fail if PPS/MARK lost" (with an end-effect "false dump")

home.cern